Dynamically Reconfigurable Sensor Electronics – Concept, Architecture, First Measurement Results, and Perspective

by

Senthil Kumar Lakshmanan & Prof. Andreas König

Contents:

➢ Challenges in Sensor Electronics
➢ Concept of a Dynamic Reconfigurable Sensor Electronics
➢ First Dynamic Reconfigurable Hardware Architecture & Implementations
➢ Measurement Results
➢ Perspective – Training Board
➢ Conclusion & Future Works
Challenges of Sensor Electronics

Typical Embedded System

- Typically with indispensable analog & mixed-signal circuits
- Sensor electronics subject to mismatch, static & dynamic drift, noise manufacturing problems ...
- Remedy: careful design & calibration/trimming at production time
- Drawbacks: slow, costly & irreversible.
- On the fly calibration desirable …, recent evolutionary techniques
Challenges of Sensor Electronics

State-of-art

- Recent approaches and products support dynamic self-calibration of analog systems/components

**ALD2724x (EPAD)**
- Trimming-
- EEPROM (finite correction cycles)

**AD8555 (DigiTrim)**
- Trimming-
- DAC (infinite correction cycles)

- Conservative methods time discrete, on building block level when dynamic.

**AnadigmVortex**

**KIP FPTA**

**JPL FPTA**

- Evolutionary Approaches

- Approaches differ in granularity
Challenges of Sensor Electronics

Motivation

➢ Inspite of good results, drawbacks of fine granular evol. approaches are,

   • Starts from *primal soup, wastes wealth of designers knowledge*
   • Too much flexibility, a curse – large area, large parasitics & expensive
   • Excessive switching resources –frequency behavior & susceptibility to noise
   • Peculiar & non-established circuit structures (Suitable for space applications)
   • Large memory & high reconfiguration time
   • Principally feasible to realize complex structures- industry spec fulfillment -?
   • Missing programmable *passive* components - Linear behavior remains open

➢ Industrial requirements *contradict black box* like structures
Concept of Dynamic Reconfigurable Sensor Electronics

Objectives

a) Investigation of Industrial applicability of EHW concepts

b) Satisfying the industrial needs in particular to sensor electronic- transparent structure

c) Consideration of Technology dependency (ITRS) & substrate issues to address the problem

d) Flexible & dynamic reconfigurable HW platform with inherent fault tolerance

e) Provides both programmable active & passive components - linearity for Res.

f) HW structure supporting Rapid Prototyping

g) On the fly & Auto calibration capabilities

h) Facilitates the implementation potentials of the desirable Self-X properties
Inclusion of dynamically reconfigurable mixed-signal FPMA

Inherently, fault-tolerance and self-x-features of OC are provided

Initially for sensor electronics, later for actuators
Overall reconfigurable embedded system architecture (*sensor-in-the-loop*)

3 functional blocks namely, Assessment, Optimization (self-x features) & Reconfigurable HW.

Assessment Unit - Aids in Parameters Assessment, e.g., for OPA- Gain, SR, PM, CMR etc. still in time discrete

- Optimization Unit - GA/PSO
  (More info by Peter Tawdross at 11:30)

- Reconf.HW- Time continuous
  medium granular,
  dyn.reconfig. HW
  hybrid FPAA/FPTA
Dynamically Reconfigurable Sensor Electronics
FPMA Building blocks

- Current FPMA with 3 self-trimmable amplifiers
- Amplifiers capable of changing AR (time-Cont.)
- Amplifiers complemented with reconfigurable passive components both cap. & res.
- Supports rapid-prototyping & dynamic reconfiguration

FPMA
Adaptive Sensor Signal Conditioning & Conversion

R,C Scalable R,C FPMA

Miller OPA  
+ -  

FC OPA  
+ -  

InAmp

Global Switches

Senthil Kumar Lakshmanan and Prof. Andreas König
Dynamically Reconfigurable Sensor Electronics
Basic Building - Block Design

- Basic blocks - heterogenous array of components – intermediate granular
  - ST (nmos & pmos), SC & SR
- Digital device selection through Shift Registers (SR)
- Scalable devices vary in powers of 2 inspired from D/A converters
- Dimensions fixed through simulations & technology dependent
- Components of hetero. array connected by transmission gate switches, W/L
  - Optimized for frequency behavior
  - Consideration of on-resistance of switch is important
First Reconfigurable OPA Implementation
Physical Realization of Scalable Devices-Active

- **Scalable Transistor with SR**
- Reconfigurable bits -11
- Scalable range (simulations)
  - Width = (1, 2, 4, 8, 16, 32, 64, 128 in µm)
  - Length = 1µm

- **Flexibility** … area criterion

- Area - ST(NMOS) 60µm*64µm
  - ST(PMOS) 65µm*69µm

- Austriamicrosystems 0.35 µm CMOS (4metal 2poly) process
First Reconfigurable OPA Implementation
Physical Realization of Scalable Passive Devices

- Passive reconfigurable bits – 8
- Scalable range Powers of two
  - Capacitor = (125f, 250f, 500f, 1p, 2p, 4p, 8p, 16p)
  - Resistors = (125Ω, 250Ω, 500Ω, 1KΩ, 2KΩ, 4KΩ, 8KΩ, 16KΩ)
- Effective for compensation and in Feedback circuitry
- Area
  - Scalable Capacitor (245µm*215µm + 17µm*156µm)
  - Scalable Resistor 213µm*53µm
First Reconfigurable OPA Implementation
Fixed Topology: Miller-OPA

- Sequential Device selection through SR

- Simple Miller OPA- Replacement scheme of unit devices by scalable version
First Reconfigurable OPA Implementation

Mixed-Signal Simulations: Miller OPA

- Complete Miller OPA with digital interface
- Timing diagram of transient analysis
- O/P
- I/P (1KHz-1MHz)
- EN
- Data (e.g., 10010)
- Clock
- Loading time 32µsec
- Consist of 13 Scalable devices – Programmable $C_c$
- Adhoc layout structure – matching not included
First Reconfigurable OPA Implementation

Mixed-Signal Simulations: FC - OPA

FC-OPA with digital interface

- Timing diagram of transient analysis

O/P

I/P (1KHz-1MHz)

EN

Data (e.g., 10010)

Clock

- Loading time 64 µsec
- Consist of 25 Scalable devices
First Reconfigurable OPA Implementation

Instrumentation amplifier

- Standard 3 Opamp, 7 resistor structure
- FC-OPA building block
- Resistor value ranges to 255 Ω
- In-Amp area = (367*1149)µm²

- Area comparison study - Miller OPA

<table>
<thead>
<tr>
<th>OPA Structure</th>
<th>OPA Area-Unit Devices</th>
<th>OPA Area-Scal. Analog Devices</th>
<th>OPA Area-Mixed cell</th>
<th>Ratio of Used to Available OPA area In %</th>
</tr>
</thead>
<tbody>
<tr>
<td>Miller</td>
<td>0.0085 mm²</td>
<td>0.10 mm²</td>
<td>0.25 mm²</td>
<td>3.4</td>
</tr>
</tbody>
</table>
Three module chip
Miller OPA
FC-OPA
InAmp (FC-OPA)

Chip as single / multiple instances to realize structures like Filters, ADC …

- Three module chip
- Miller OPA
- FC-OPA
- InAmp (FC-OPA)

- Chip as single / multiple instances to realize structures like Filters, ADC …

- 3 Additional pins D, Clk, EN
- Chip area 2.3mm * 2.1mm
- 40 – Pins
- Dual In Line package

(Pre-fabricated chip)

(Post-fabricated chip)
Measurement Results of Our First FPMA

<table>
<thead>
<tr>
<th>S.Nr.</th>
<th>OPA Parameters</th>
<th>Measured Values</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Slew Rate</td>
<td>0.03V/µSec</td>
</tr>
<tr>
<td>2</td>
<td>CMR</td>
<td>1.3</td>
</tr>
<tr>
<td>3</td>
<td>Offset</td>
<td>0.9mV</td>
</tr>
<tr>
<td>4</td>
<td>Settling time</td>
<td>35µSec</td>
</tr>
</tbody>
</table>

Miller OPA

<table>
<thead>
<tr>
<th>S.Nr.</th>
<th>OPA Parameters</th>
<th>Measured Values</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Slew Rate</td>
<td>0.09V/µSec</td>
</tr>
<tr>
<td>2</td>
<td>CMR</td>
<td>1.7</td>
</tr>
<tr>
<td>3</td>
<td>Offset</td>
<td>2mV</td>
</tr>
<tr>
<td>4</td>
<td>Settling time</td>
<td>14.4µSec</td>
</tr>
</tbody>
</table>

FC - OPA

Inverting Miller OPA

Inverting FC - OPA
Generic Operational Amplifier (GOPA)
Feasibility of the Concepts

- Special structure- flexibility within known amplifier topologies
- 40 scalable devices & 60 TS (Topology Switches)
Generic Operational Amplifier
Flexible Topology Selection

- Cascoded current mirror
- Diode loaded differential pair
- Cascoded second stage
- Bootstrap biasing feasible
Generic Operational Amplifier
Flexible Topology Selection

- Fully differential OPA
- Scalable pole - zero compensation

- Telescopic OPA-Wilson current Source
Simulation Results
Result Comparison (Miller-OPA) Transient vs. AC-Analysis
Fixed Topology vs. GOPA Block

GOPA
- Dynamic modification of AR and amplifier topology
- Capable of realising 16 different amplifier structures
- large area 1512µm*552µm – feasibility study
Suitable Teaching Platform
Analog Designers Advanced Training Board

- PSPICE
- Netlist Generation
- Converted Bit Chain
- Embedded System
- RS 232
- PHYTEC miniMODUL-515C

Chip Designer
Re-design Option
- e.g., Inv OPA with parasitic effects

View results
Suitable Teaching Platform
Analog Designers Advanced Training Board

PSPICE
Netlist Generation
ST-11, SC-9, SR-8
Converted
Bit Chain

Chip Designer
Re-design Option

– e.g., Inv OPA with parasitic effects

View results

Embedded System
PHYTEC miniMODUL-515C

(schematic entry)

RS 232

Senthil Kumar Lakshmanan and Prof. Andreas König
Suitable Teaching Platform
Analog Designers Advanced Training Board

PSPICE
Netlist Generation
(e.g., 0101011100…
(138, 270 & 1258 bits)

Chip Designer
Re-design
Option
– e.g., Inv OPA with parasitic effects

View results

Embedded System
PHYTEC miniMODUL-515C

Converted Bit Chain
ST-11, SC-9, SR-8
(e.g., 0101011100…
(138, 270 & 1258 bits)

RS 232
Interface
Suitable Teaching Platform

Analog Designers Advanced Training Board

PSPICE Generation

Netlist

ST-11, SC-9, SR-8

e.g., 0101011100…
(138, 270 & 1258 bits)

Converted

Bit Chain

Chip Designer

Re-design

Option

New entry - based on re-design

View results

– e.g., Inv OPA with parasitic effects

Embedded System

PHYTEC miniMODUL-515C

RS 232

(schematic entry)

Interface

Senthil Kumar Lakshmanan and Prof. Andreas König
Conclusions & Future Works

- Design of Reconfigurable Operational Amplifier validated
- Generic amplifier block on intermediate granularity level
- Aspect ratio and amplifier topology can be dynamically modified
- Measurement performed to prove the basic functionality
- Overall view of the embedded system
- On the fly & Auto-calibration feasible
- Inherent fault-tolerance and self-X capability

- Measurement for predictable industry like behavior & substrate noise issues
- Next generation FPMA chip would be upgraded - ultra low power OPA, transimpedance amplifiers, Working Instrumentation amplifier , V-I, I-V etc.
- Targets at Generic Sensor Electronic Front End.
Thanks For Your Attention