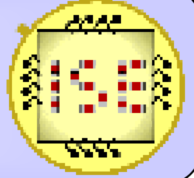
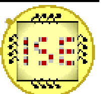


Multi-project Sensor Chip Design
Global Pad Placement

Jiawei Yang

February, 2009

Prof. Dr.-Ing. Andreas König

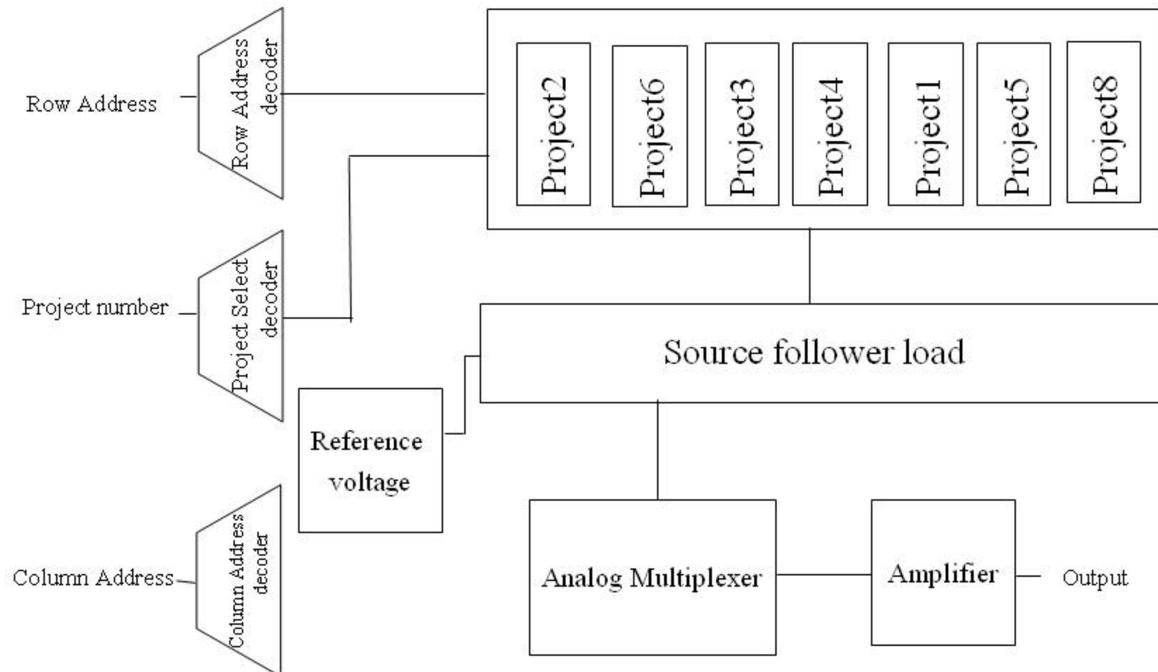


Overview

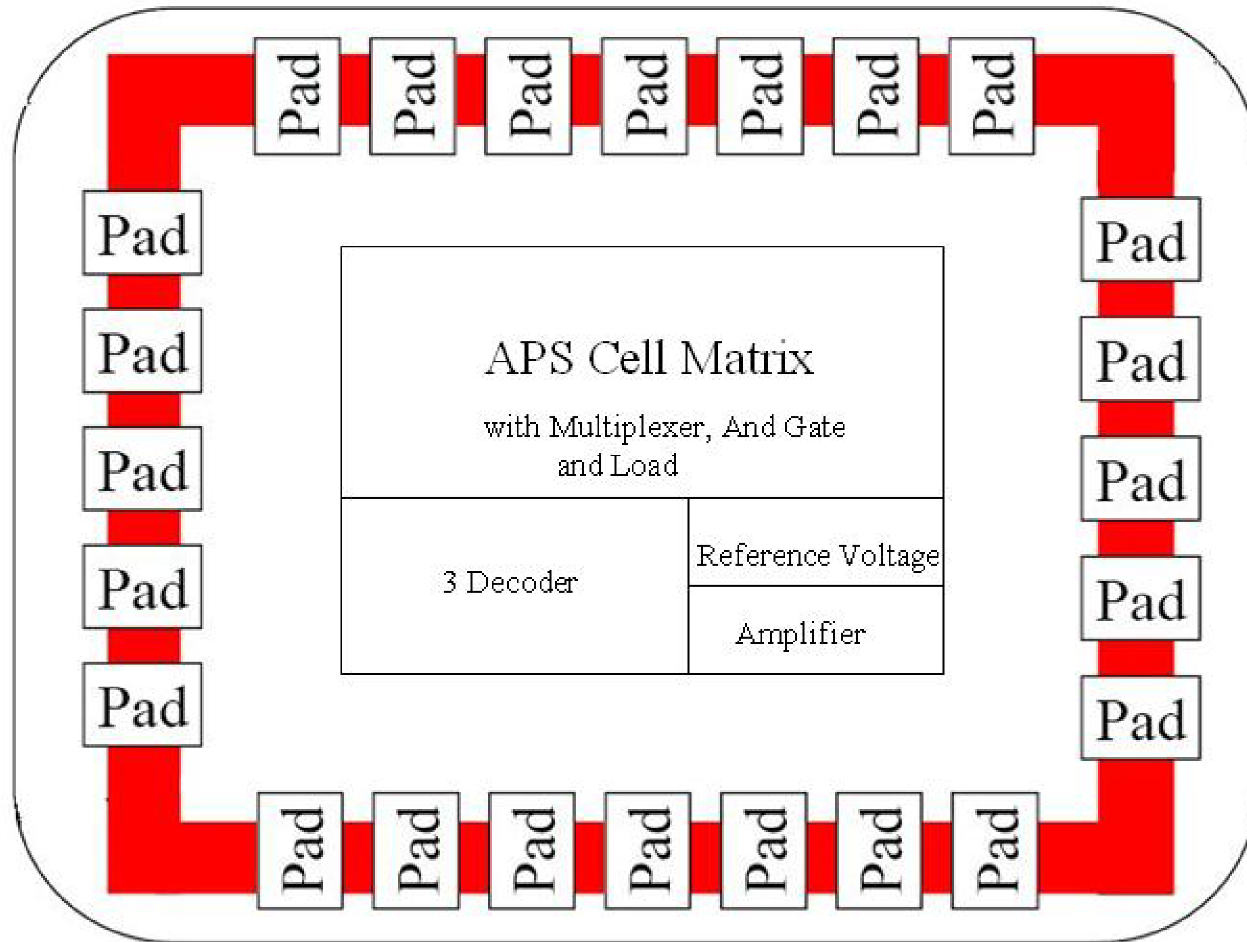
1. Introduction
   - *Task*
2. Parts of the Project
   - *Global Schematic*
   - *Global layout*
   - *Simulation*
   - *Pins*
   - *Pads selection*
   - *Package*
   - *Pads Placement*
3. Conclusion
   - *Signal pad*
   - *Power pad*

Task

This global task is to place the I/O pads and global pads for the Multi-project Sensor Chip.



Task



Individual Project

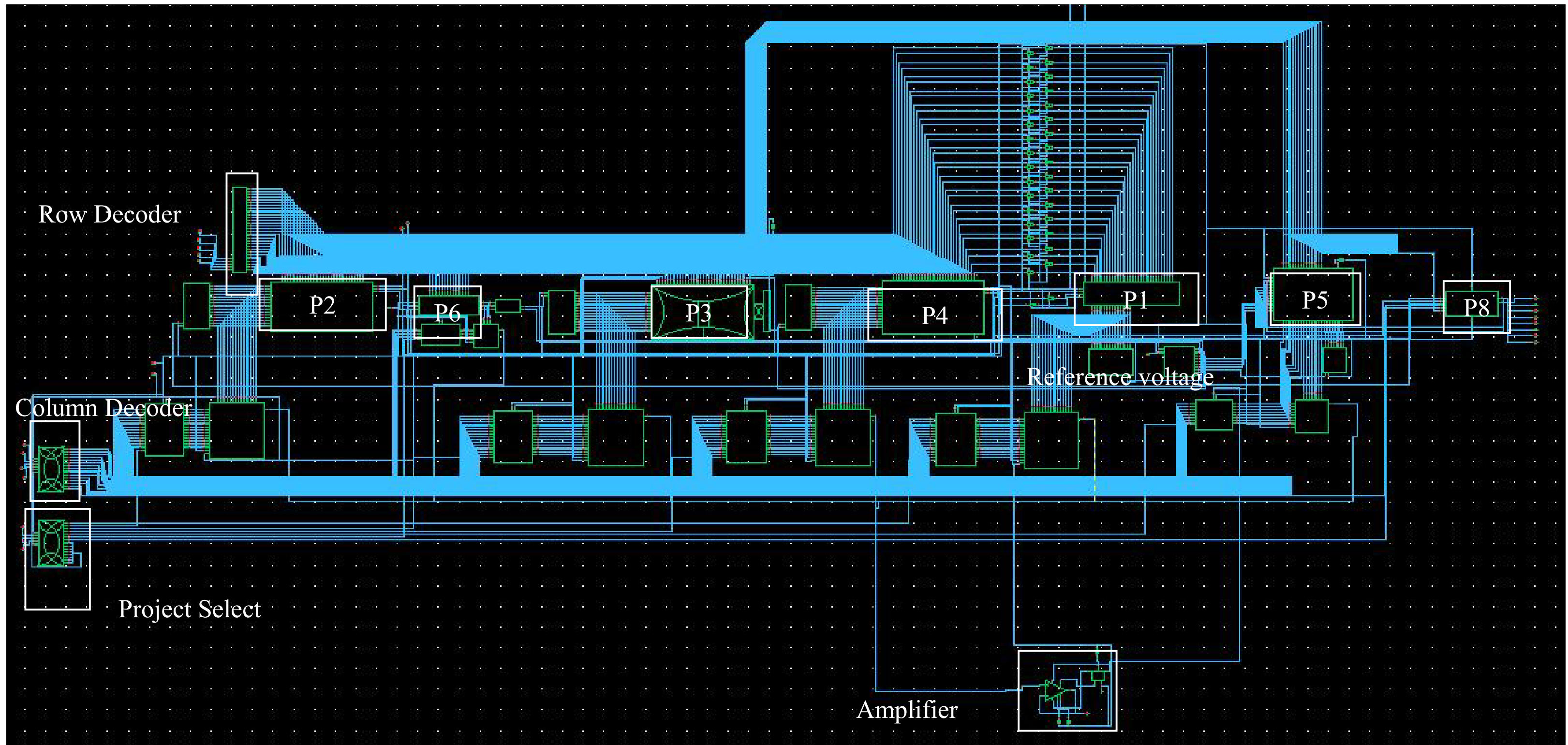
- Project 2: Designed by Abhay
- Project 6: Designed by Kuan Shang
- Project 3: Designed by Mahesh
- Project 4: Designed by Jiawei Yang
- Project 1: Designed by Juergen Hornberger
- Project 5: Designed by Robert Freier
- Project 8: Designed by Hetteries Martin

(links to the ppt of each project can be added later)

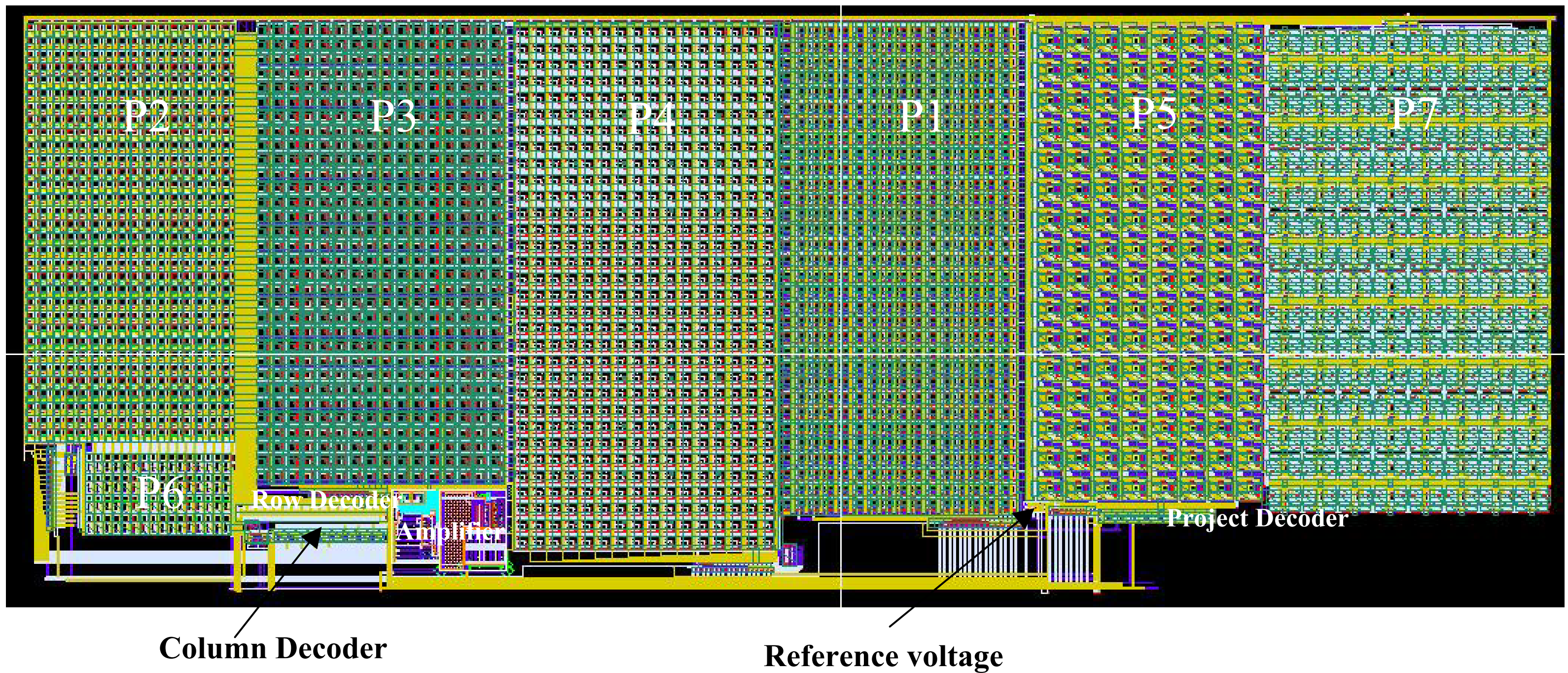
Global Task

- Placing, Routing, global simulation: Juergen Hornberger
- Global decoder cells Rows/columns: Abhay
- Analog MUX design and layout: Mahesh
- Placements of I/O pads and Global pads: Jiawei Yang
- Source follower load placements: Robert Freier
- Reference voltage: Kuan Shang

Global Schematic

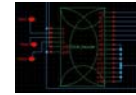


Layout



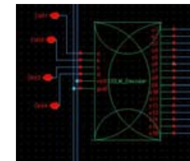
Simulation

- Simulation from schematic
- Project Selected by Project Select Decoder
  Project 4, input signal: 011(LSB Pbit3)



- Row Selected by Row Address Decoder
  Row 2, input signal: 00001 (LSB Rbit5)

- Column Selected by Column Address Decoder
  Column 2, input signal: 0001 (LSB Cbit4)



- VDD, Shutter, Reset: 3.3v
- IREF: 11.7uA

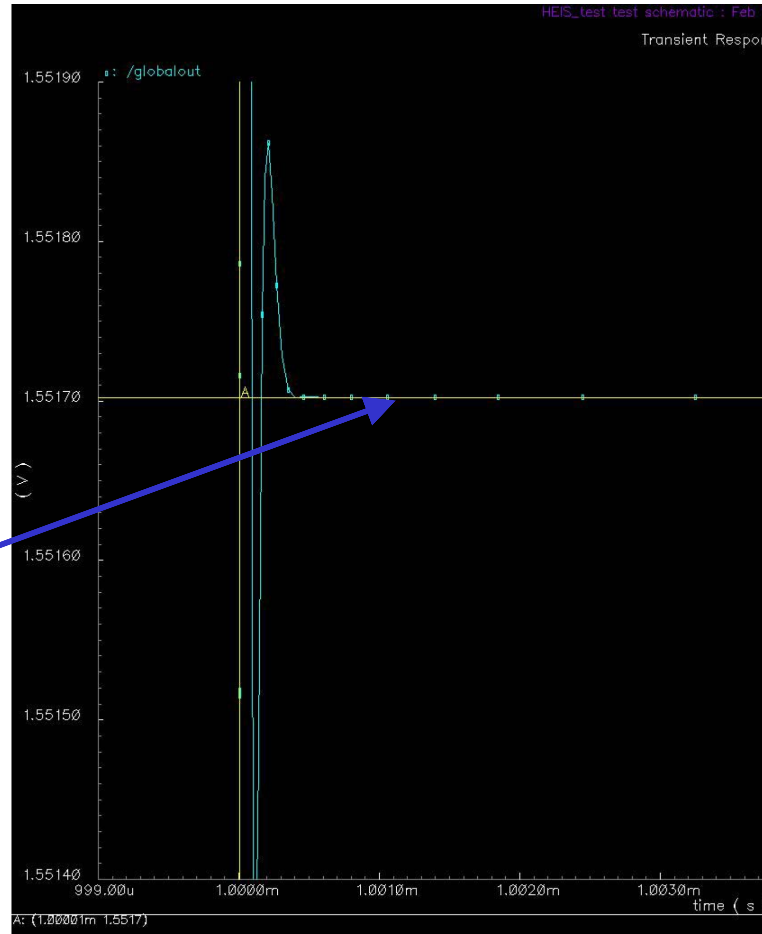
Result

Simulation Result

Project4

Simulation Result

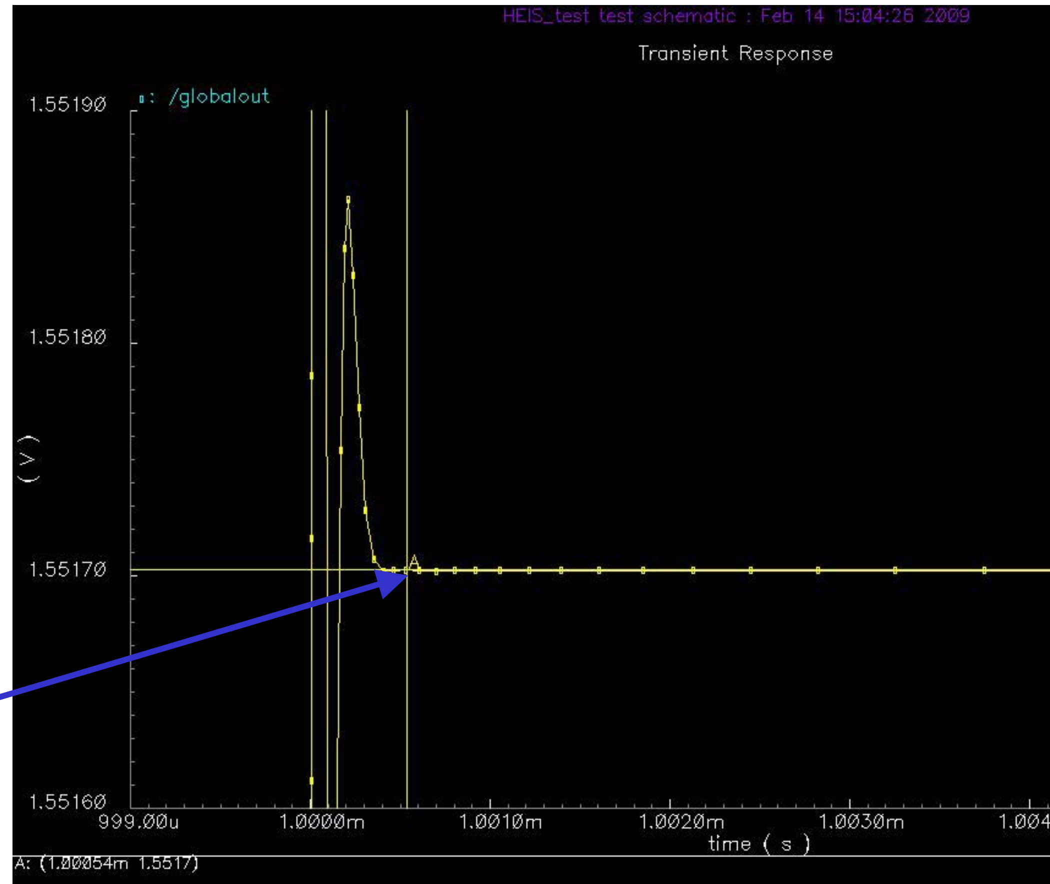
Offset voltage



A(1.00001m, 1.5517v)

Simulation Result

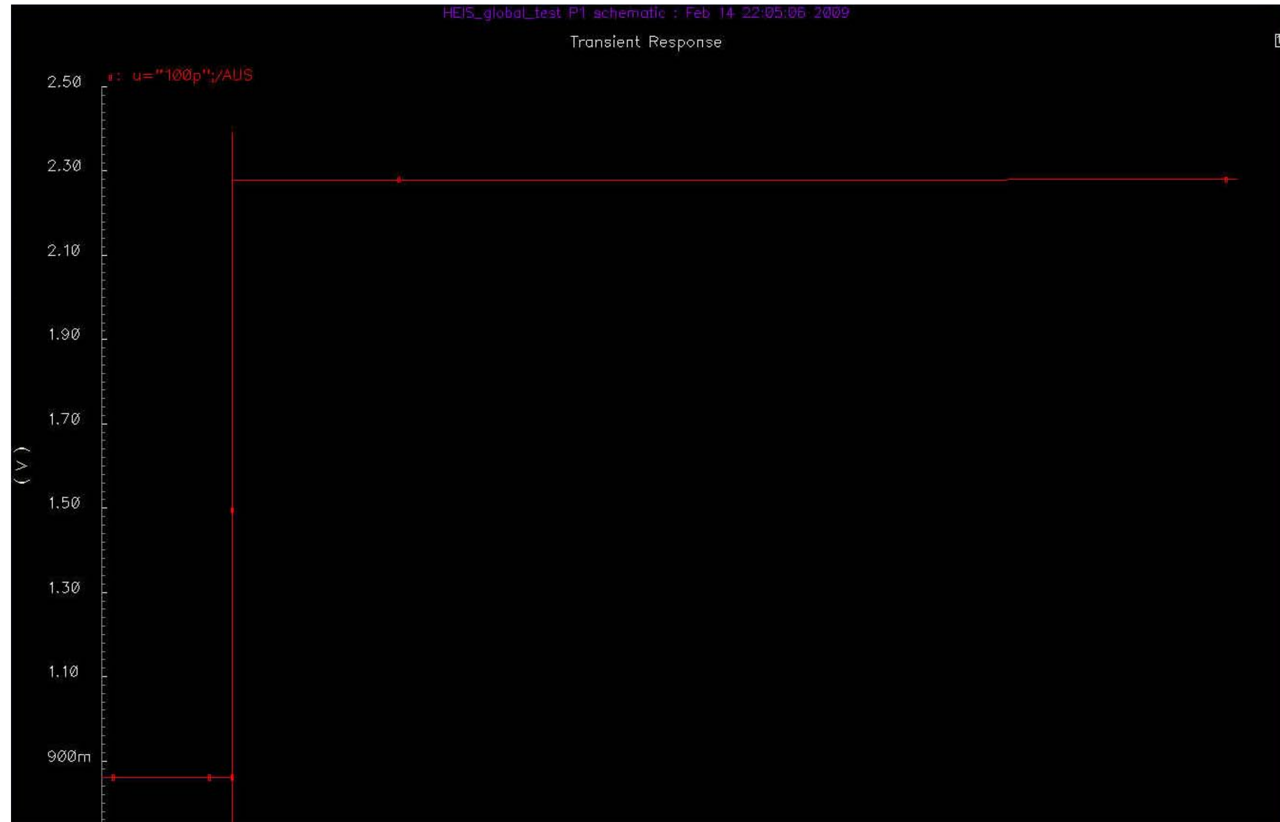
Readout Time



A(1.00054m, 1.5517)

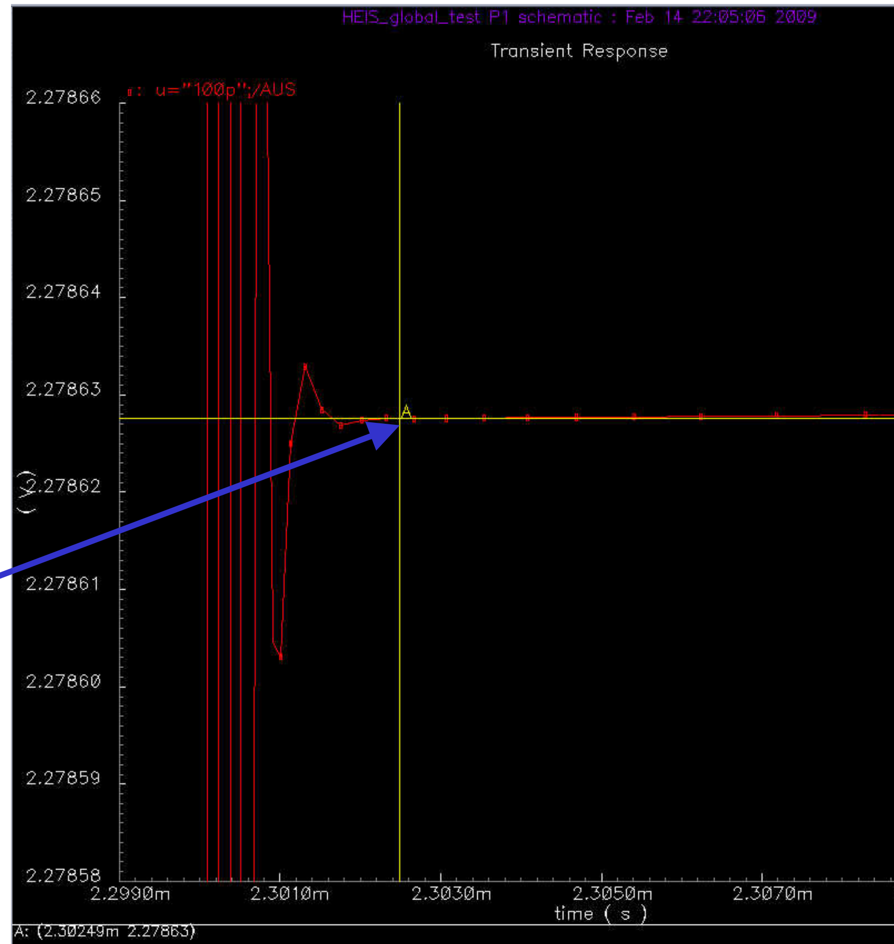
Simulation Result

Project1



Simulation Result

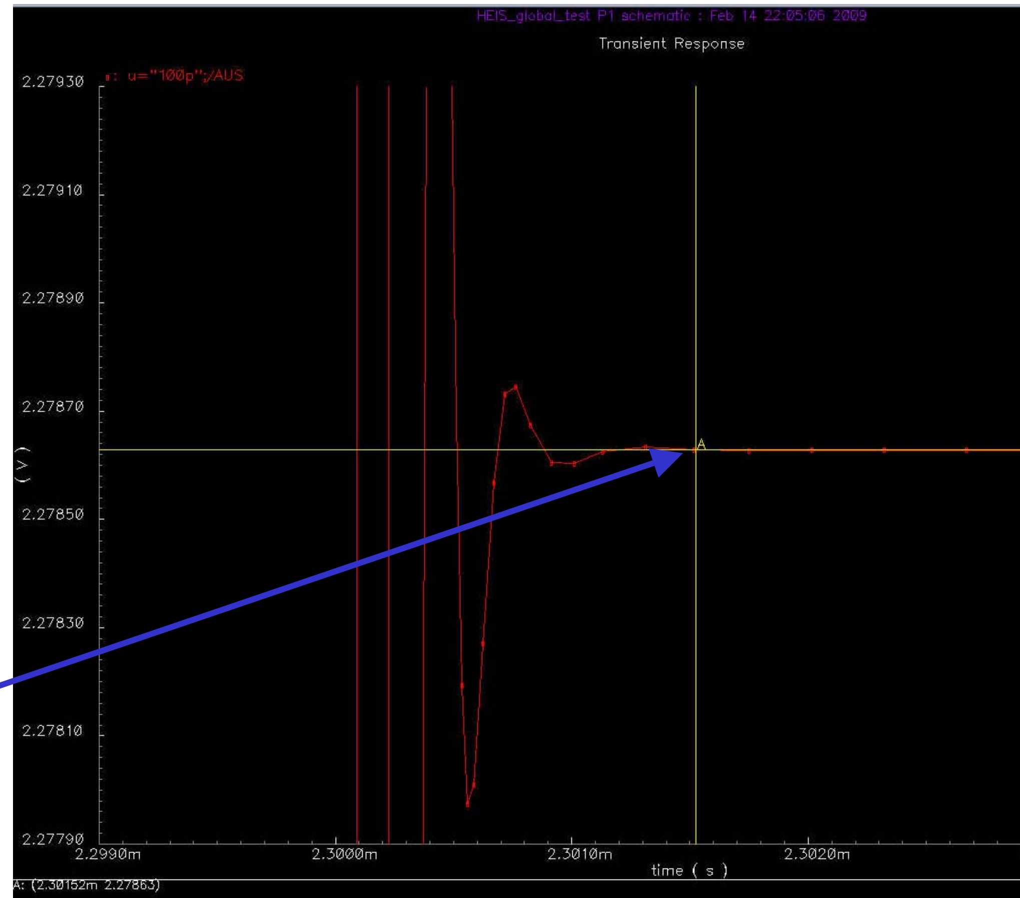
Offset voltage



A(2.3m, 2.278v)

Simulation Result

Readout Time



A(2.30152m, 2.278v)

Result

Input								Output	
Project	**VDD**	**Row Decoder Input**	**Column Decoder Input**	**Project Decoder Input**	**Rest**	**Shutter**	**IREF**	**Output Voltage**	**Readout Time**
Project4	3.3v	00001	0001	011	3.3v	3.3v	11.7uA	1.5517v	540ns
Project1	3.3v	00010	0010	000	3.3v	3.3v	11.7uA	2.278v	1520ns

Signal pad

- Signal pad die placement considerations:
- The logic located on the die that will connect to the pad.
- Bonding wire angles.
- Cross-talk between pads.
- The analog pad should be as close as to the analog signal.
- ESD considerations – charge concentrates at points, like in comers of the die – pads placed in the corners of the die may be more susceptible to ESD, so use VSS pads in the die corners.

Power pad

- Power pad die placement considerations:
- Don't place different power rails next to each other.
- Power pads should be close to fast switching outputs with high slew rates, particularly if those output pads drive large loads.
- The ground pad of the digital device and the Analog device should be separated (if necessary).

Pad Placement Strategy

- Counts the number of pins.
- Conclusion the pads number and types.
- Select the package according to the number of pads.
- Considering the shape of the package and the circuit.
- Considering the bonding rules.
- Considering the distance between the pads.
- Considering the whole circuit structure and path delay, in order to reduce the interconnection length and circuit delay.
- Minimum core/chip area consumption
- Pad placement

Pad Selection

Device	Pin Name	Pin used	Pin type	Pad select
Row Select Decoder	Rbit	5	digital input	ISP_3B
Project Select Decoder	Pbit	3	digital input	ISP_3B
Column Select Decoder	Cbit	4	digital input	ISP_3B
Global	Shutter	1	digital input	ISP_3B
Global	RES (reset)	1	digital input	ISP_3B
Global	vdd!	1	VDD	AVDDALLP
Global	gnd!	1	Ground	AGNDALLP
Reference Voltage	IREF	1	analog input	APRIO200P
Project5	Vmode Vconfigure Vin0 Vin1 Vin2 Vin3 Vin4 Vin5	8	digital input	BBC8P_3B
Project8	Output	8	digital output	BBC8P_3B

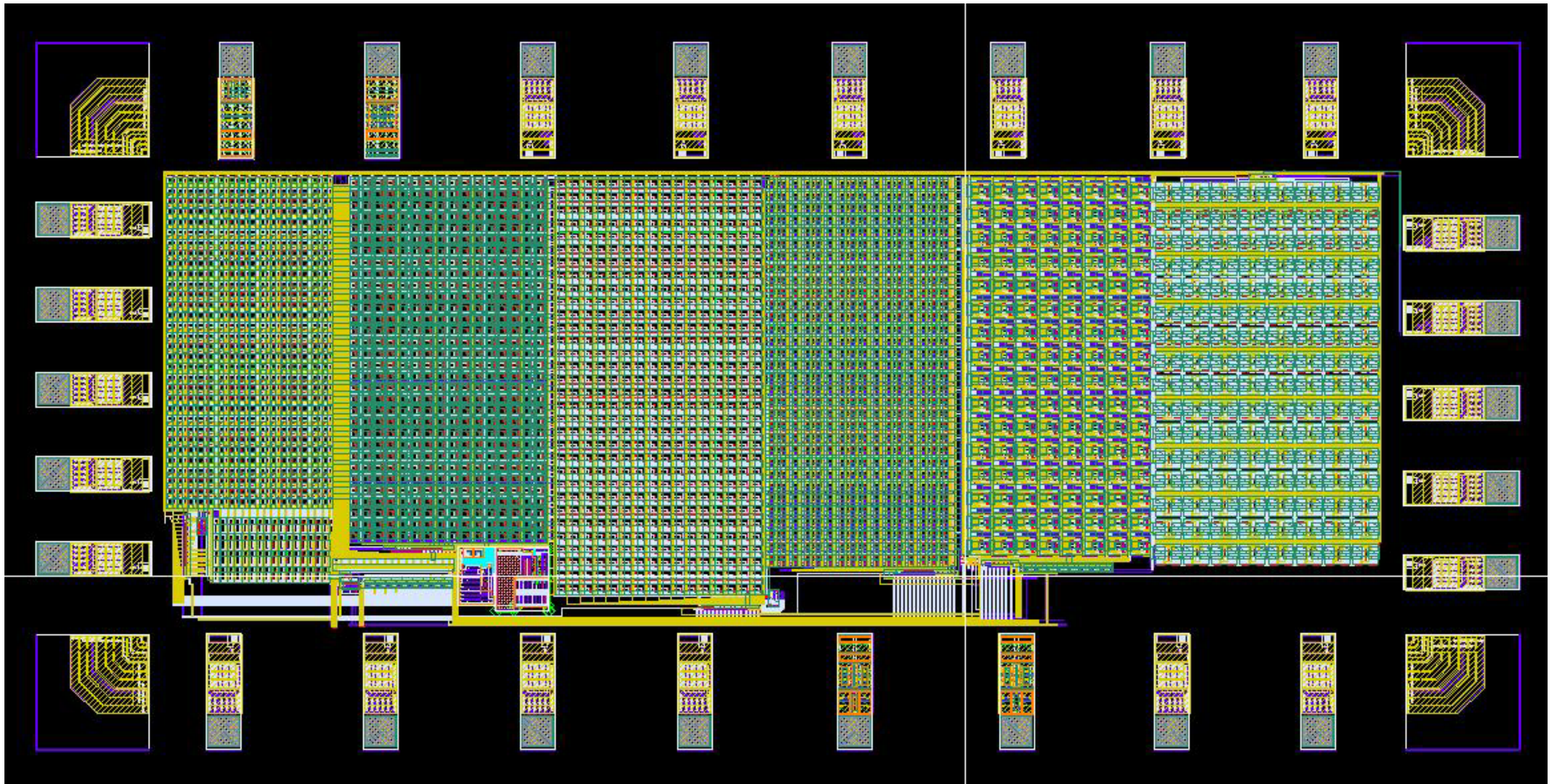
Pad Placement

- The total pins are 34.
- Project 5 and 8 can share the 8 pins by bidirectional pads.
- Total pads: 26
- Select DIL_28 package
- Pad finger: 7 7 7 7
- The circuit layout is rectangle
- Pad Placement: 4 sides, 5 5 8 8
- The die area: 4436.7 x 2119.6

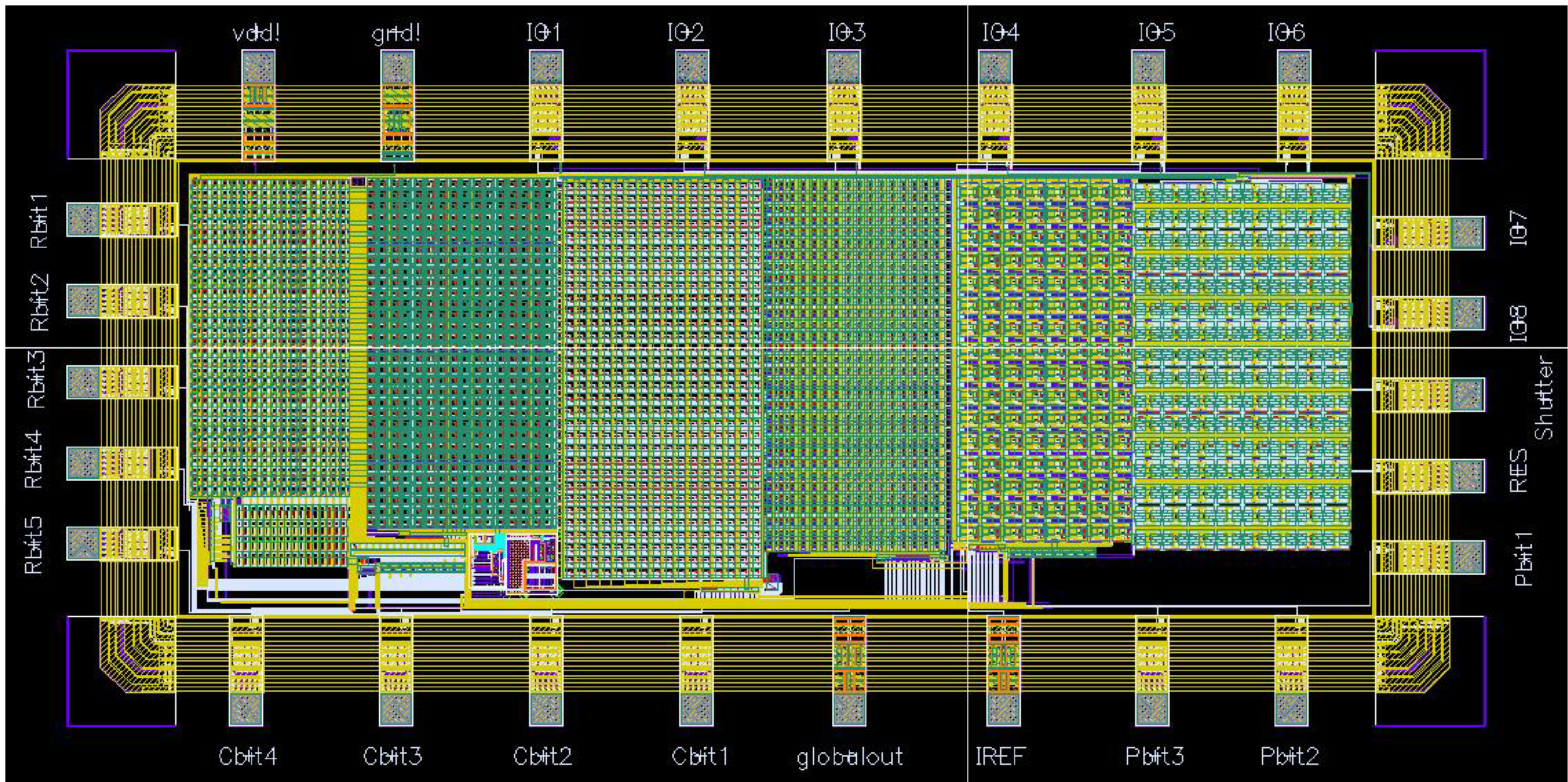
Pin and Pad

Pin Name	Pad Name
Rbit1/Rbit2/Rbit3/Rbit4/Rbit5	Rbit1/Rbit2/Rbit3/Rbit4/Rbit5
Pbit1/Pbit2/Pbit3	Pbit1/Pbit2/Pbit3
Cbit1/Cbit2/Cbit3/Cbit4	Cbit1/Cbit2/Cbit3/Cbit4
Shutter	Shutter
RES (reset)	RES
vdd!	vdd!
gnd!	gnd!
IREF	IREF
Vmode /Vconfigure /Vin0 /Vin1/Vin2 /Vin3 /Vin4 /Vin5	IO1/IO2/IO3/IO4/IO5/IO6/IO7/IO8
Output1/Output2/Output3/Output4/Output5/Output6/Output7/Output8	IO1/IO2/IO3/IO4/IO5/IO6/IO7/IO8

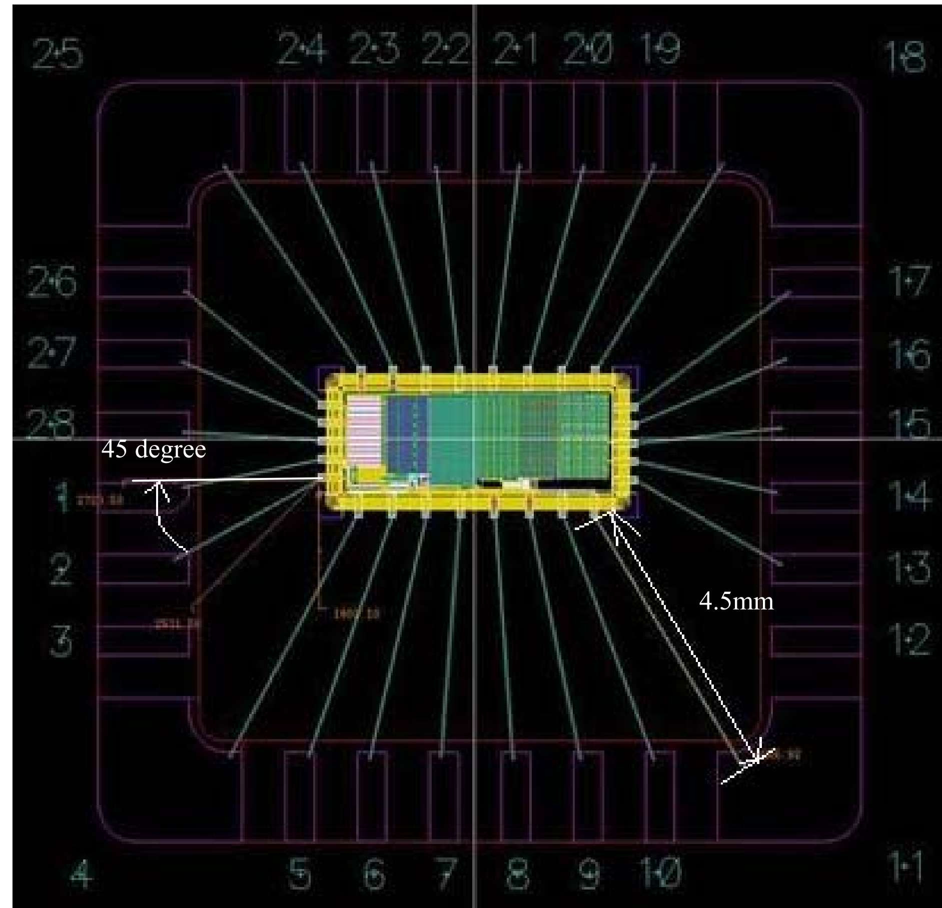
Pad Placement



Pad frame



Bonding Pattern



Layout Check

```
# errors  Violated Rules
       8  AML1/AML2 Minimum slot length = 30.0 Maximum slot length = 300.0 metal2
      64  AML1/AML2 Minimum slot length = 30.0 Maximum slot length = 300.0 metal3
       8  AMTS1 Maximum MTOP spacing when the width of one or both MTOP shapes is less than 10...
      20  AMW1 Fixed slot width = 3.0  metal3toolarge
       4  ERC Warning: Floating met1
      21  ERC Warning: Gates connected to VSS/GND
       7  ERC Warning: Latchup rule LAT3 distance s/d diff ngate subtap > 20
      22  ERC Warning: Latchup rule LAT3 distance s/d diff pgate welltap > 20
       7  ERC Warning: floating gate not connected to s/d, pad or resistor
      15  Figure Causing Multiple Stamped Connections.
       1  Figure Having Multiple Stamped Connections.
     521  INFO: hot nwell
       1  M1R1 Minimum density of MET1 area [%] = 30
       1  M2R1 Minimum density of MET2 area [%] = 30
       1  M3R1 Minimum density of MET3 area [%] = 30
       1  M4R1 Minimum density of MET4 area [%] = 30
       5  ODC3 Minimum NDIFF to HOT_NTUB spacing = 2.6
       1  POR1 Minimum density of POLY1 area [%] = 14
       8  VERT10_E1 Element Rule : NTUB enclosure of ntap = 0.45
       2  VERT10_P2 Element Rule : Base Ntub Perimeter/4 = 13.8
       2  VERT10_P3 Element Rule : Ptap Inside Perimeter/4 = 14.9
     720  Total errors found
```

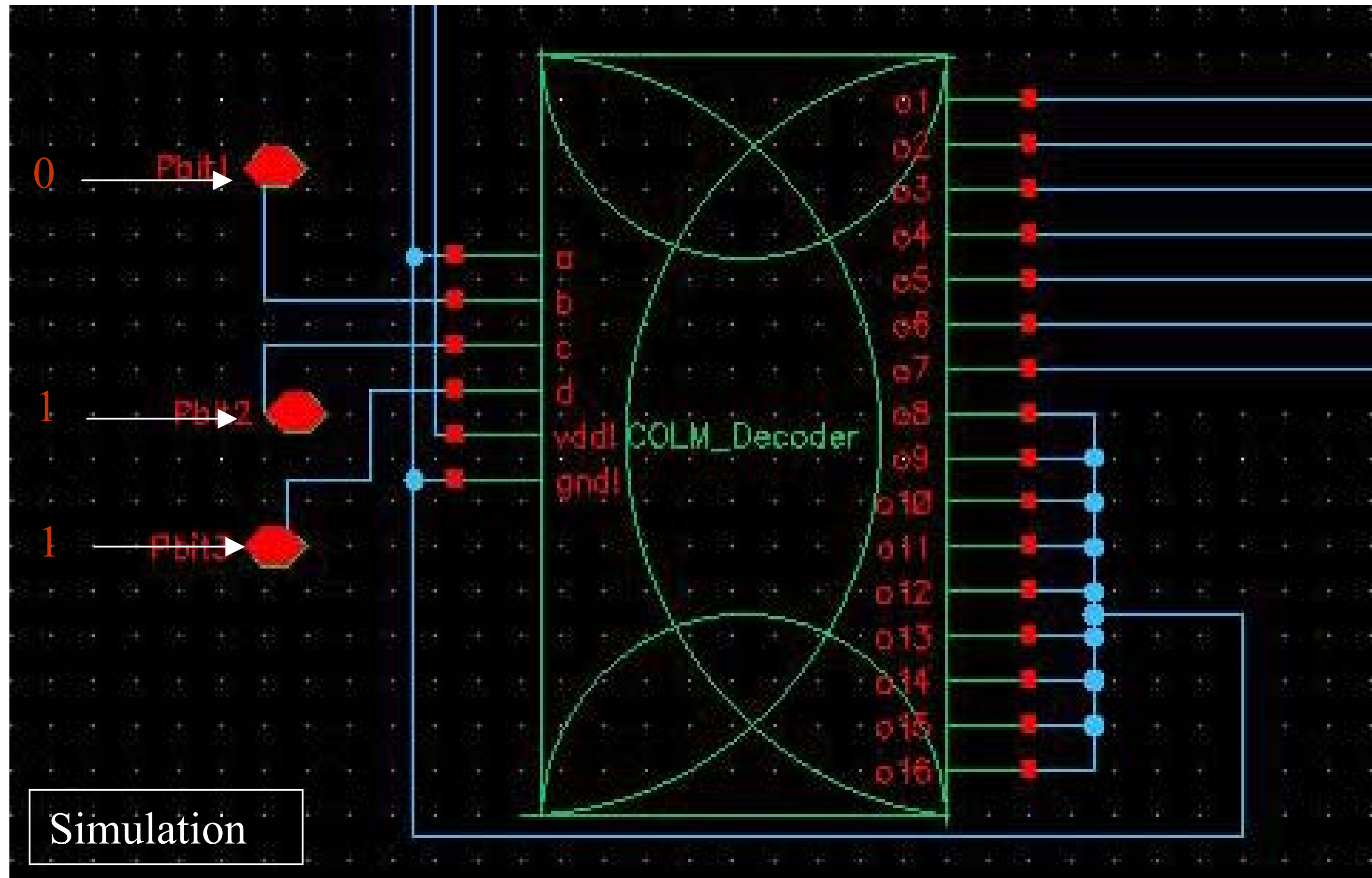
The hot nwell error from project 3, others from the standard amplifier and the standard corner used in the project.

Conclusion

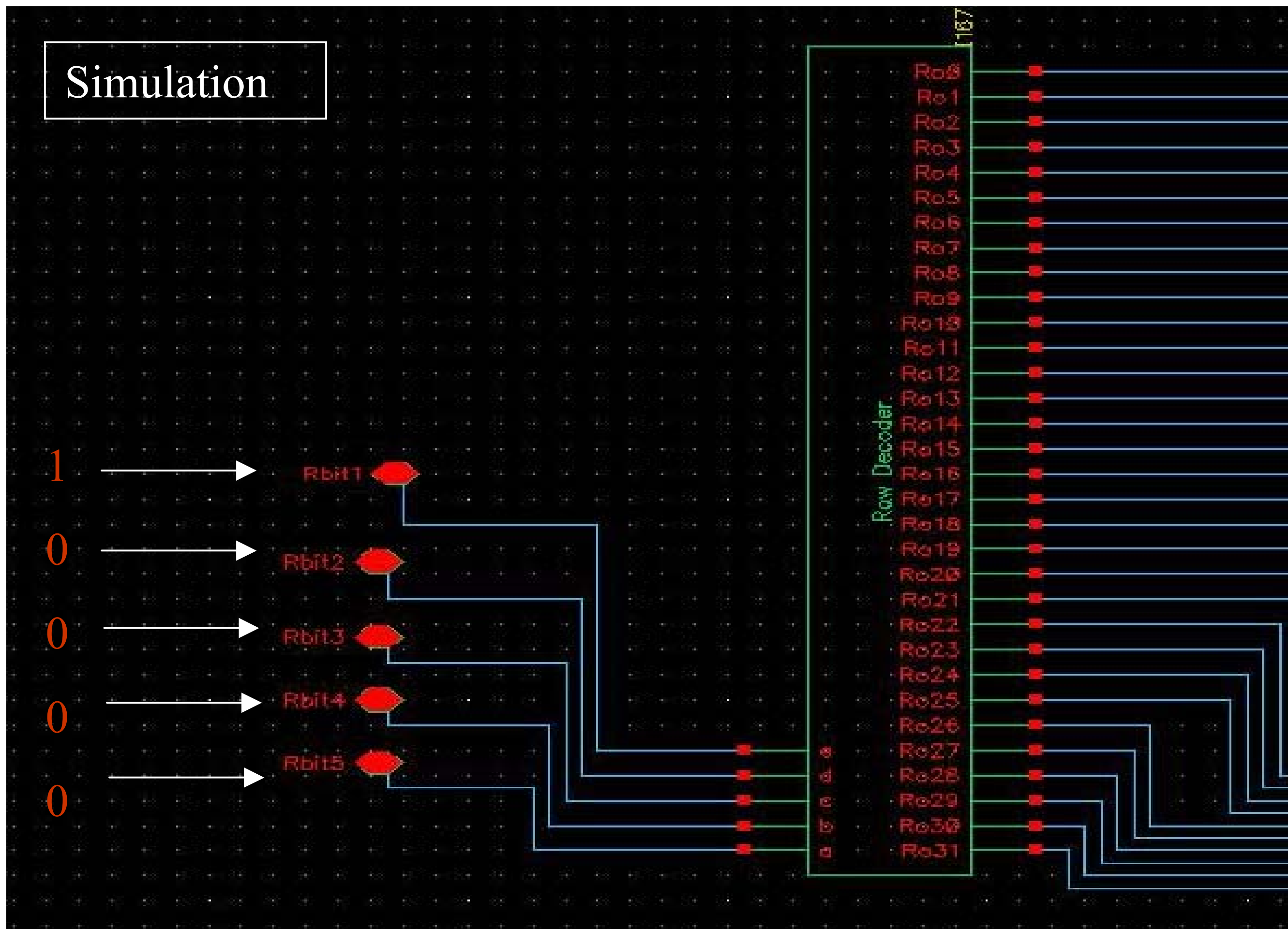
- The project is to place the I/O pads and global pads for the Multi-project Sensor Chip.
- It is no necessary in this project to separate digital ground and analog ground.
- In order to put the analog output as close as to the pad, reorganize the layout .
- Minimum the cost, project 5 and 8 share 8 bit I/O pads by using bidirectional pad.

Thank You for your attention!

Project Selection



Row Selection



Column Selection