RPTU
Institute of
Cognitive Integrated Sensor Systems
Department of Electrical and Computer Engineering

Semester Project in TESYS, 2023

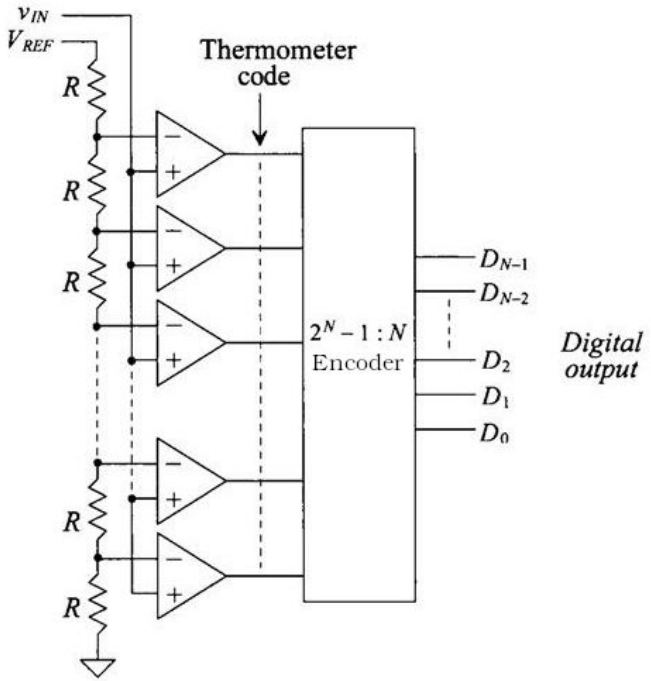
Front-To-Back Implementation of a 3-Bit Analog to Digital Converter in XFAB 0.35µm CMOS Technology

Furkan Aktas
Elias Biehl

Supervisor: Prof. Dr.-Ing. Andreas König

Contents

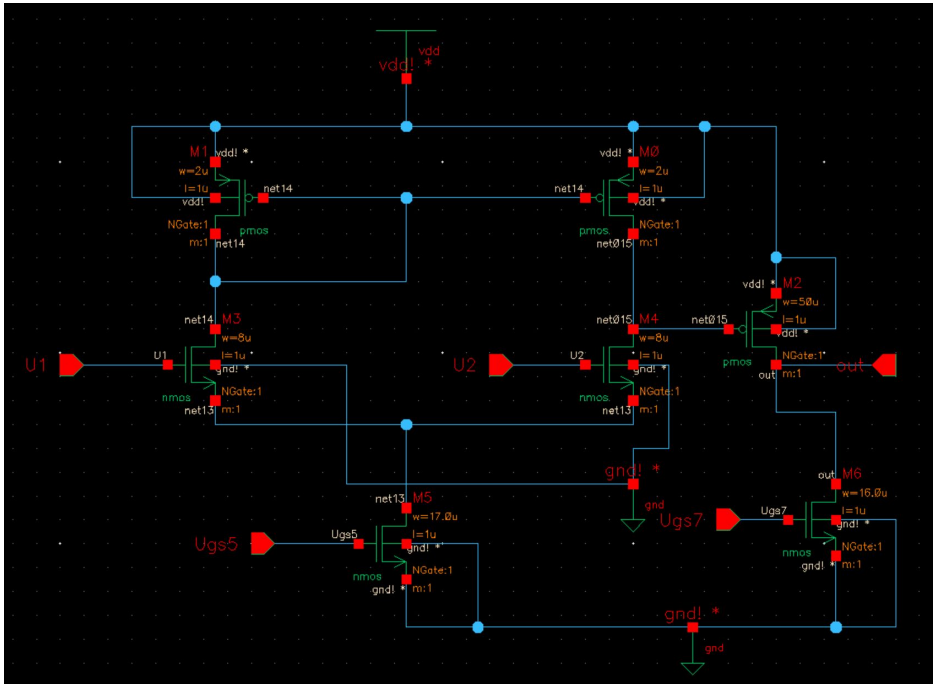
Parts of the project



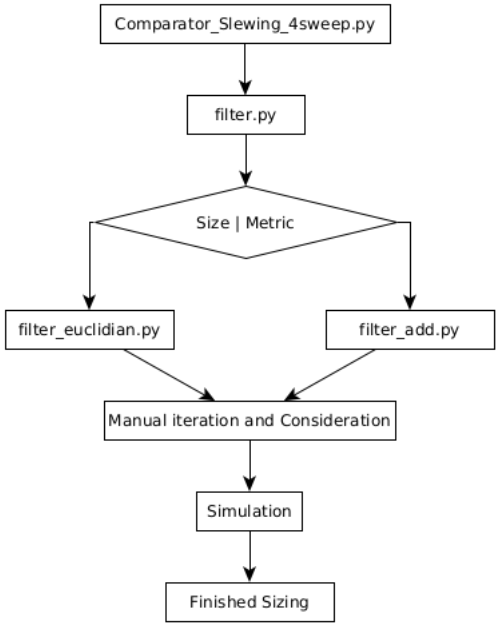
- 8 matched Resistors
- Thermometer Code Encoder
- 7 Comparators
- all Resistors have the same size due to simplification (R=4124.4 Ohm)

NMOS Comparator
Schematic

- Design after Allen/Holberg (7 transistor design)
  a. Design flow on next slide
- Prioritize in order:
  a. Wide CMR-range
  b. Size
  c. Speed
  d. Allowed tolerance (CI)



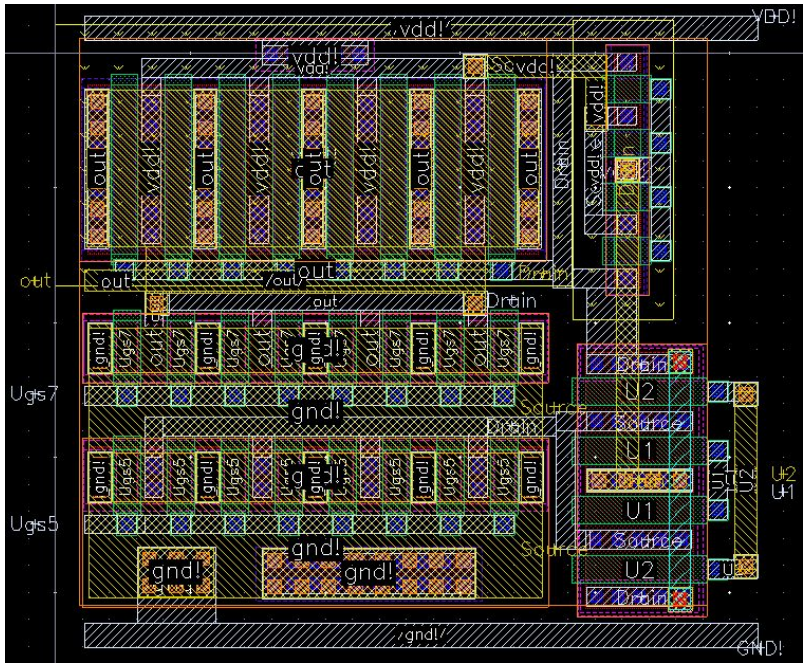
NMOS Comparator
Schematic

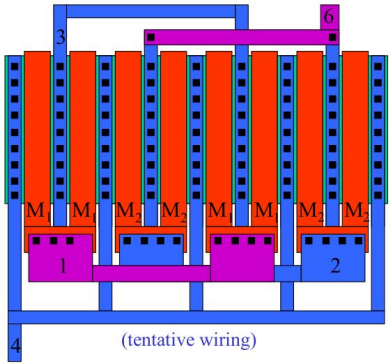


- Comparator_Slewing_4sweep.py:
  - 4-dimensional parameter sweep
- filter.py:
  - exclude corner sizes (100µm & 1µm)
- filter_euclidian.py:
  - select everything below certain top boundaries e.g. for P_{diss} or aspect ratios
- filter_add.py:
  - Include all solutions with a CMR greater than a given value
- Results hold size and Bias-Voltage

NMOS Comparator

Layout



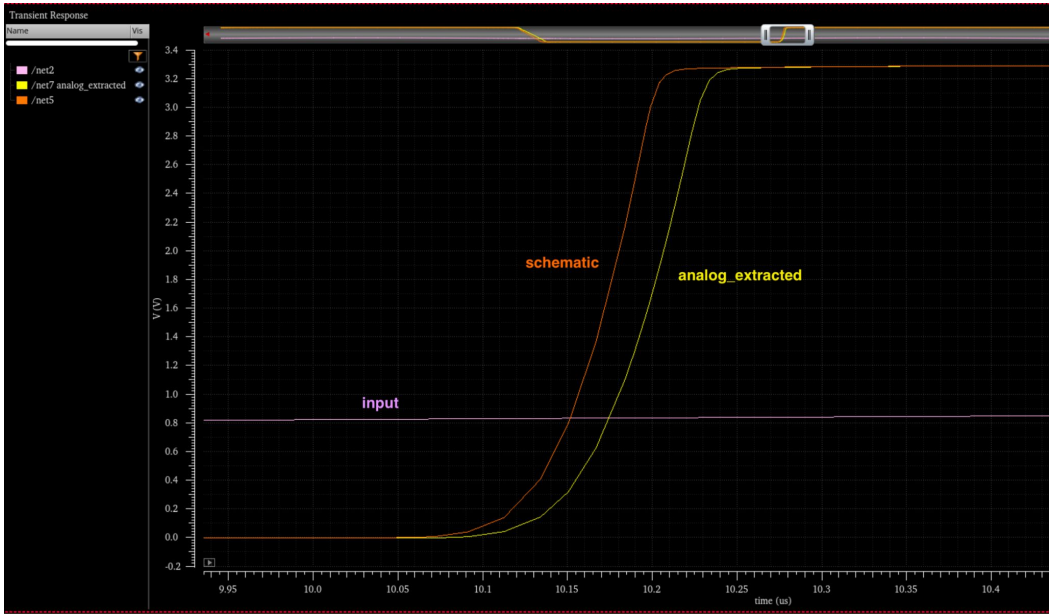


- Interdigitized “folded/matched” Transistors
- Allows matched positioning & sizing
- 23.4µm x 25.1µm

NMOS Comparator

Analog extracted

- Slightly bigger capacitance in layout resulting in slower speed
- Input Sine, 100kHz, 825mV, amp 100mV



NMOS Comparator

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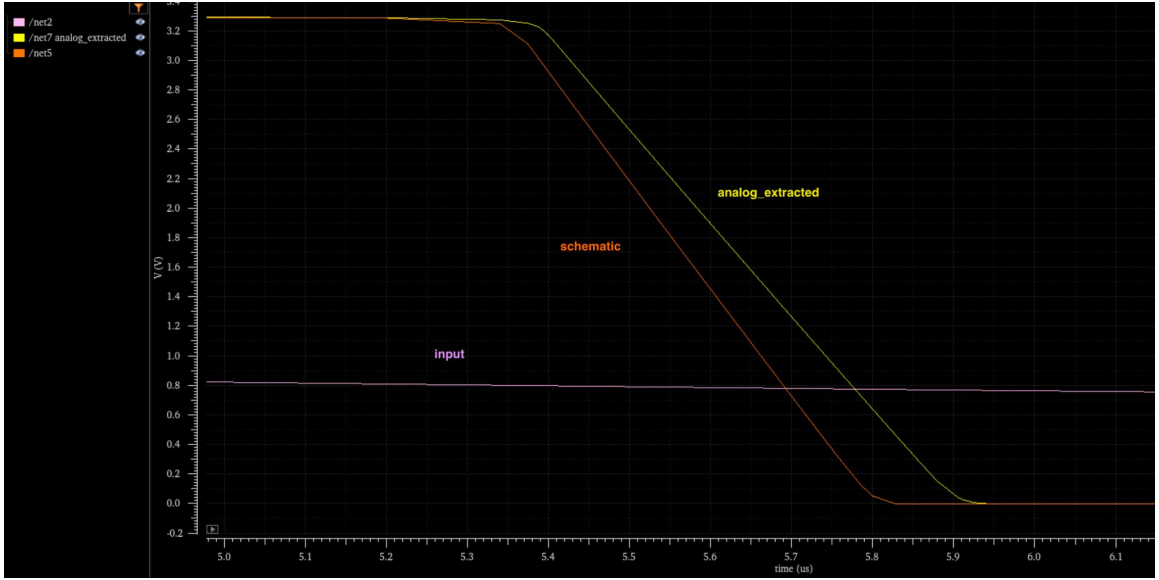
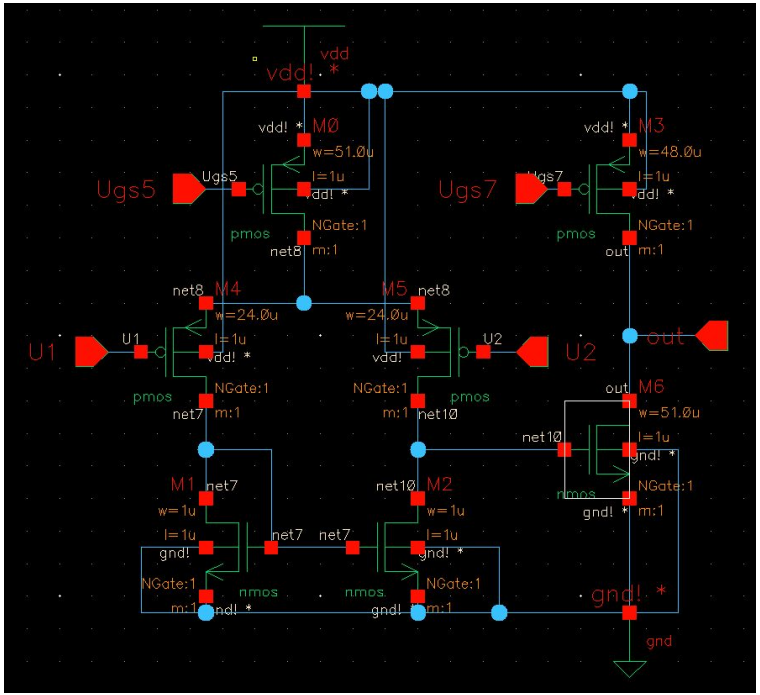
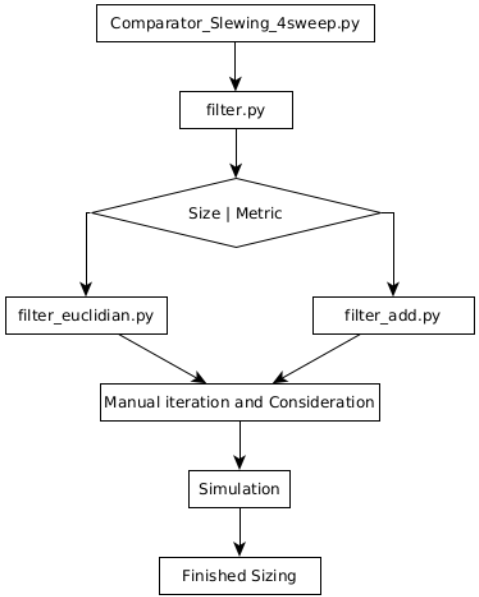


PMOS Comparator
Schematic



- Design after Allen/Holberg (7 transistor design)
  a. Design flow on next slide
- Prioritize in order:
  a. Wide CMR-range
  b. Size
  c. Speed
  d. Allowed tolerance (CI)

PMOS Comparator
Schematic



- Comparator_Slewing_4sweep_PMOS.py:
  - 4-dimensional parameter sweep
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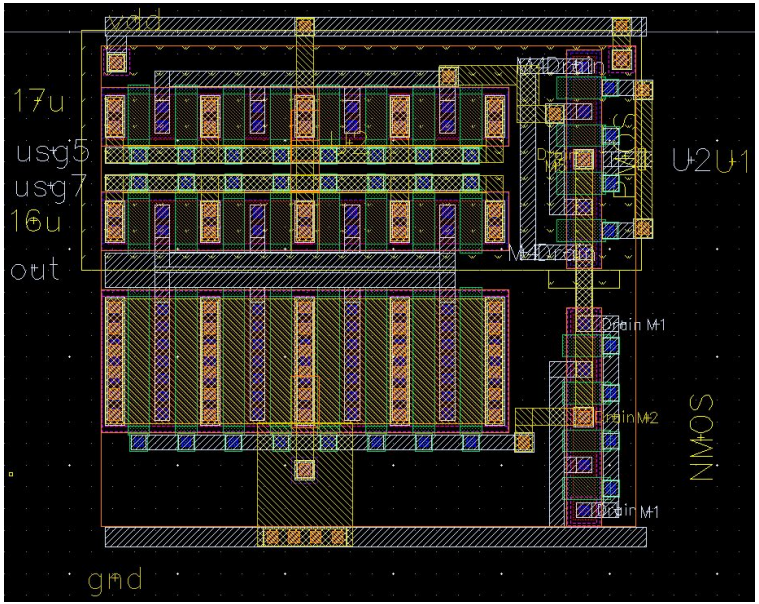
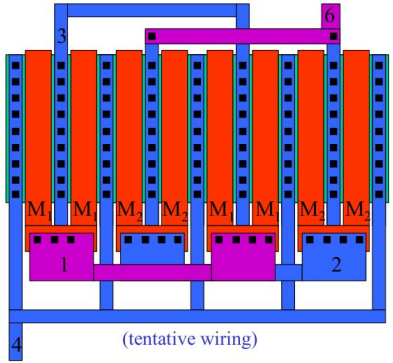
- filter_euclidian.py:
  - select everything below certain top boundaries e.g. for P_{diss} or aspect ratios
- filter_add.py:
  - Include all solutions with a CMR greater than a given value
- Results hold size
- Bias-Voltage needed to be extracted experimentally

PMOS Comparator

Layout

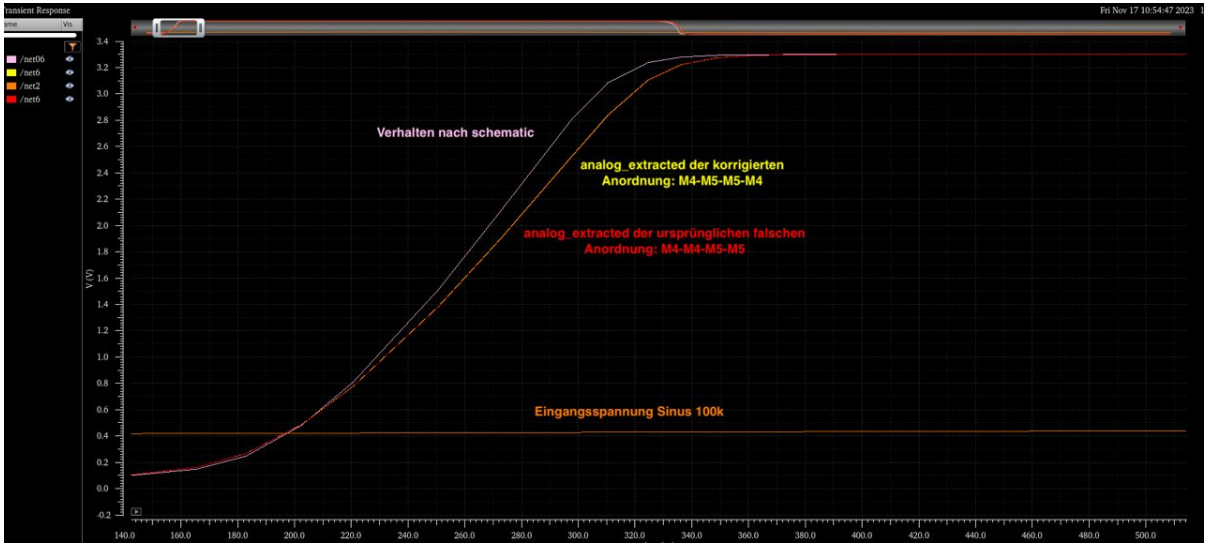




- Interdigitized “folded/matched” Transistors
- Allows matched positioning & sizing
- 24.475µm x 25.525µm

PMOS Comparator

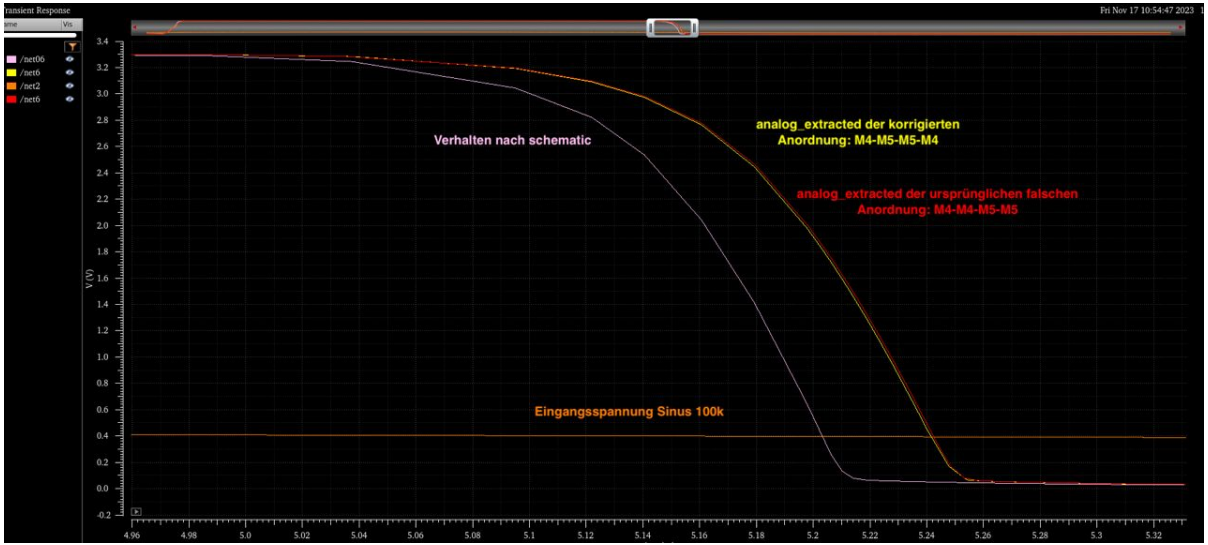
Analog extracted - RE & FE



- Slightly bigger capacitance in layout resulting in slower speed
- simulation with Sine, 100kHz, offset: 412.5mV, amp: 100mV

PMOS Comparator

Analog extracted - RE & FE



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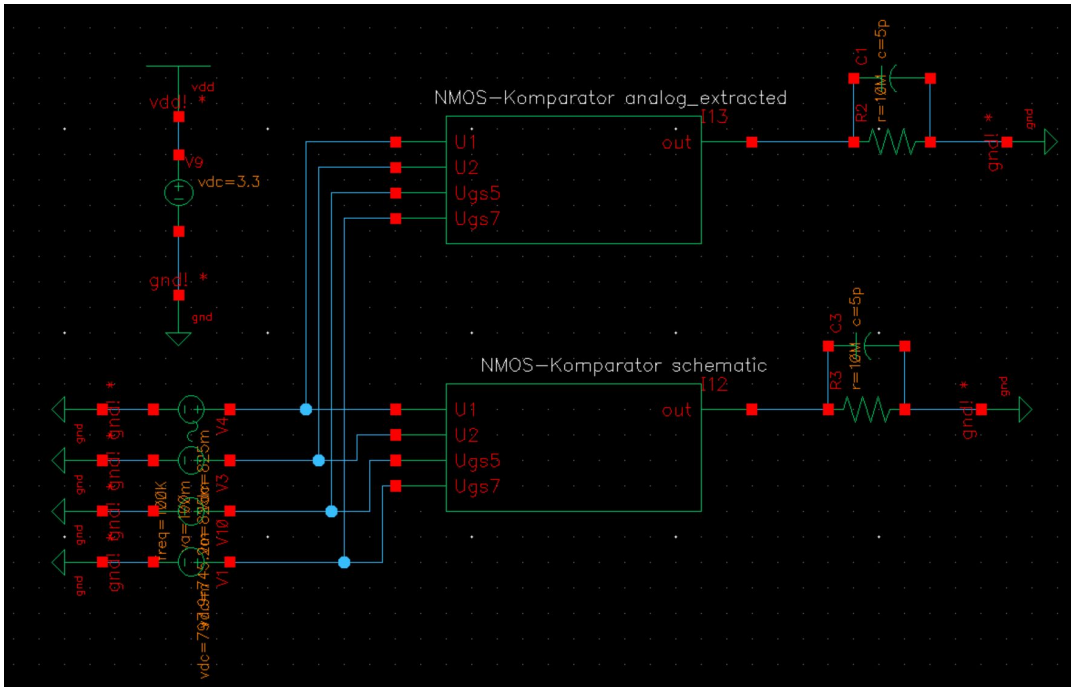
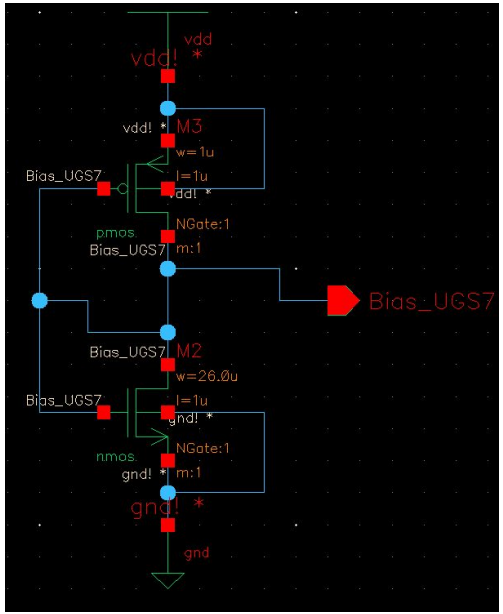
PMOS / NMOS Comparator

Testbench



BIAS Circuit for NMOS Comparator

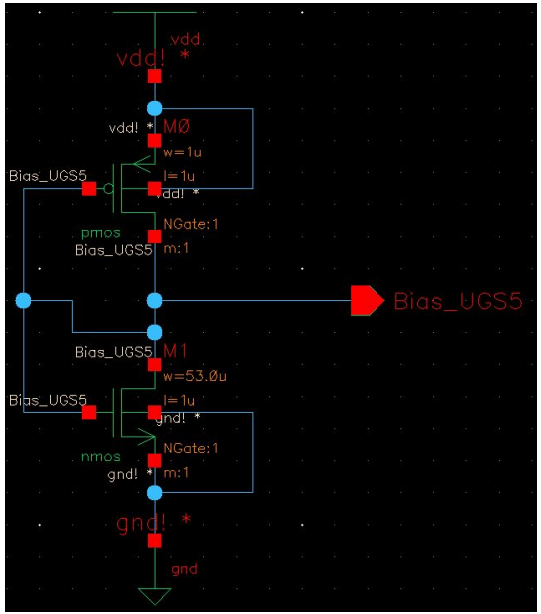
Schematic



- Simple voltage divider per MOST-Diode with near round transistor sizes
  - result with smallest rounding error used
- Analytical design for given wanted voltage
  - Slides 5-25/26
  - per simple python calculation scripts:
    - Bias-Circuit-PMOS-sweep_usg5.py
    - Bias-Circuit-PMOS-sweep_usg7.py
  - Sweep current through circuit
  - Current/Area tradeoff

BIAS Circuit for NMOS Comparator

Schematic



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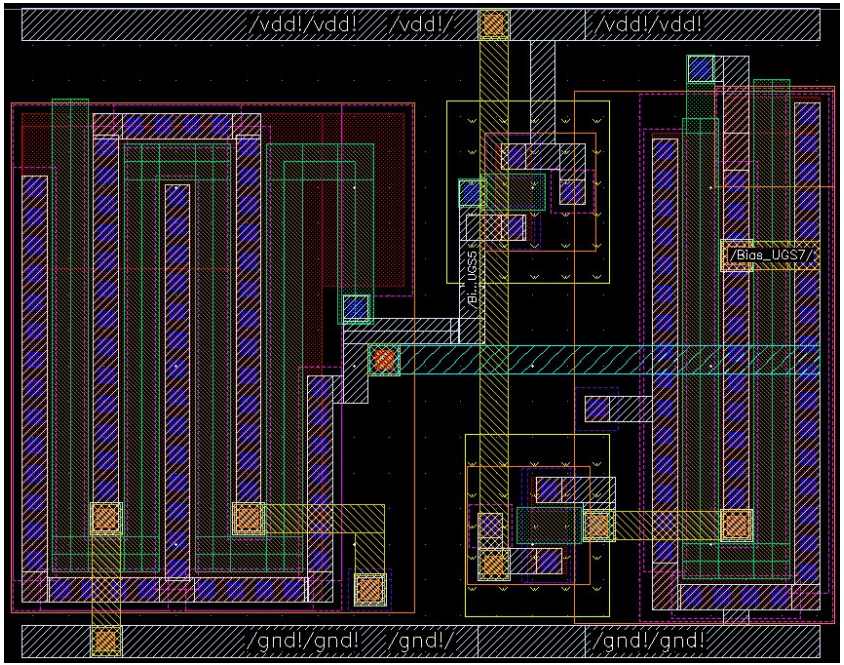
BIAS Circuit for NMOS Comparator

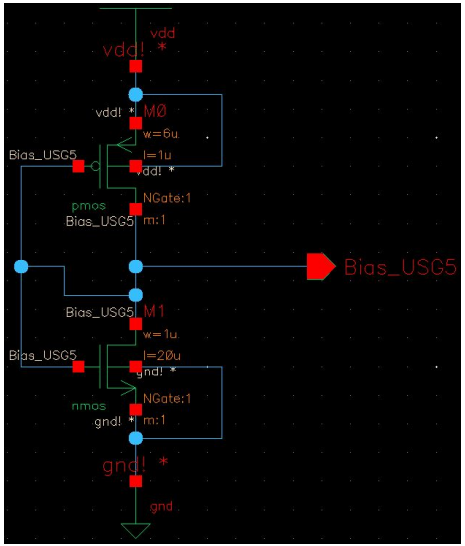
Layout



- Lengths not easy matchable (need to go through DRC & LVS) for very long
- Meanderized transistors to save space for very long transistors
- Both bias circuits into one layout (size matching in layout needed)
- 18.2µm x 23.075µm

BIAS Circuit for PMOS Comparator

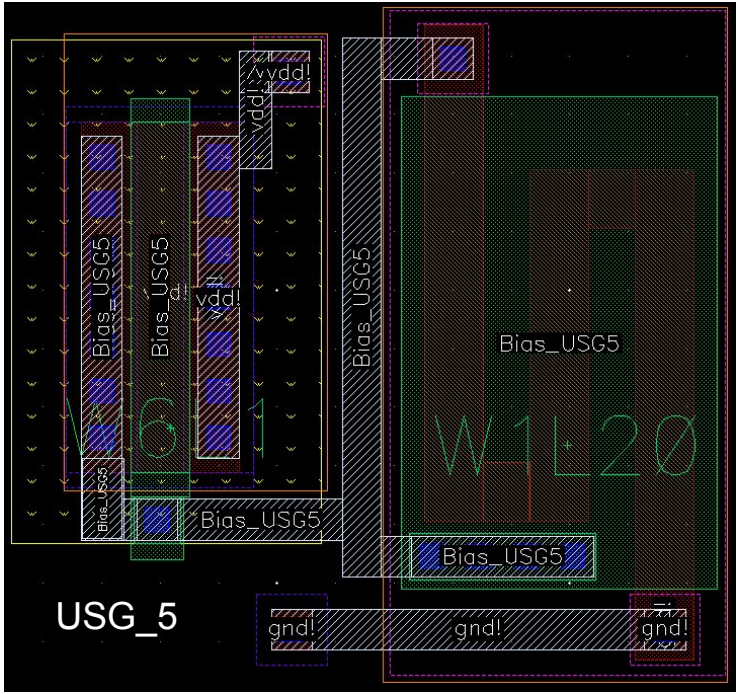
Schematic



- Simple voltage divider per MOST-Diode with near round transistor sizes
  - result with smallest rounding error used
- Analytical design for given wanted voltage
  - Slides 5-25/26
  - per simple python calculation scripts
  - Sweep current through circuit
  - Current/Area tradeoff
- No combined layout was easy to implement

BIAS Circuit (U_{SG5}) for PMOS Comparator

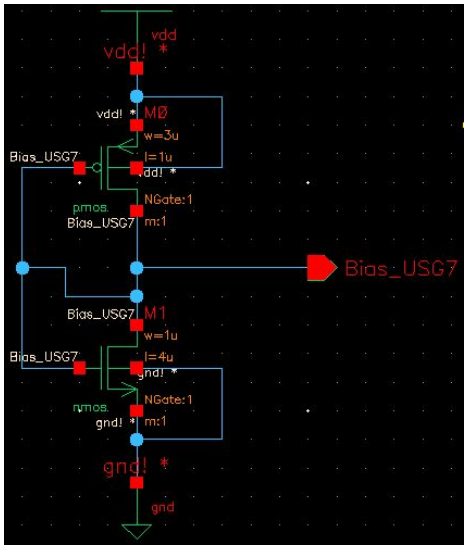
Layout



- Lengths not easy matchable (need to go through DRC & LVS) for ultra long
- meanderized transistors to save space for very long transistors
- Both bias circuits into one layout (size matching in layout needed)
- 12.25µm x 11.525µm (first)
- 14.5µm x 6.15µm (second)

BIAS Circuit for PMOS Comparator

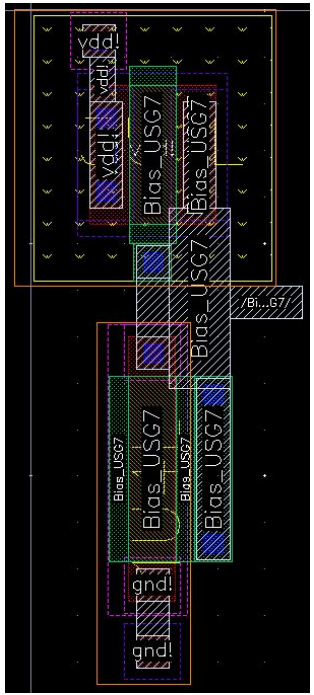
Schematic



- Simple voltage divider per MOST-Diode with near round transistor sizes
  - result with smallest rounding error used
- Analytical design for given wanted voltage
  - Slides 5-25/26
  - per simple python calculation scripts
  - Sweep current through circuit
  - Current/Area tradeoff
- No combined layout was easy to implement

BIAS Circuit (U_{SG7}) for PMOS Comparator

Layout



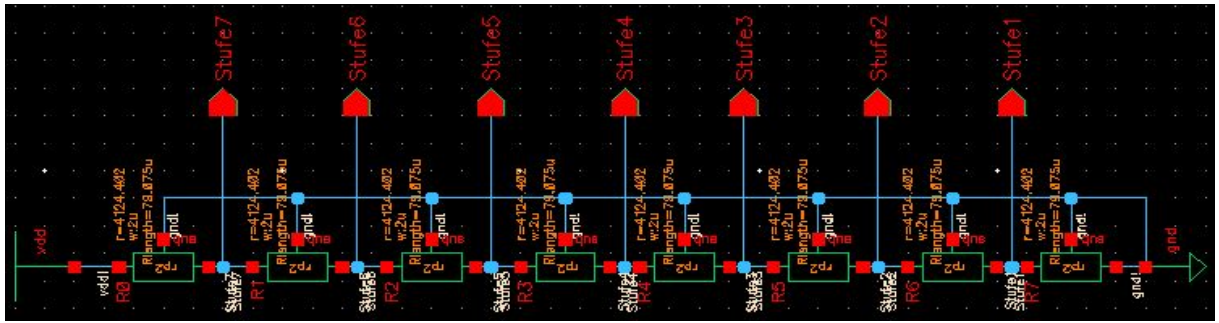
USG_7

- Lengths not easy matchable (need to go through DRC & LVS) for ultra long
- Both bias circuits into one layout (size matching in layout needed)
- 12.25µm x 11.525µm (first)
- 14.5µm x 6.15µm (second)

Resistor Chain

Schematic

- Current limit set to 100µA
- For Supply voltage of 3.3V:
  - 3.3V / 100µA = 33.3kΩ
- Used High-Res Poly2 Instances from PrimLib
- due to simplification: all resistors have the same value
- Same step size across full range -> goal was to simplify layout design (homogenous structure)

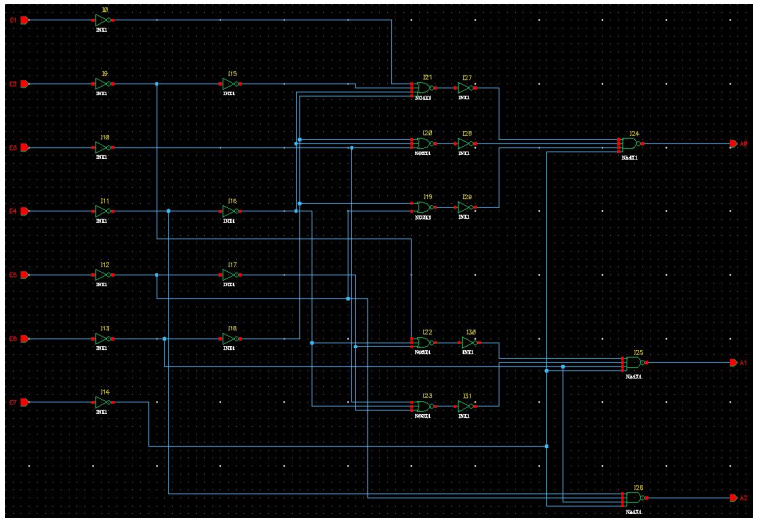


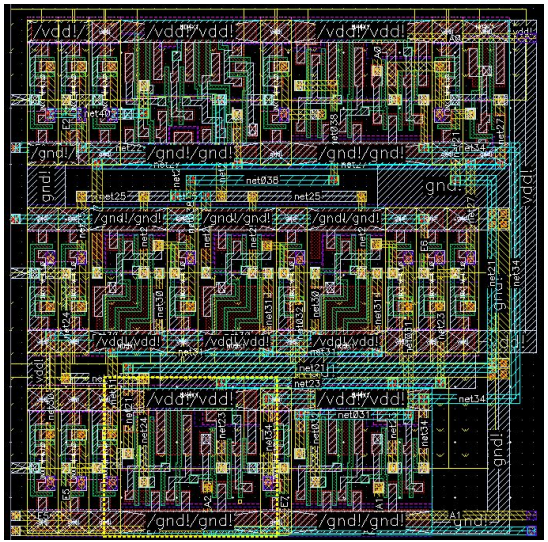
Resistor Chain

Layout

- Layout generated from cells of PrimLib
- Connection of strips via MET1
- Contacting through MET1

Encoder

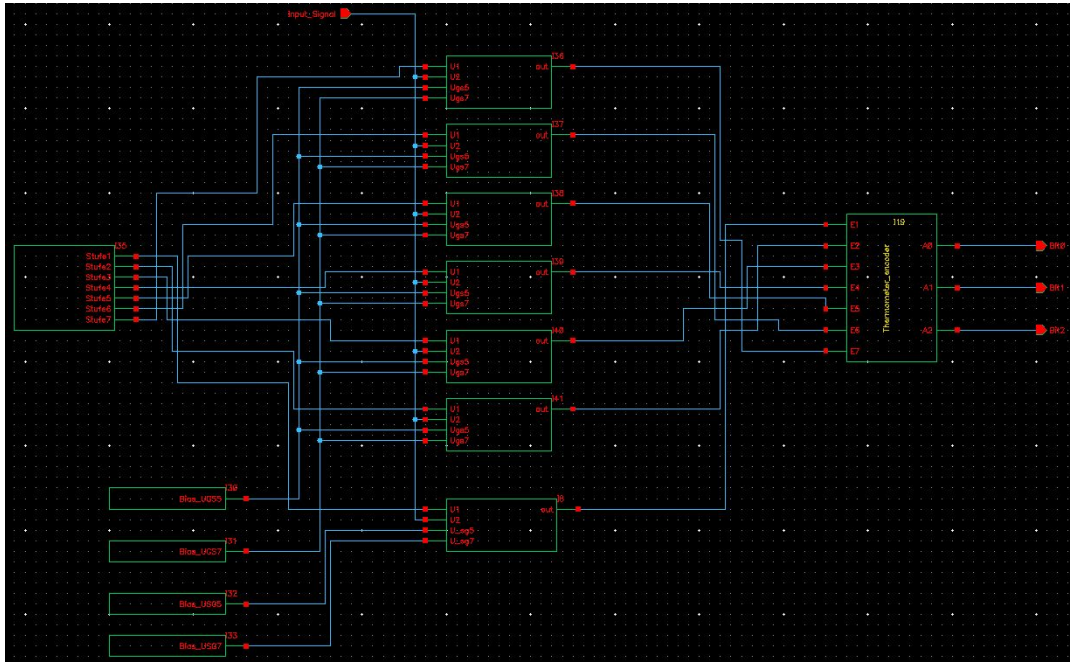




- Schematic & Layout provided from Lukas Birkenmeier for MelLab

Top level design & wiring

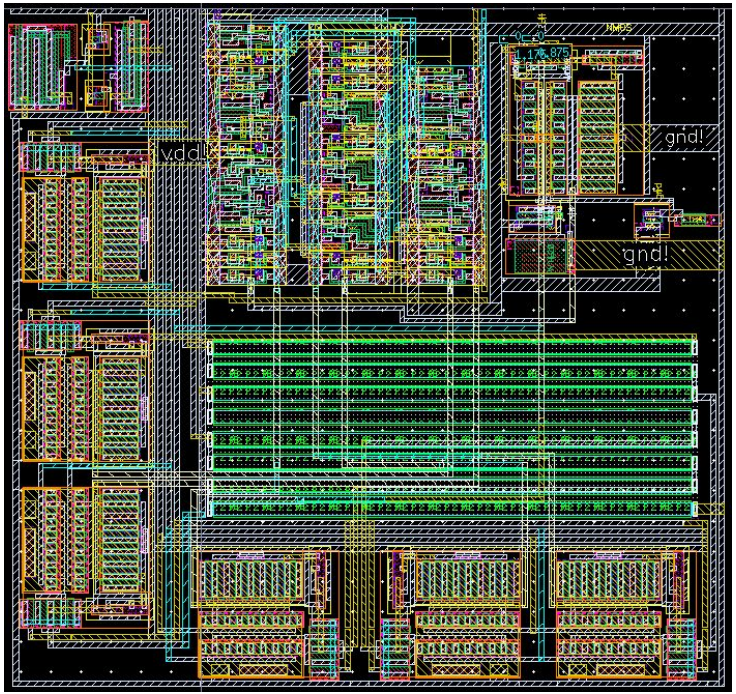
Schematic



- 4 Bias Cells
- Resistor Chain (8)
- Encoder
- 7 Comparators

Top level design & wiring

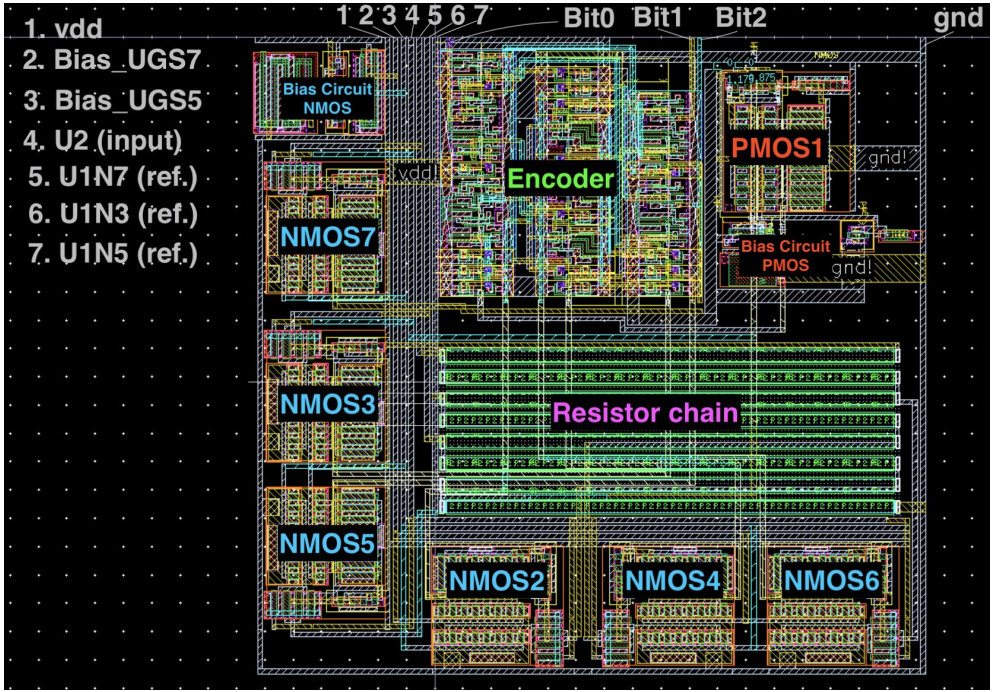
Layout



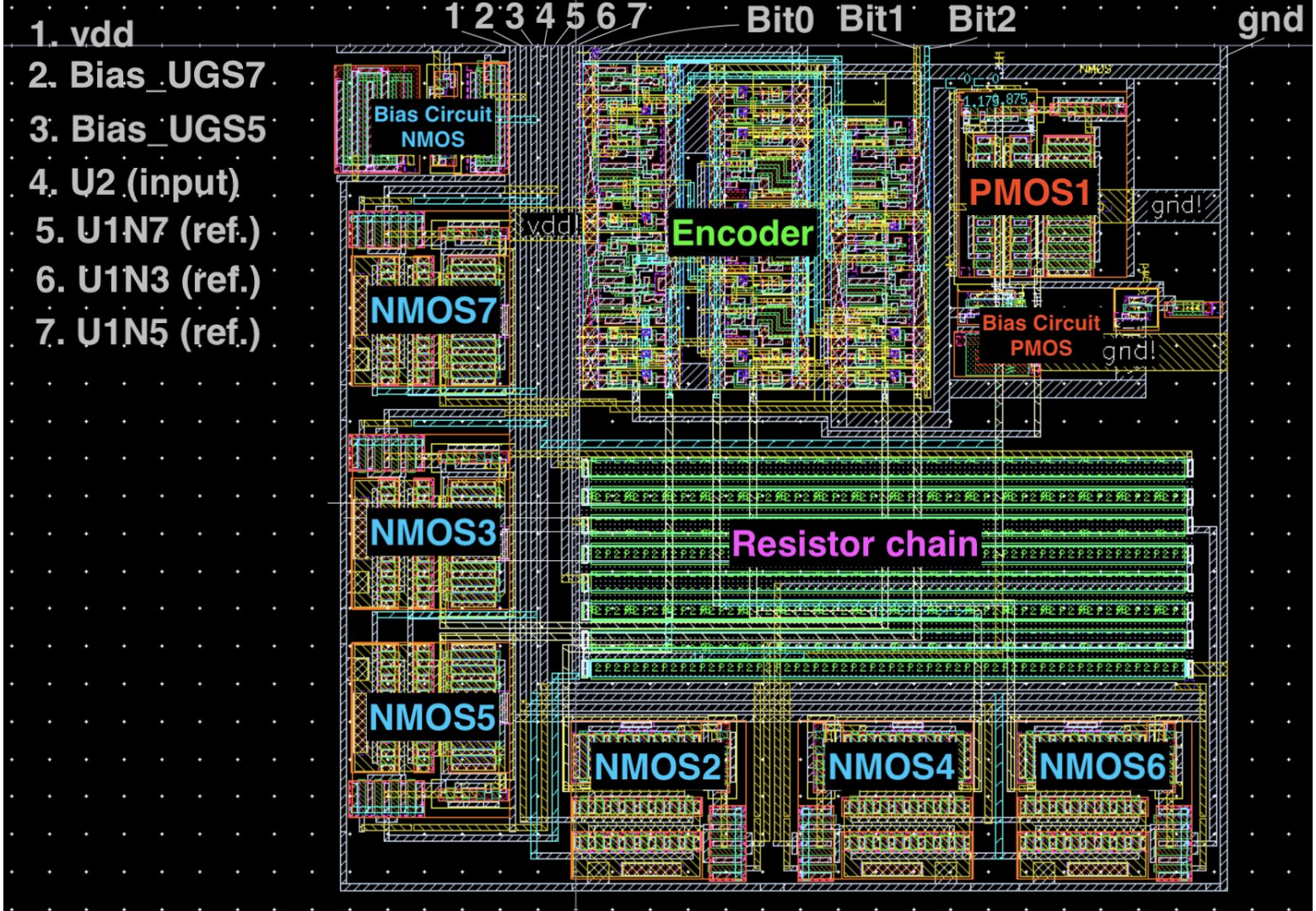
- Main Voltage “Bus” to distribute voltages
- Floorplan pre-planned in painting software
- Minimal Area and 1:1 Aspect Ratio prioritised
- Mirrored positioning of Comparators for less area
  - esp. for Bias-voltage distribution
- 112.475µm x 118µm

Top level design & wiring

Layout

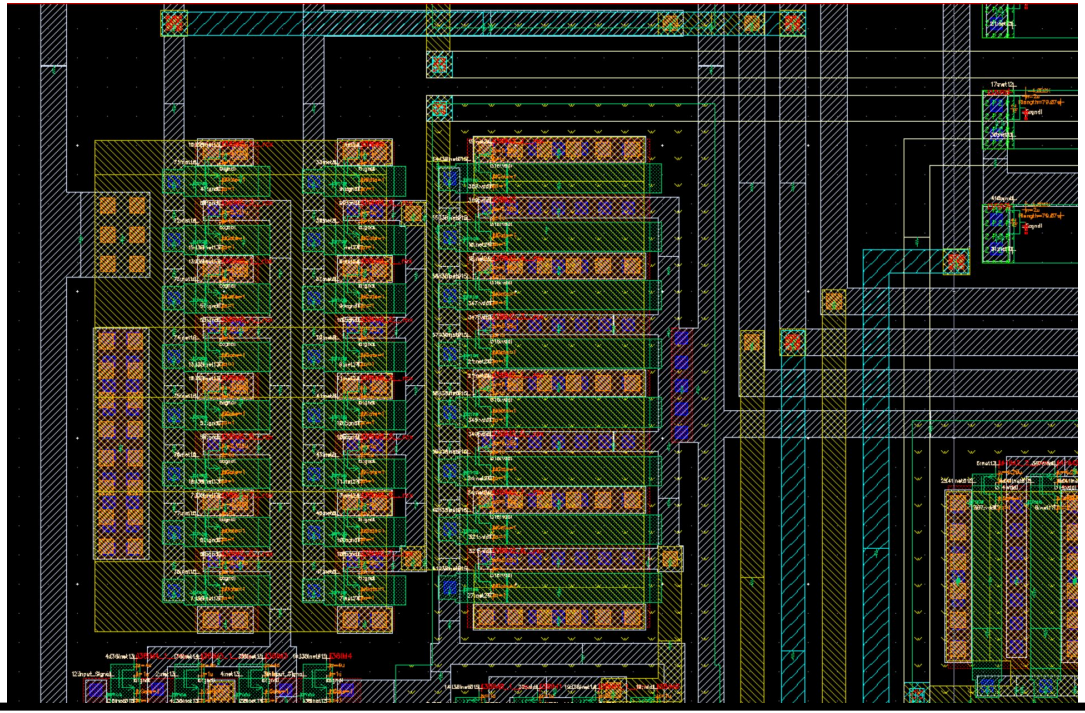


U1N7, U1N3, U1N5 not input/outputs, just internal connections that can be accessed


1. vdd
2. Bias_UGS7
3. Bias_UGS5
4. U2 (input)
5. U1N7 (ref.)
6. U1N3 (ref.)
7. U1N5 (ref.)
1 2 3 4 5 6 7
Bit0
Bit1
Bit2
gnd
Bias Circuit NMOS
vdd!
Encoder
PMOS1
gnd!
NMOS7
Bias Circuit PMOS
gnd!
NMOS3
Resistor chain
NMOS5
NMOS2
NMOS4
NMOS6

Analog extracted, DRC and LVS

Layout



Analog extracted, DRC and LVS

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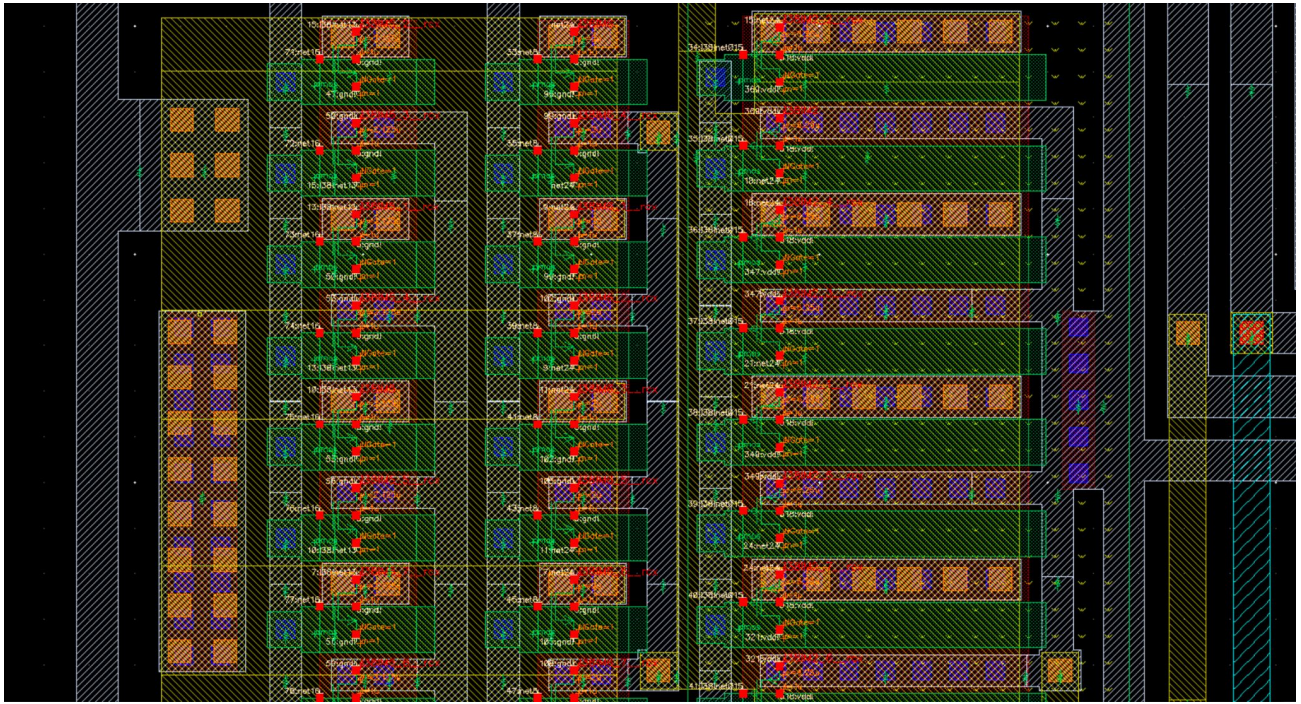

Analog extracted, DRC and LVS

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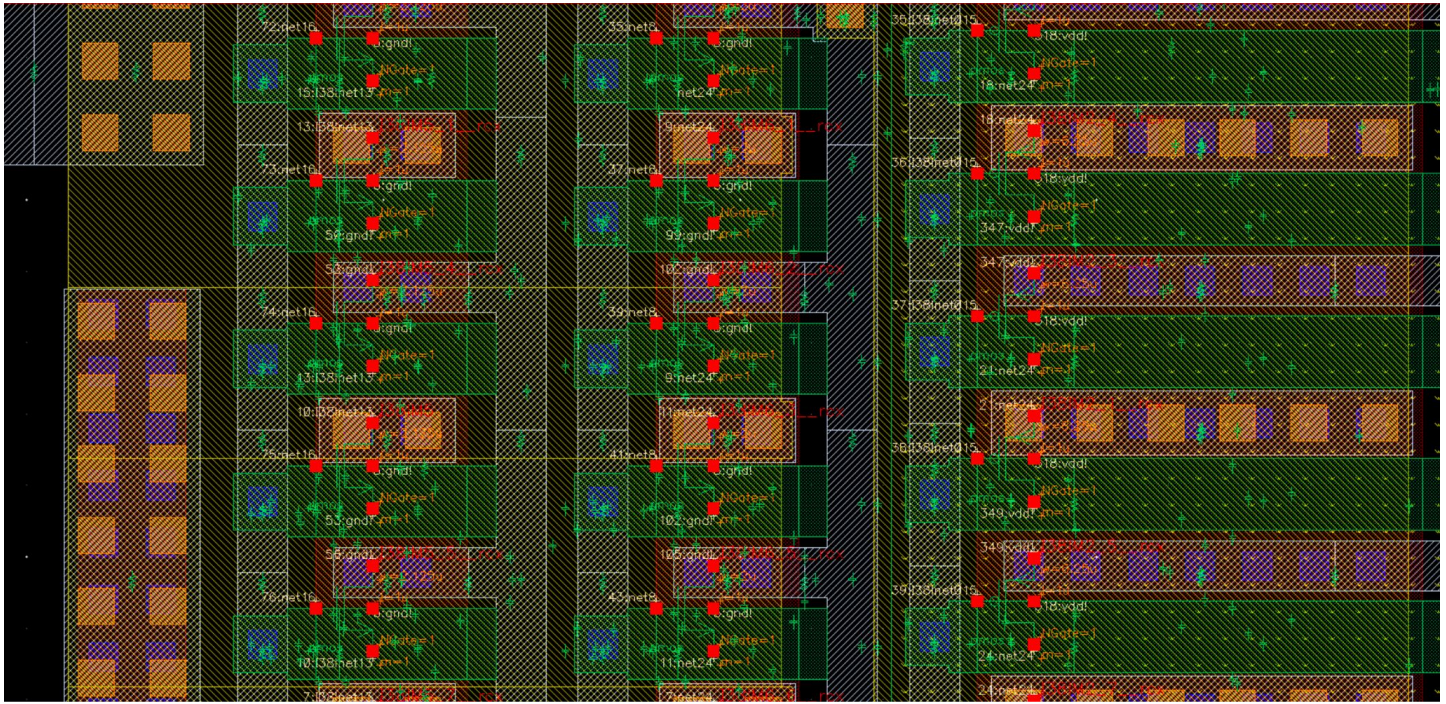

Analog extracted, DRC and LVS

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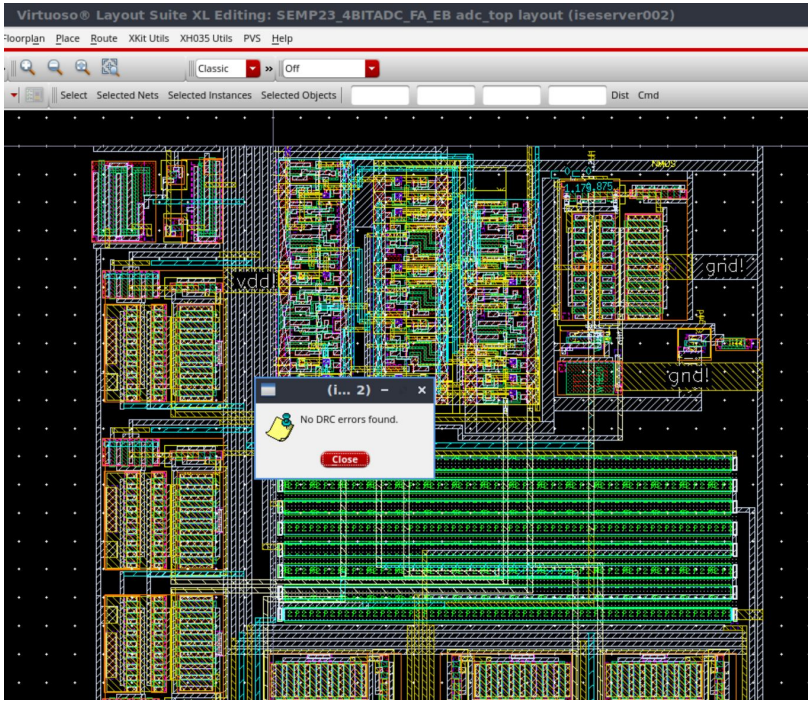
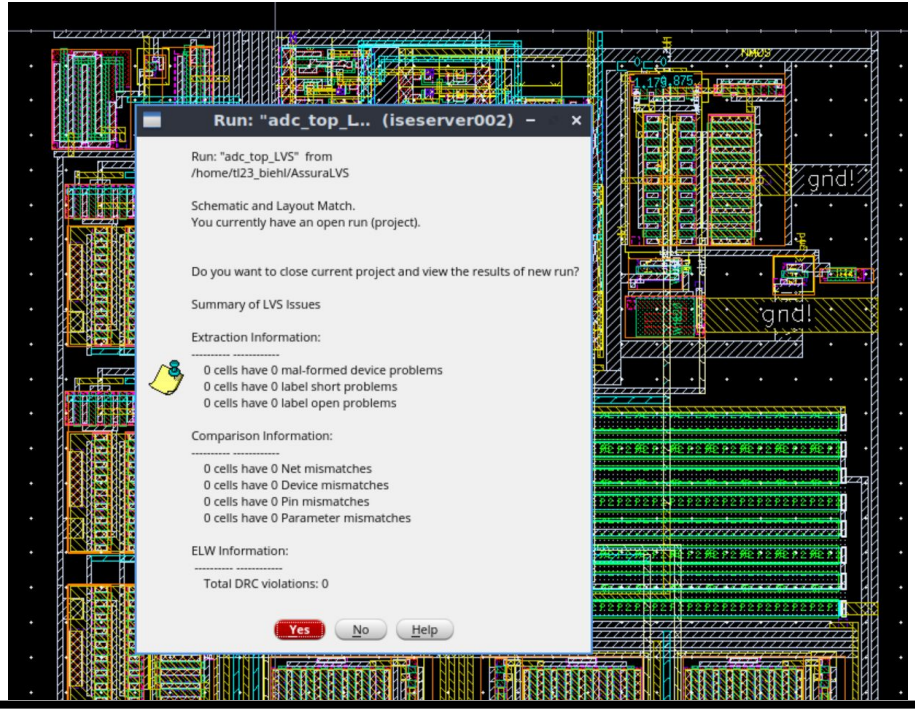
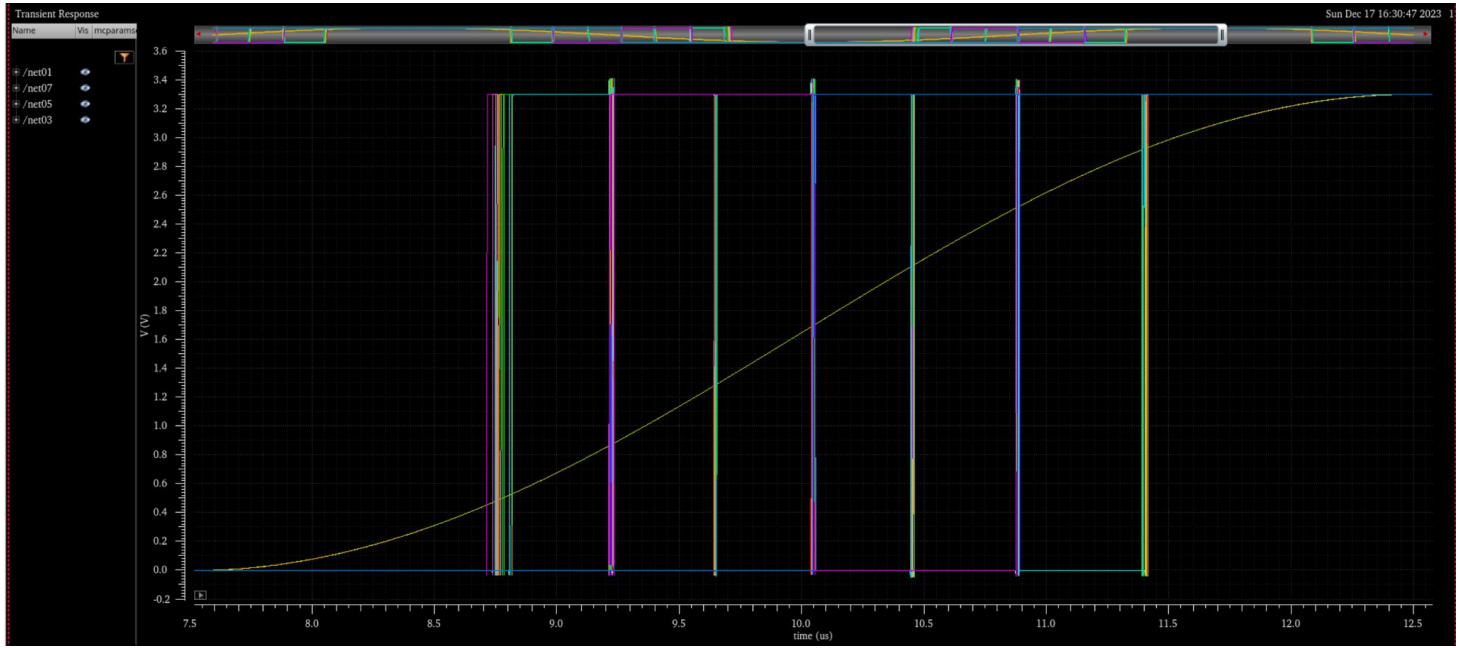


Analog extracted, DRC and LVS

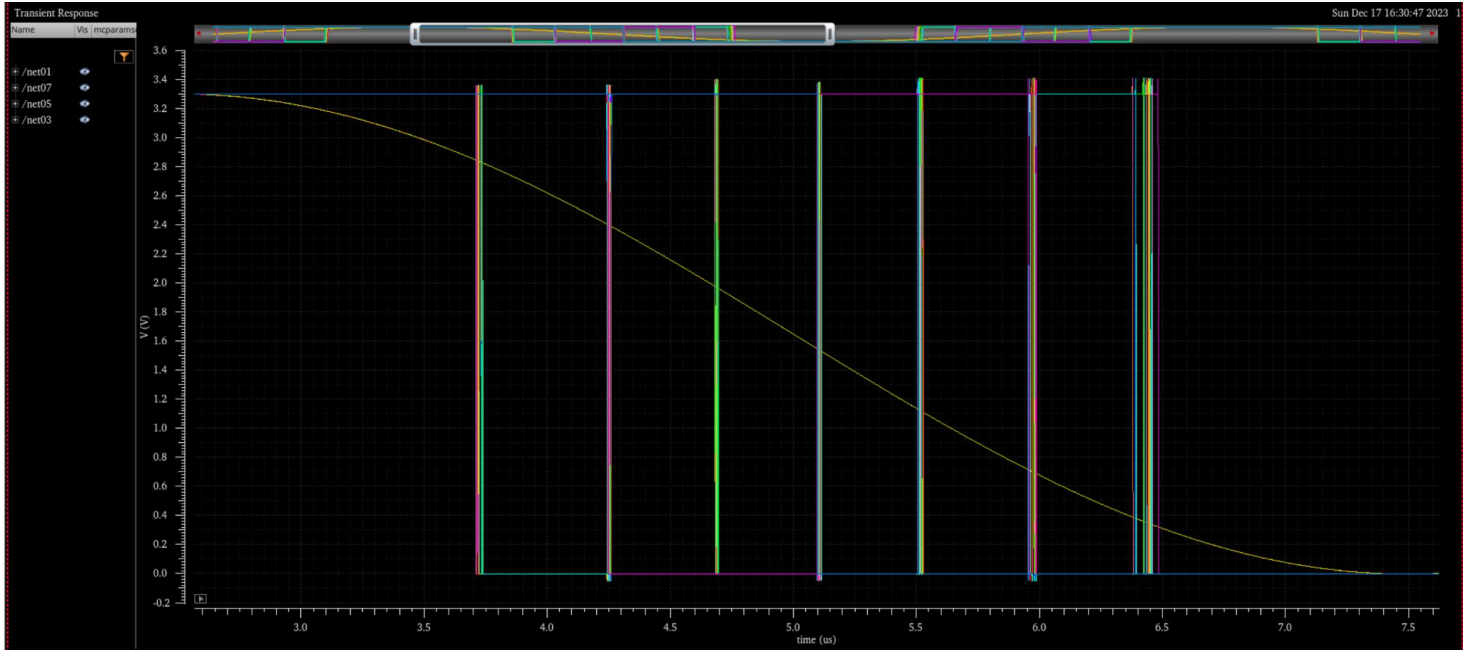
Layout



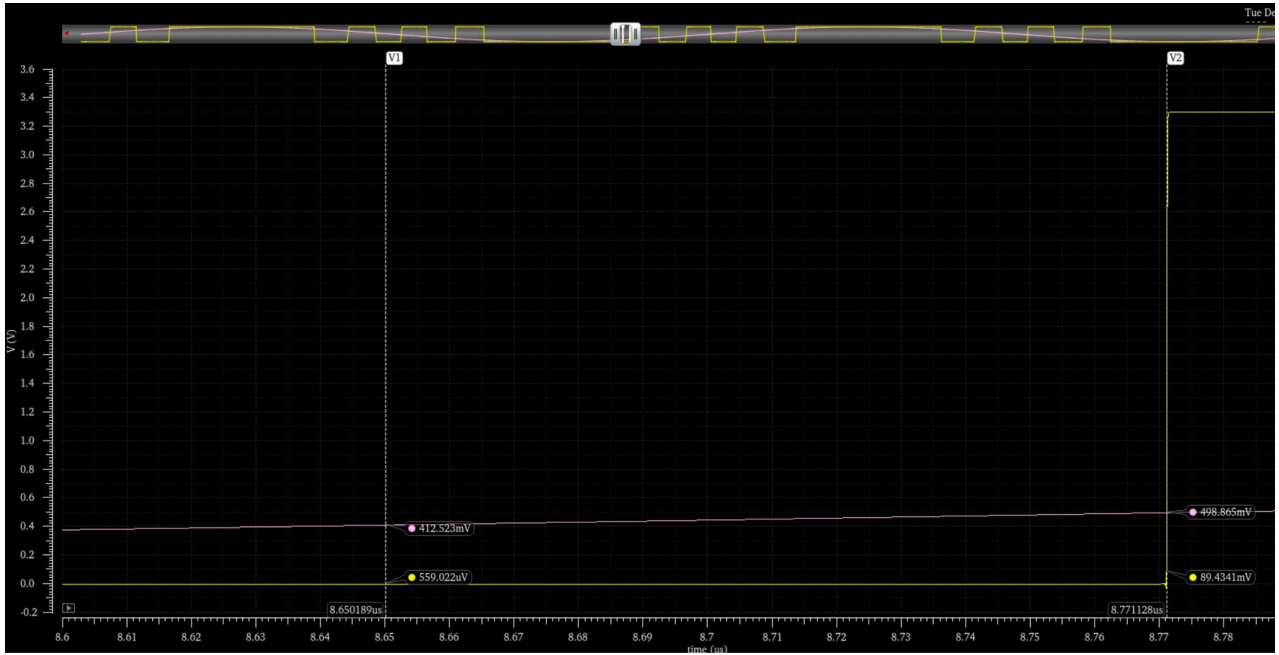
Monte Carlo (Rising Edge)



Monte Carlo (Falling Edge)



Conclusion

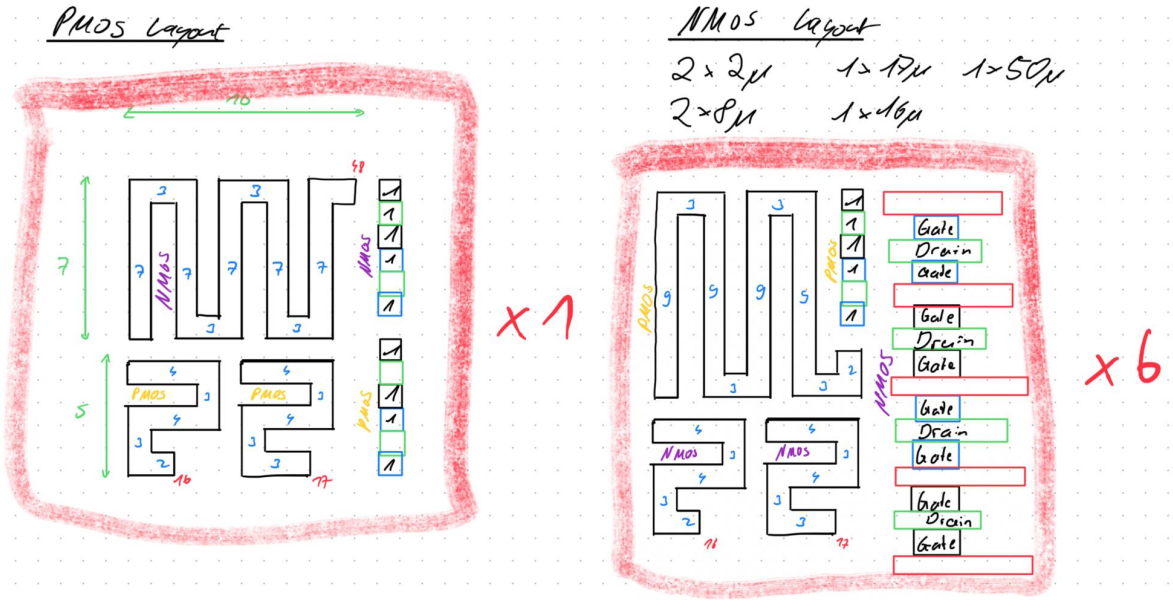


- Theoretical/Simulated max. Sample Rate: 8.3MS/s

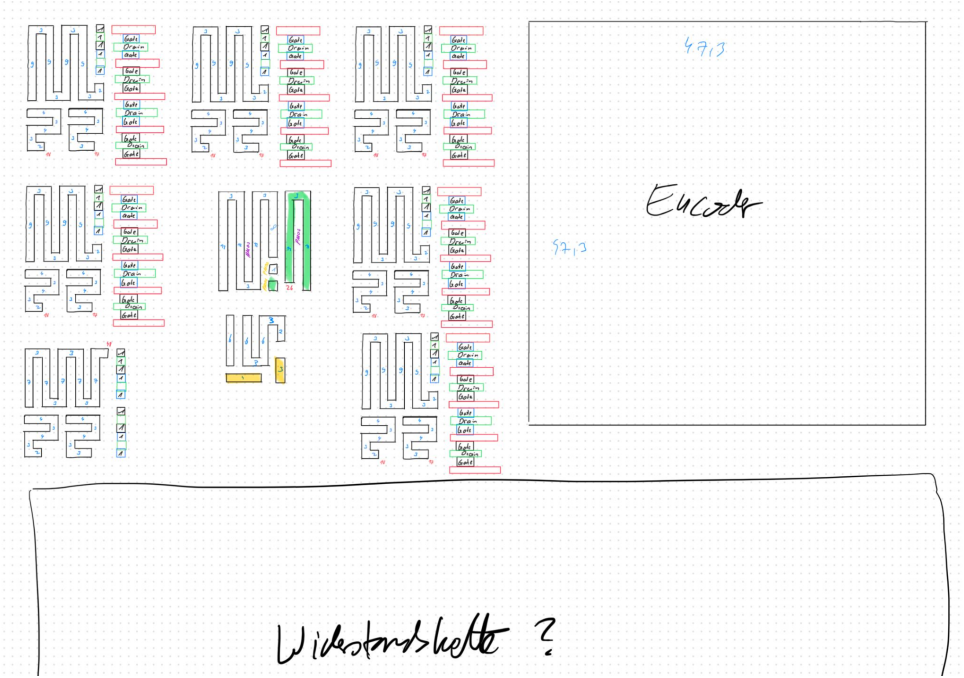
Conclusion

- Slightly slower and wider spread vs. schematic
- Better Matching & Layout possible
  - especially PMOS comparator
  - also NMOS2 comparator
- Static Power: 1.41735 mW
- Total area: $1.327*10^{-8}$ m^2 = 0.01327 mm^2

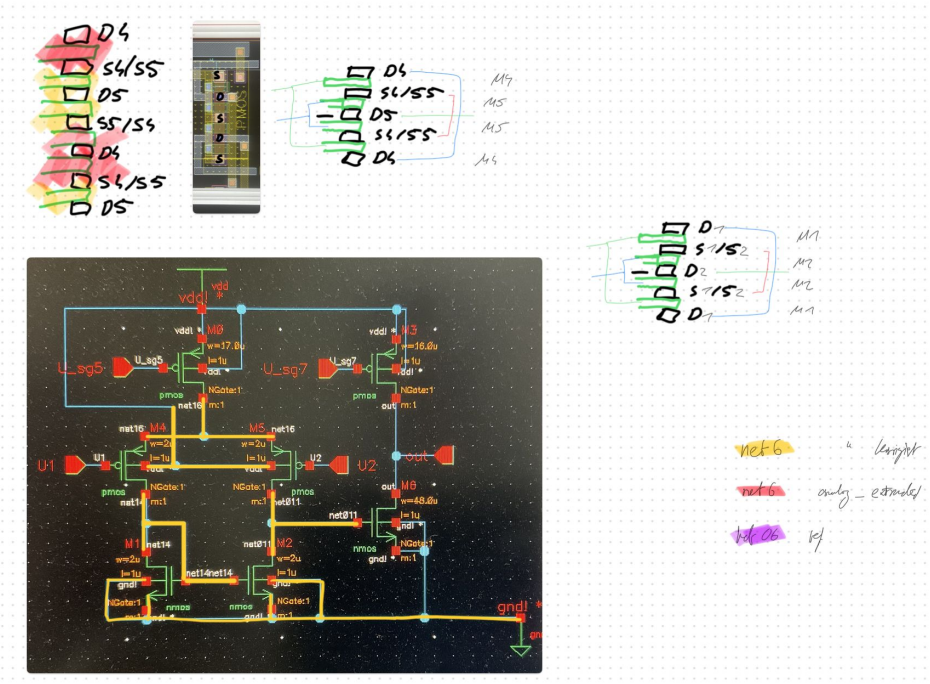
Planning in Freeform



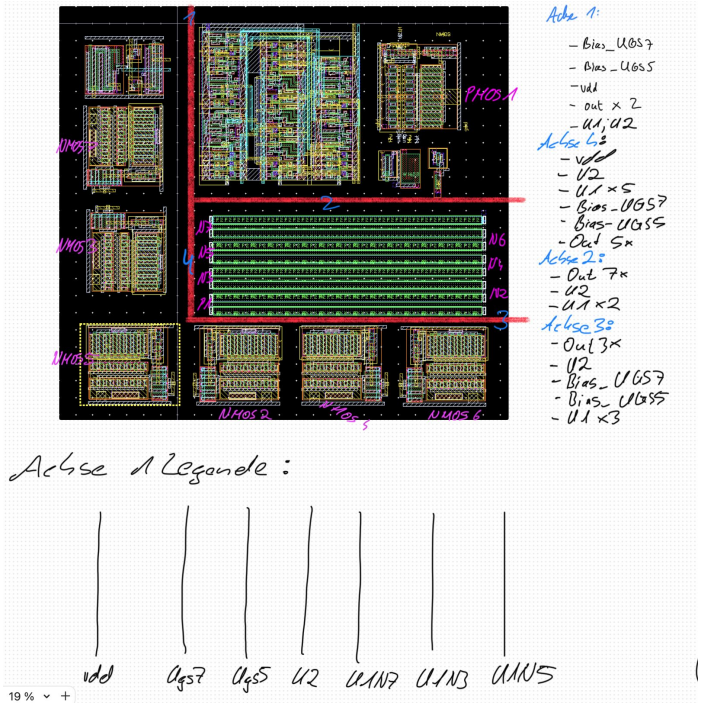
Planning in Freeform



Planning in Freeform



Planning in Freeform



Thank you for your attention!
Questions?

Sources

- https://www.researchgate.net/figure/Example-of-a-3-bit-Flash-ADC-4_fig15_304346665
- TESYS script
- Electronics I/II script
- XFAB application note
- Microelectronic Lab course (Prof. König)