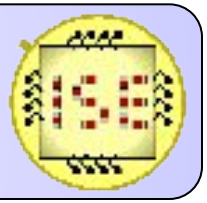
RPTU
Institute of
Cognitive Integrated Sensor Systems
Department of Electrical and Computer Engineering



Tesys Project SS23

3-Bit Rail to Rail DAC Design and Layout in XFAB 0.35 um CMOS Technology

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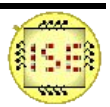
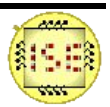
Conner Cordruwisch

Supervisor: Prof. Dr.-Ing. Andreas König



Overview



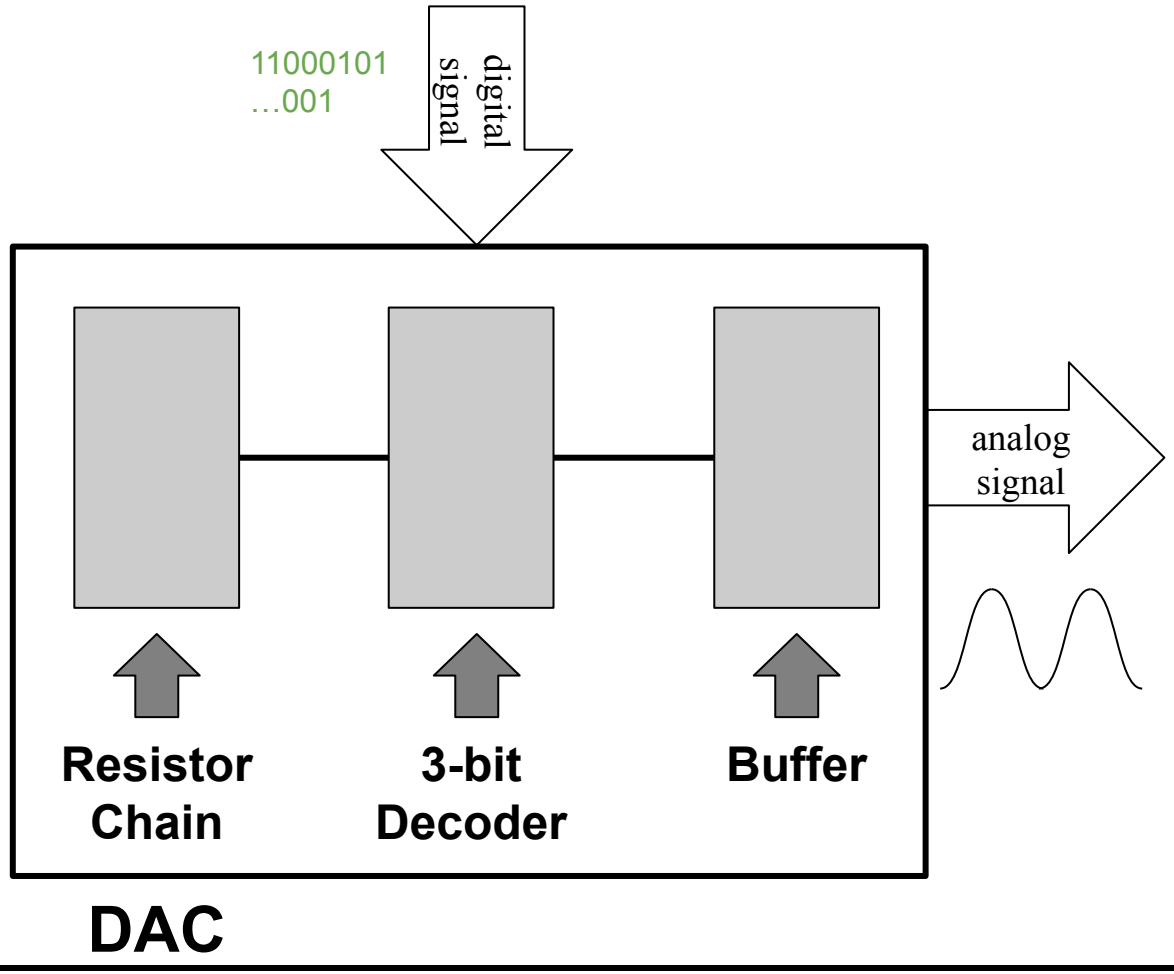
1.1 - Motivation

- Design methods for application-specific cells and blocks
  - Selection, dimensioning, simulation, layout

- Project contents:
  - Modeling, design, simulation, layout
  - Integration with analog structures in mixed-signal designs
  - Utilize state of the art software
  - Integration of industrial process parameters (XFAB 0.35 um)

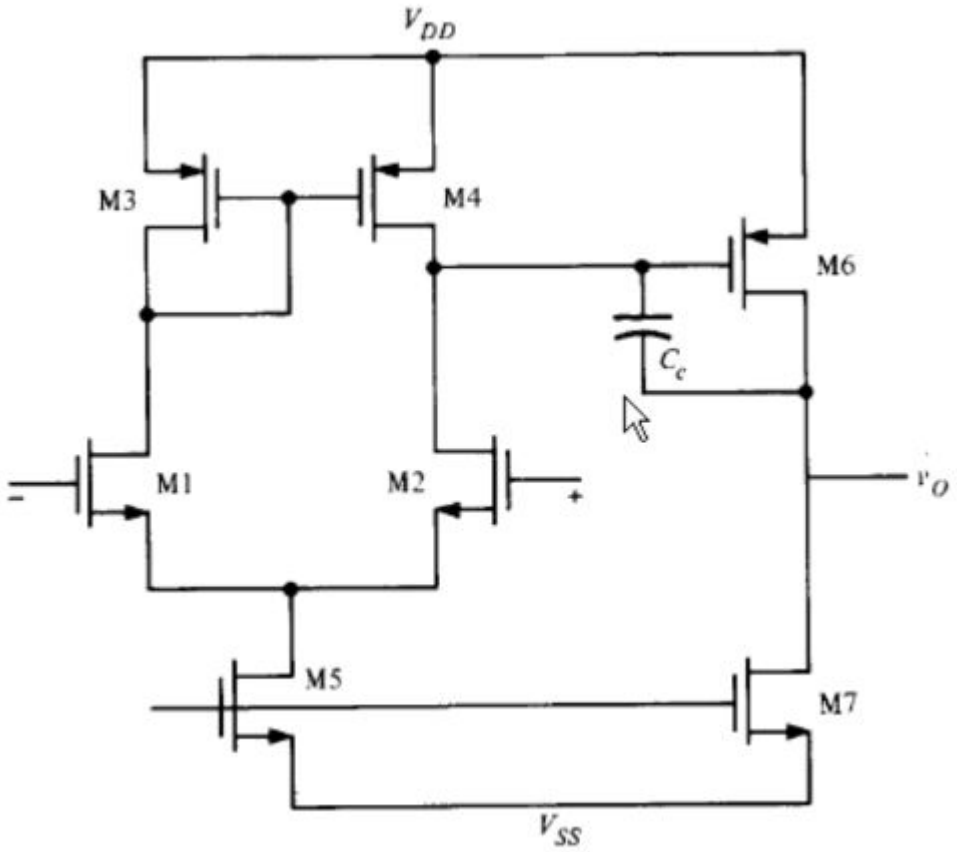
⇒ **3-Bit Rail to Rail DAC Design and Layout**

2 - Topology



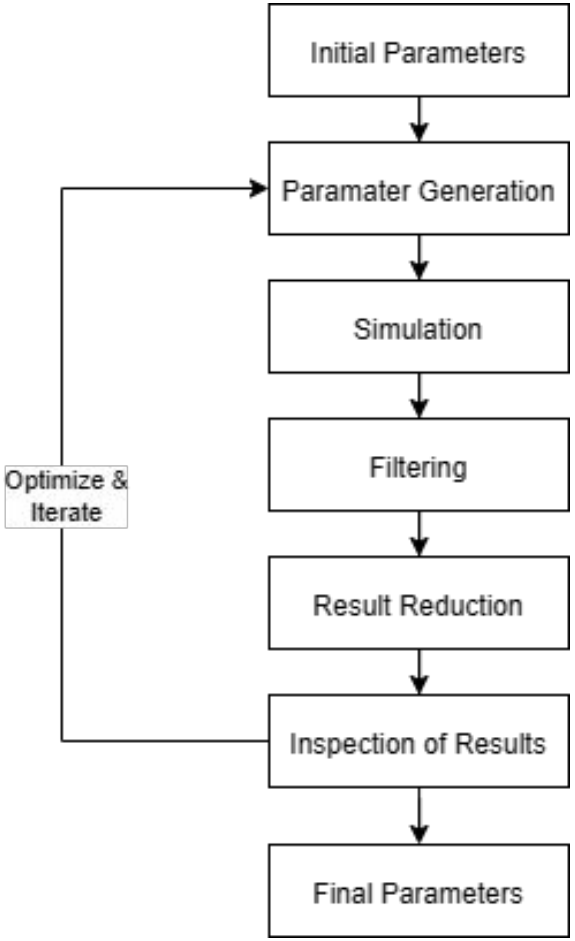
- 8 matched resistors
- PTL decoder
- Operational amplifier

3 - Component Design & Simulation



- Miller OpAmp configuration
- Designplan based on Allen/Holberg
- MATLAB implementation by Prof. Dr.-Ing. König
- Development of python adaption for extended parameter sweep

3 - Component Design & Simulation



- Sweep parameters:
  - AV0, GBW, CMRp, CMRm, ABp, ABm, SR
- Filtering:
  - drop transistors with dimension greater than 100 um
  - Metric:
    - 0.999 quantile for CMR
    - 0.999 quantile for OR
- Manual simulation and inspection of final parameters

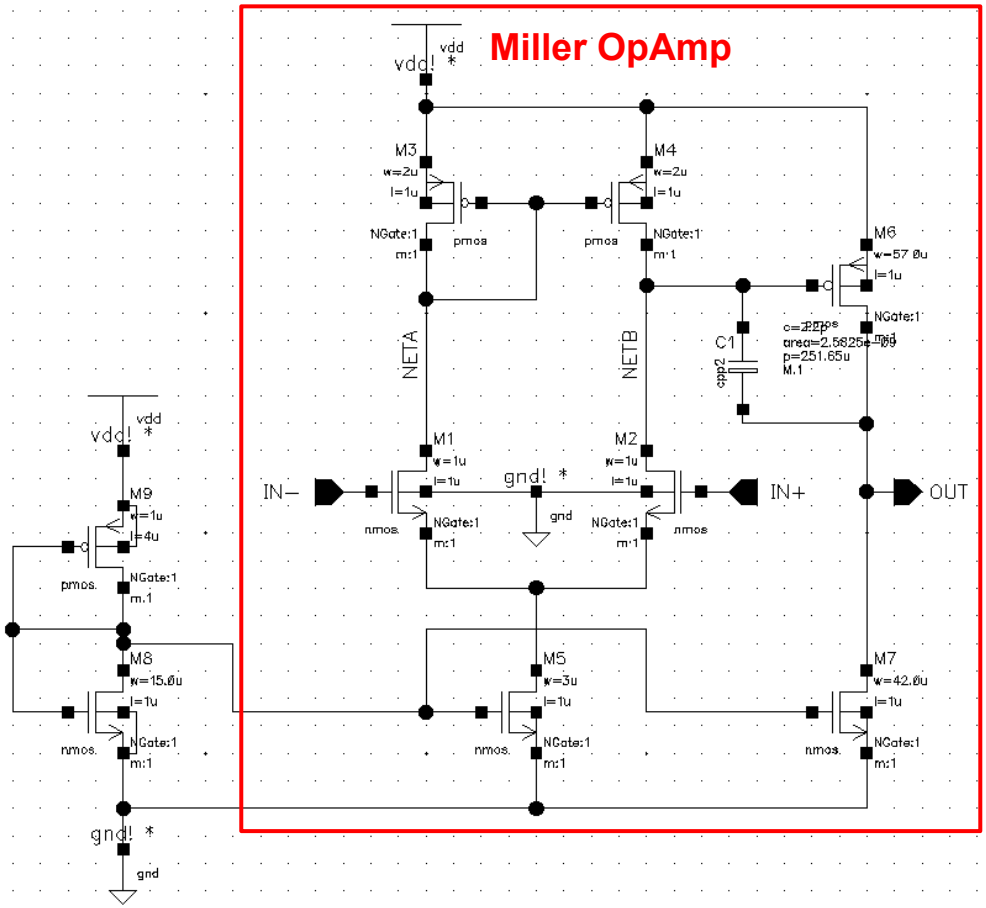
3 - Component Design & Simulation

Design Specification		Simulation Results	
AV0	60	I5	2.22E-06
GBW	2.00E+06	I7	2.25E-05
CMRp	1.45	S2	1
CMRm	-1.50	S3	2
ABp	0.70	S5	3
ABm	-0.80	S6	41
Phasemargin	1.05	S7	30
CMRR	80	Cc	2.22E-12
SR	1.00E+06	AV0_r	81.28063218
Ts	1.00E-09	Pdiss_r	8.16E-05
VDD	1.65	ABp_r	1.569649262
VSS	-1.65	ABm_r	-1.556066356
CL	1.00E-11	gm6	3.16E-04
RL	1.00E+05	gm2	3.63E-06
Pdiss	1	RI	1.43E+07
L	1.00E-06	RII	7.05E+05

- Optimized for:
  - small transistor dimensions
  - low power consumption

3.1 - Operational Amplifier

Schematic - Sizings

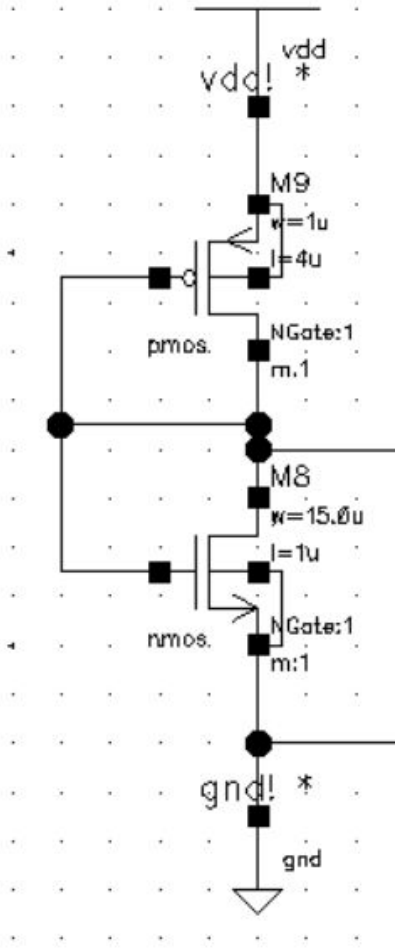


Transistor	W/L [um]
M1 / M2	1 / 1
M3 / M4	2 / 1
M5	3 / 1
M6	57 / 1
M7	42 / 1
M8	15 / 1
M9	1 / 4

- Optimization / Iteration of sizings for M6 & M7 to increase output driving capabilities

3.1 - Operational Amplifier

Schematic - Bias Circuit

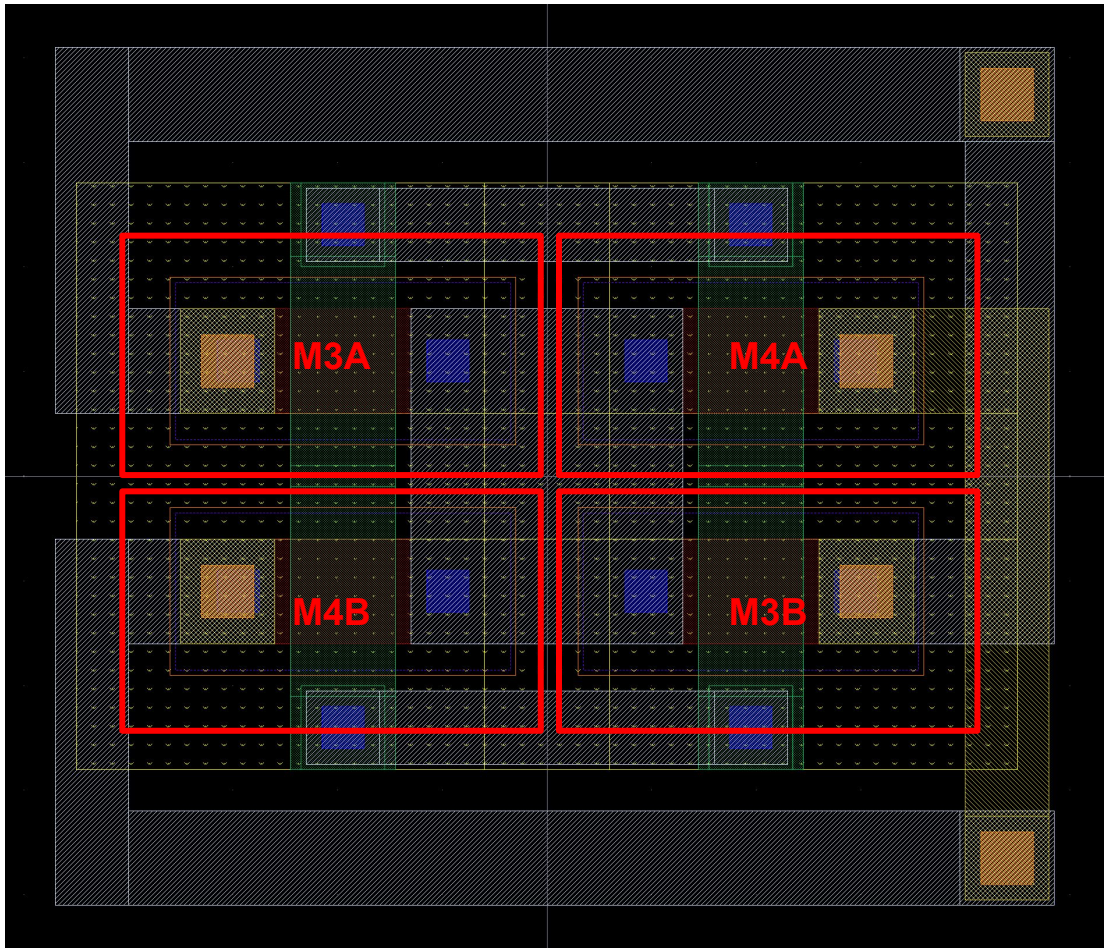


- MOST-Diode voltage divider
- Current mirror for I5 = 2.22 uA

- Optimized for low area
  - Parameter sweep of M8 & M9
  - Channel length adjustment
  - achieved current of 2.25 uA

3.1 - Operational Amplifier

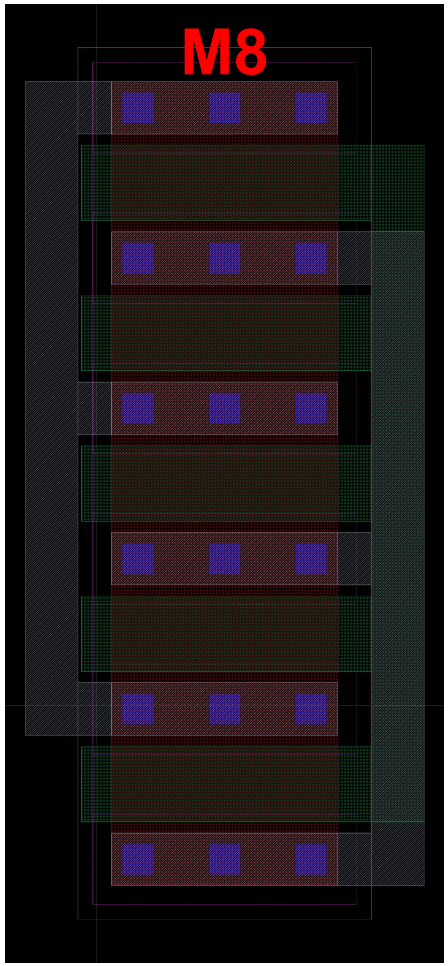
Layout - Differential Stage



- no matching for M1 & M2 due to small dimension width and length of 1 um
- custom matched centroid transistor layout for M3 & M4

3.1 - Operational Amplifier

Layout - Folded Transistors

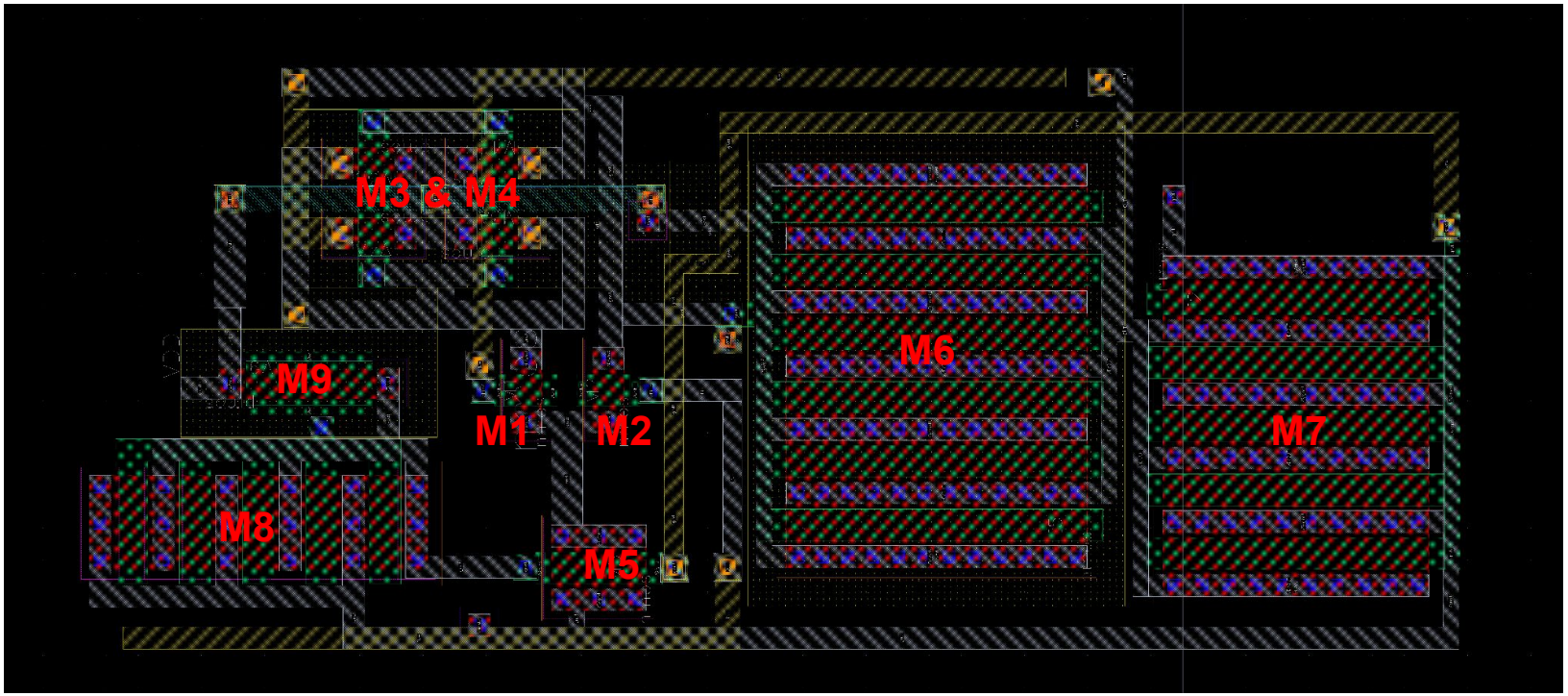


- Full custom folded transistor M8
- M6 & M7 generated from PRIMLIB template

- Advantages of folding
  - reduce area
  - flexibility of aspect ratio
  - minimize fabrication variation

3.1 - Operational Amplifier

Layout



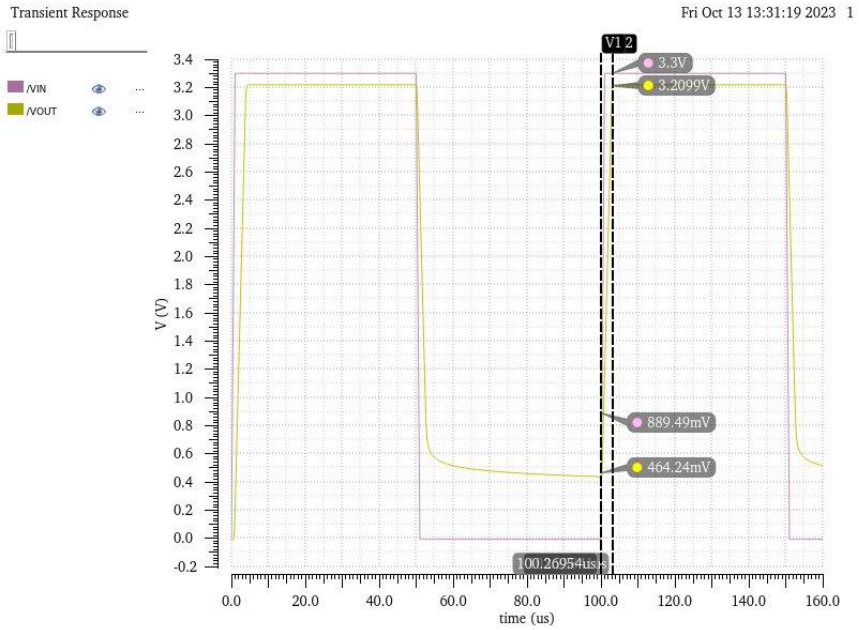
3.1 - Operational Amplifier

Final Specs

Parameters	Design Plan	Final Results
Open loop gain **AV0**	60dB	81.54dB
Gain **B**and-**W**idth	2MHz	1.10MHz
Common **M**ode **R**ange **p/m**	1.45V | -1.5V	1.61 V | -1.43 V
Phasemargin	60°	78.57°
Slew **R**ate	1 V/us	1.02 V/us
Settling **T**ime	1ns	0s
Output **R**ange **p/m**	1.56V | -1.56V	1.62 V | -1.63V

3.1 - Operational Amplifier

Simulation



Note: LSB not reachable due to limited ICMR.

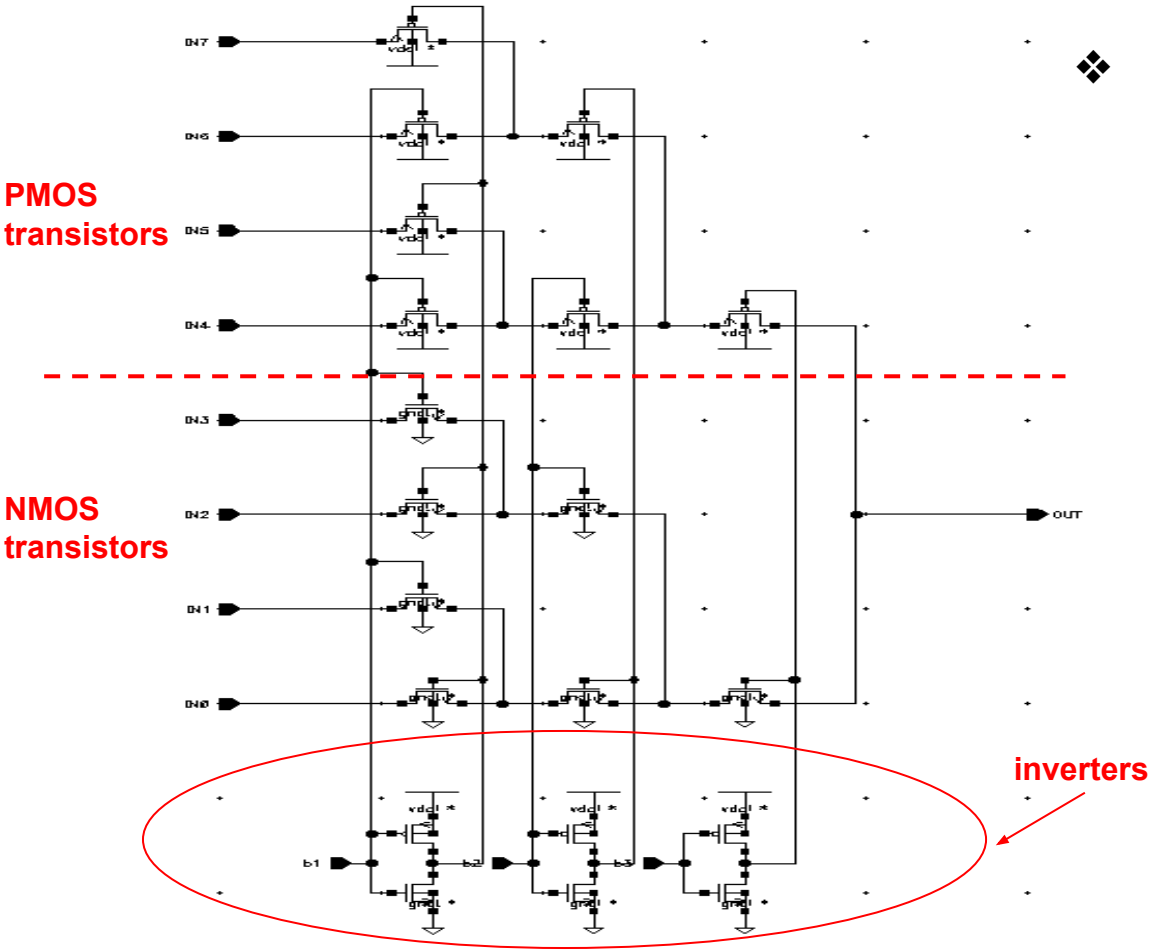
Possible solutions:

- ❖ independent output stage for lower stages
- ❖ Non-inverting OpAmp circuit with small gain
- ❖ Rail to Rail OpAmp Designplan

In consultation with the supervisor, it was decided, due to the advanced timeline, to retain the imperfection and proceed with the layout

3.2 - Decoder Logic

Schematic

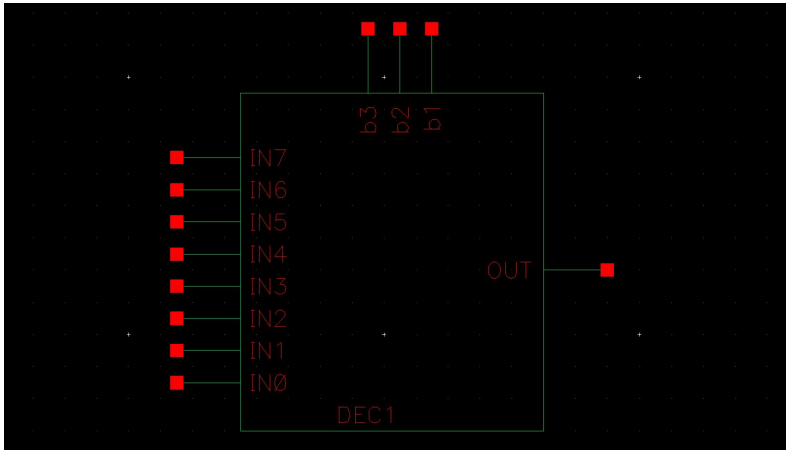


- Design based on “Analog integrated circuit design” by Johns David and Martin Kenneth W.
  - Pass Through Logic (PTL) design
  - area minimization

3.2 - Decoder Logic

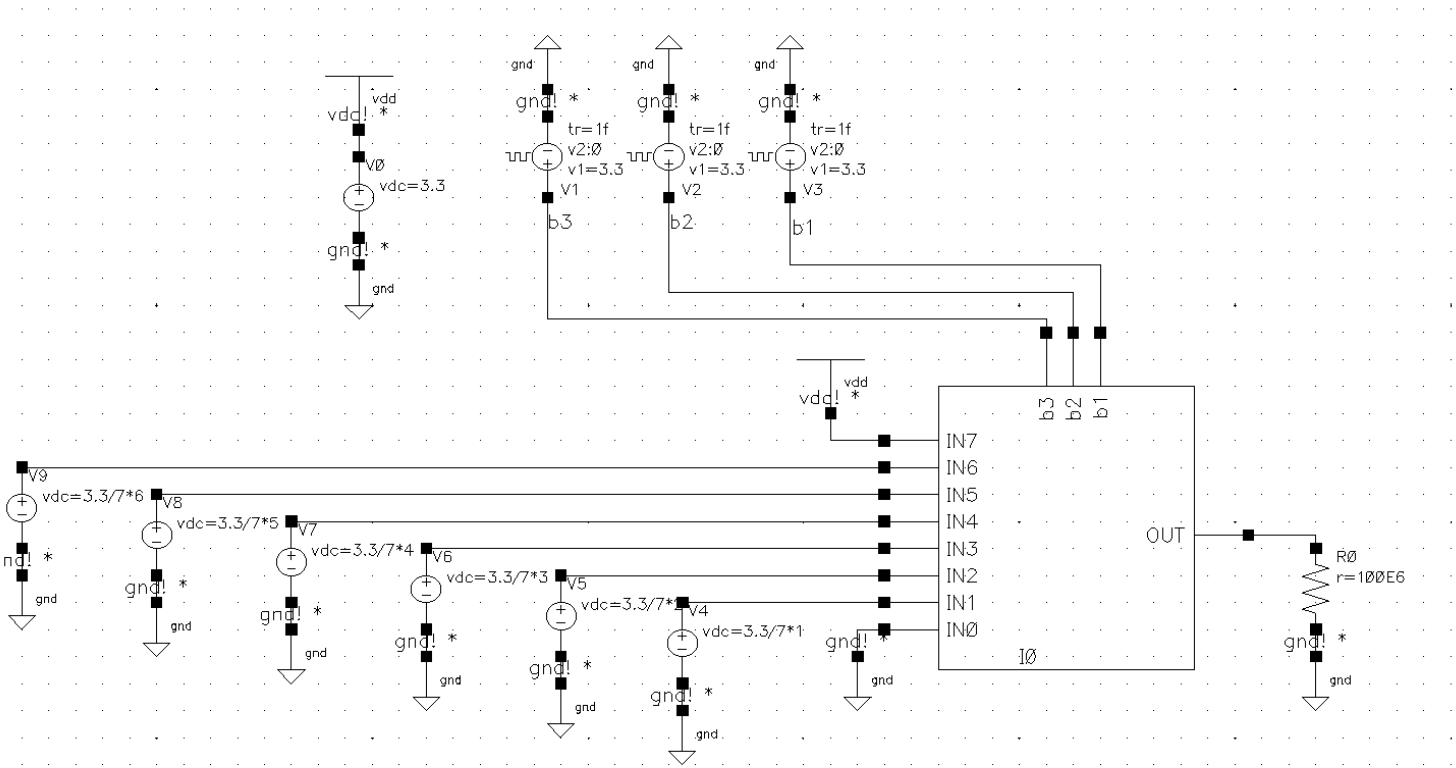
Layout

- Layout for 3-Bit decoder
- Usage of uniform 1 um PRIMLIB transistors



3.2 - Decoder Logic

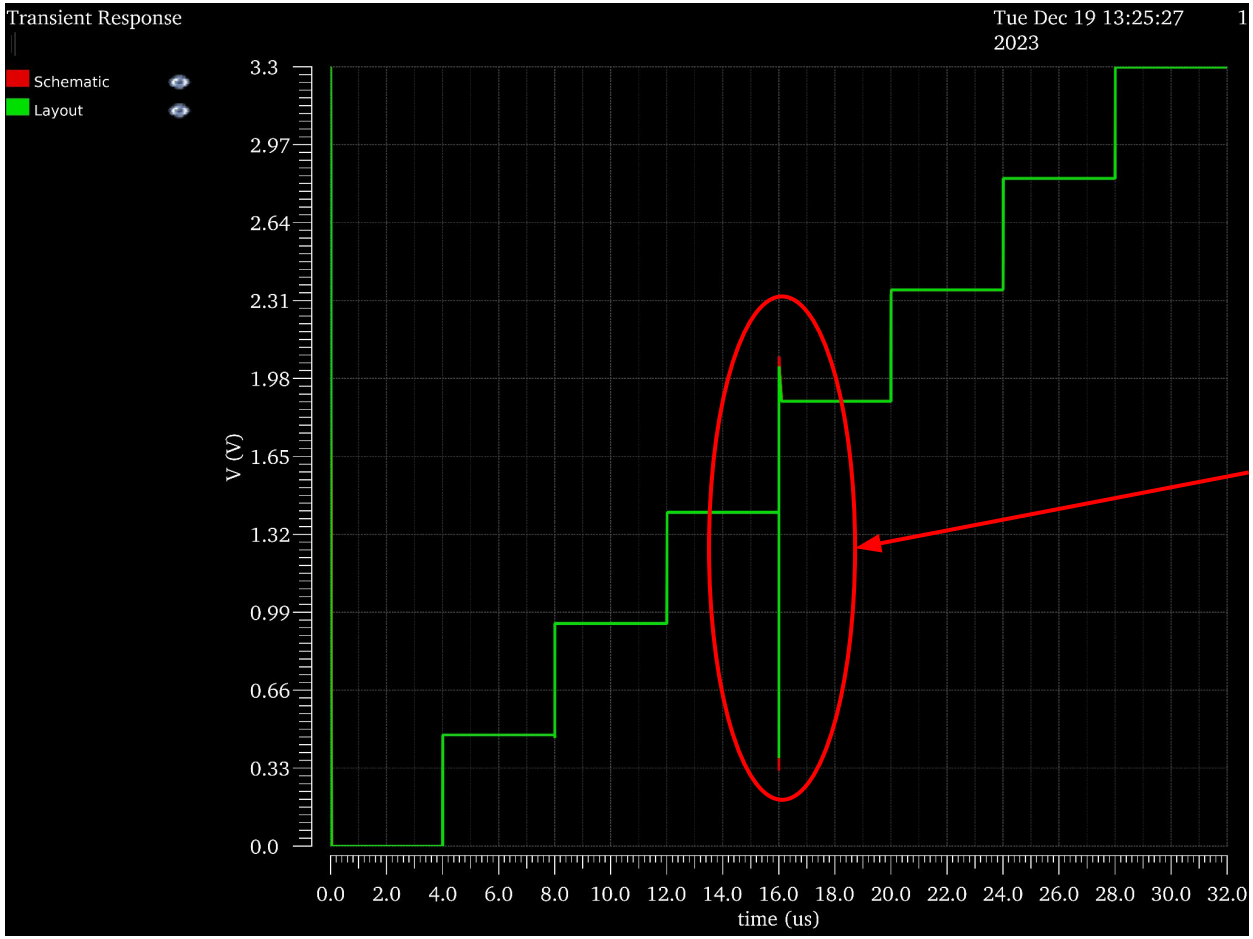
Simulation - Testbench



- Fixed input voltages
- Bit pattern for maximum decay and discrete rise

3.2 - Decoder Logic

Simulation - Layout vs. Schematic



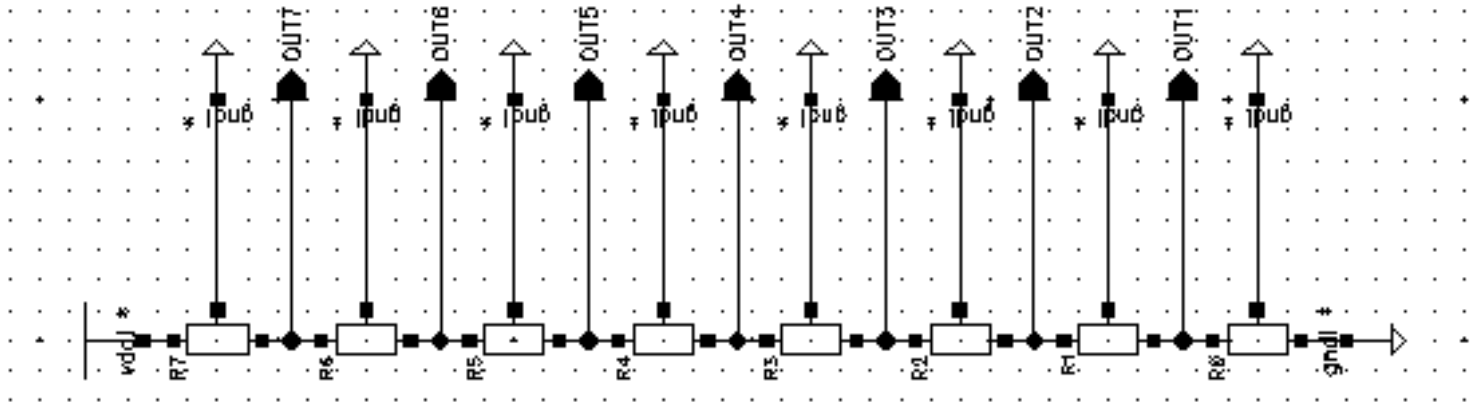
Transition from NMOS to PMOS transistors

3.3 - Resistive Divider

Schematic

- Goal: High impedance to minimize idle current
  - **PrimLib High-Res Poly2** Resistors

- Dimensions:
  - 2^3 = 8 Stages = 8 Resistors
  - 1um x 100um results in 10.734 kΩ
  - Power consumption: $(3.3\ V)^2 / (8 \times 10.734\ k\Omega) = 0.13\ mW$

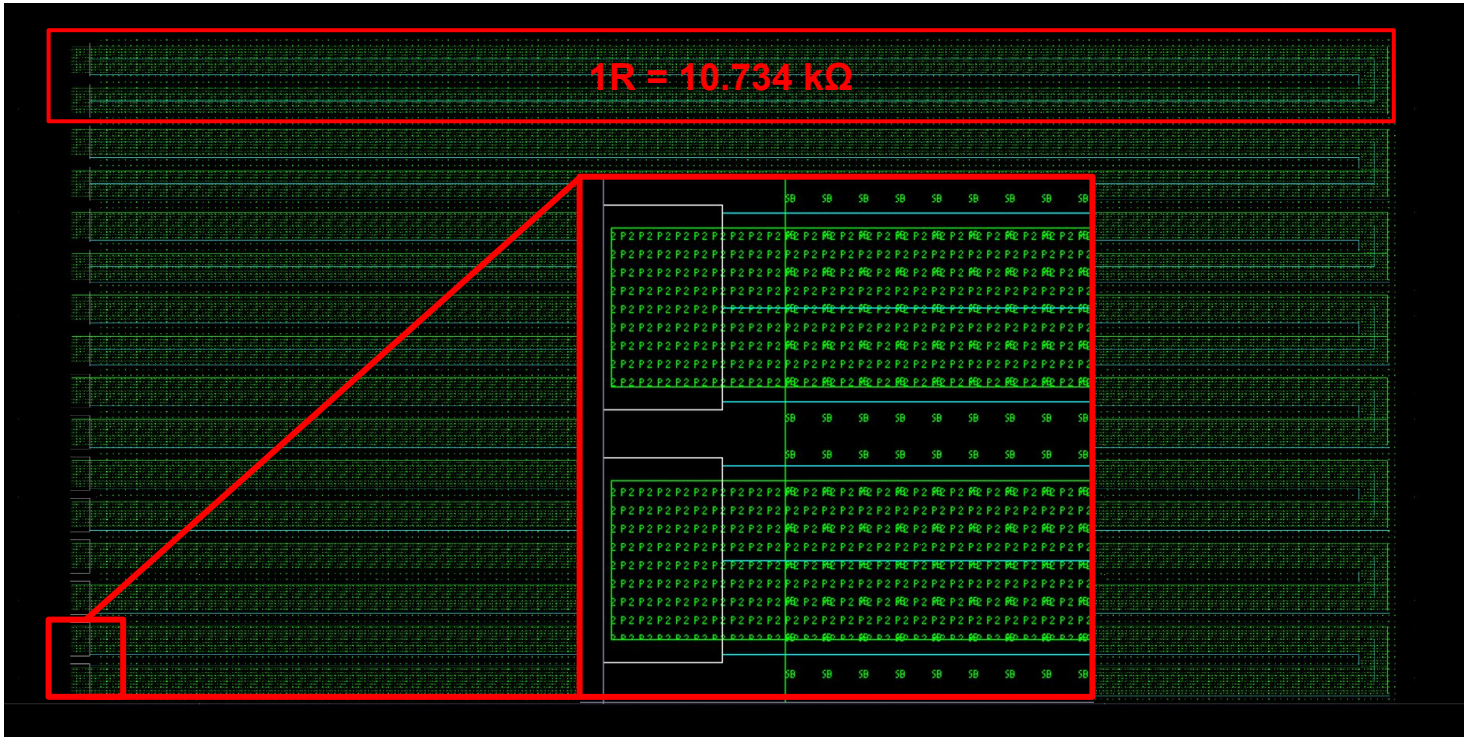


3.3 - Resistive Divider

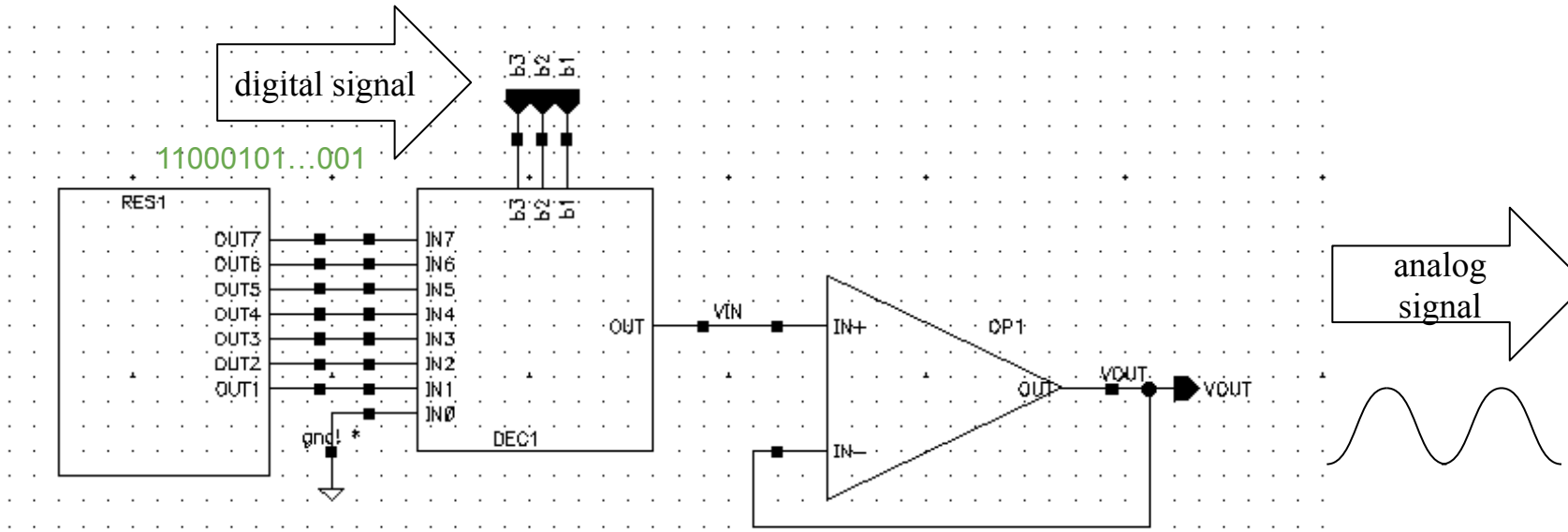
Layout

Fully custom layout design using:

- POLY2 (high resistance per area)



4 - DAC Design



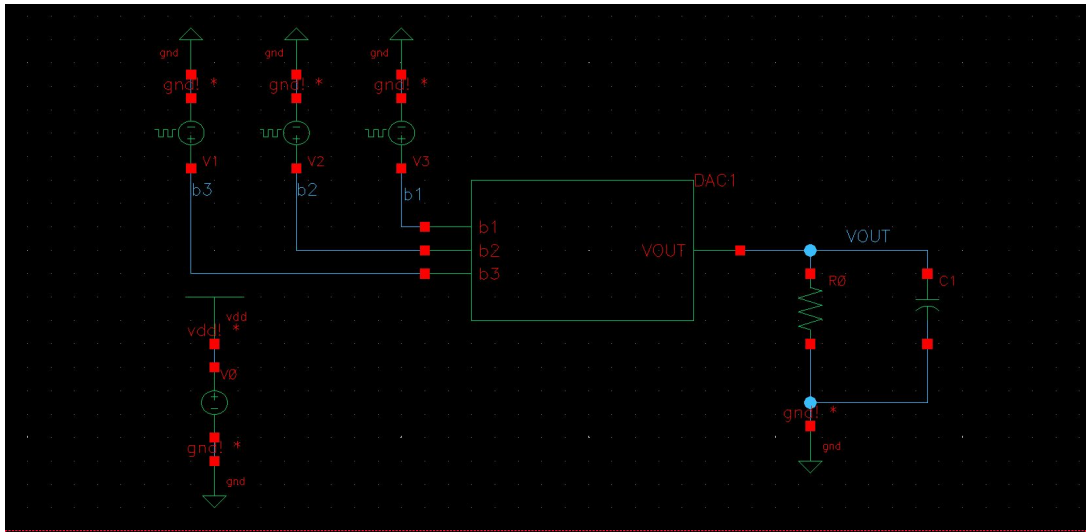
Resistor Chain

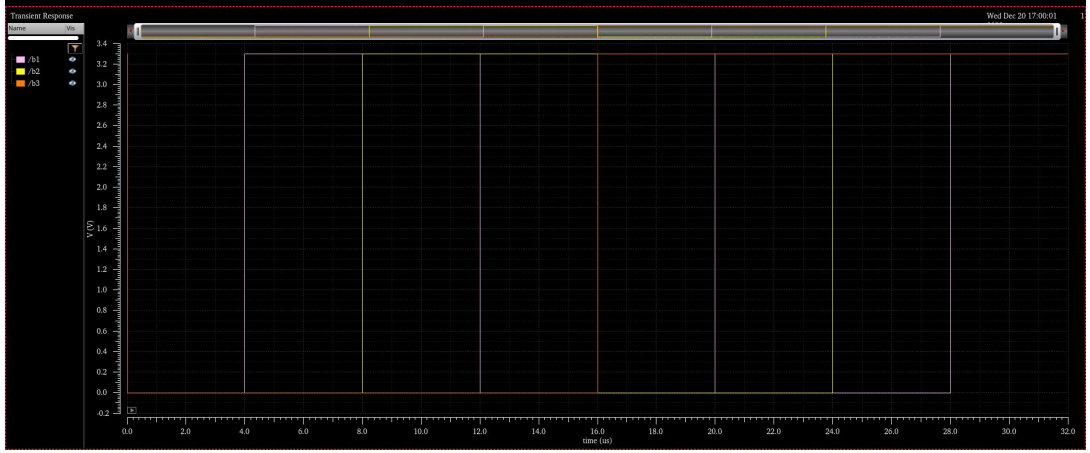
3-bit Decoder

Buffer

4.1 - DAC Design

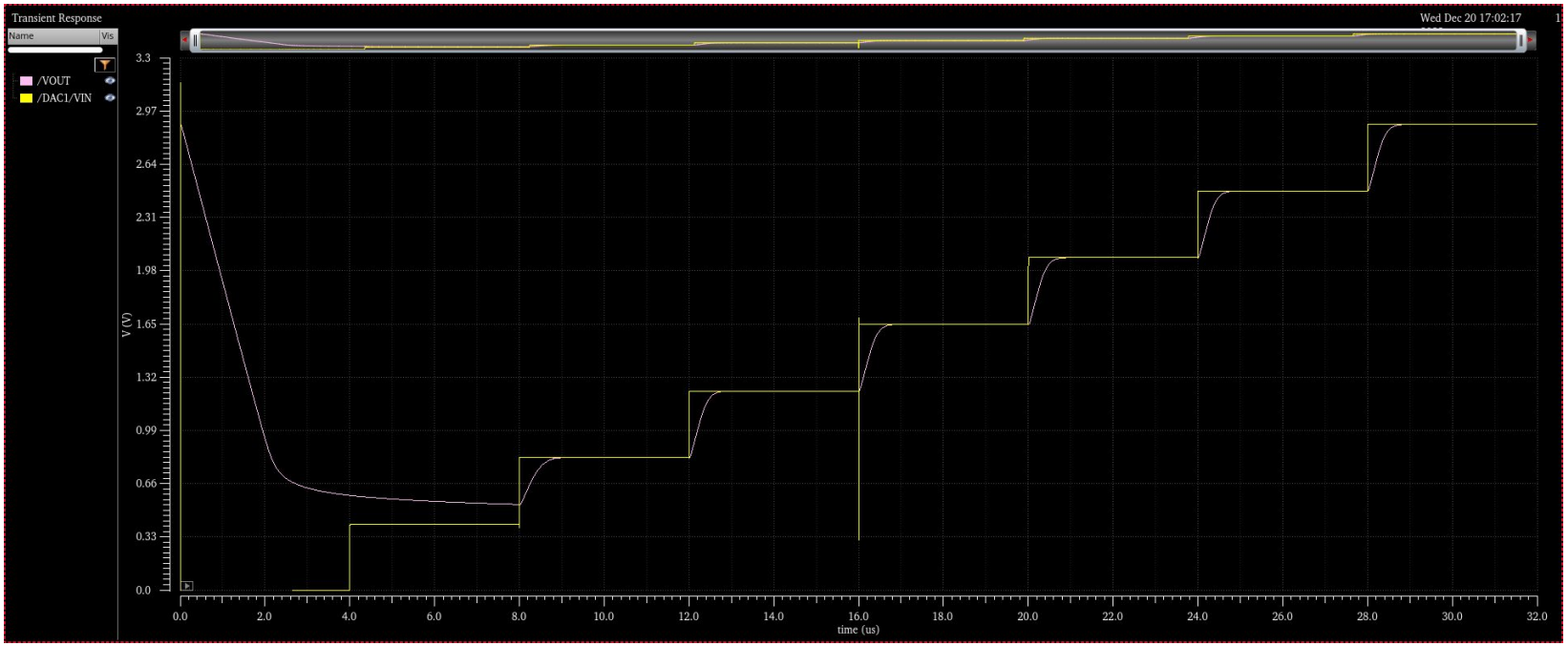
Testbench





4.1 - DAC Design

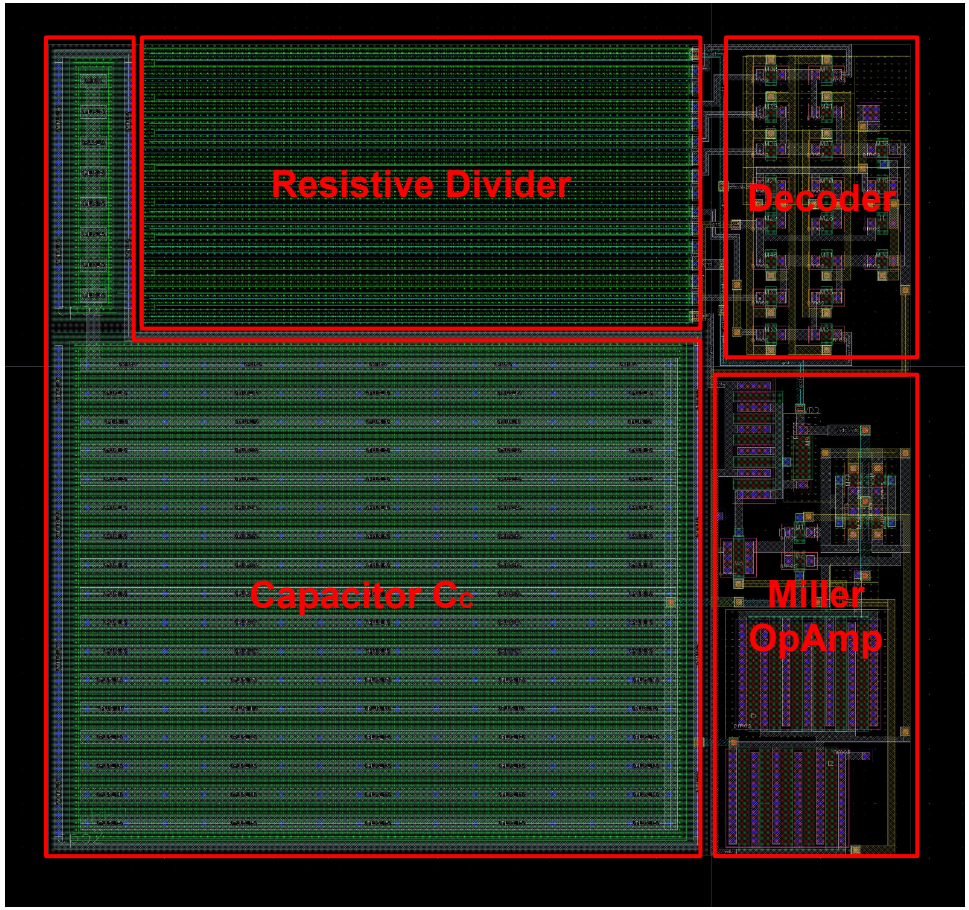
Simulation

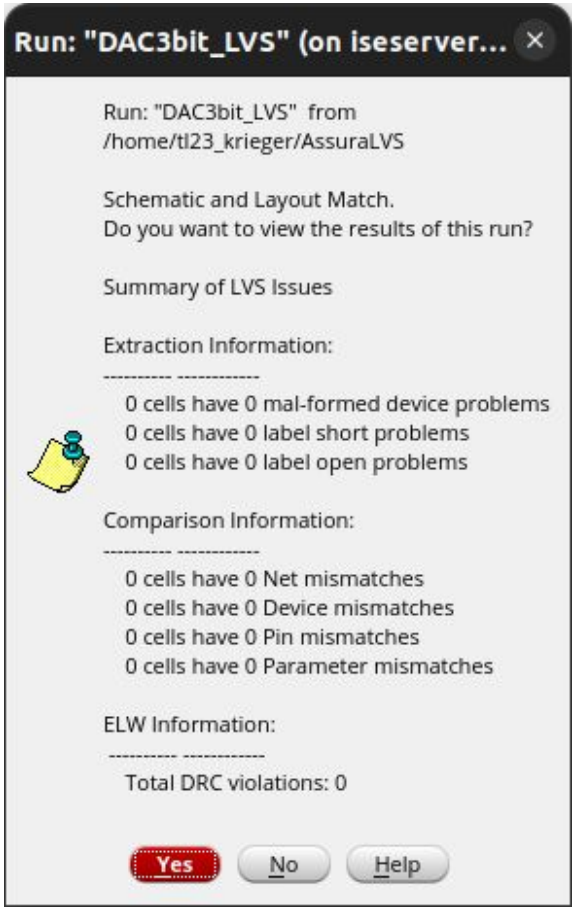


- Two lower bits cannot be reached due to limited ICMR
- Behaviour as expected with slew rate of 1 V/us

4.2 - DAC Design

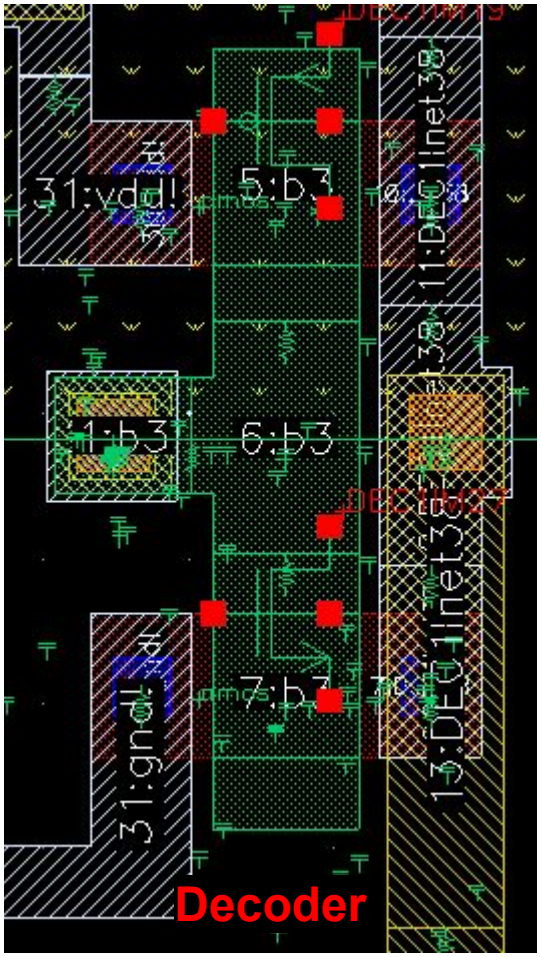
Layout

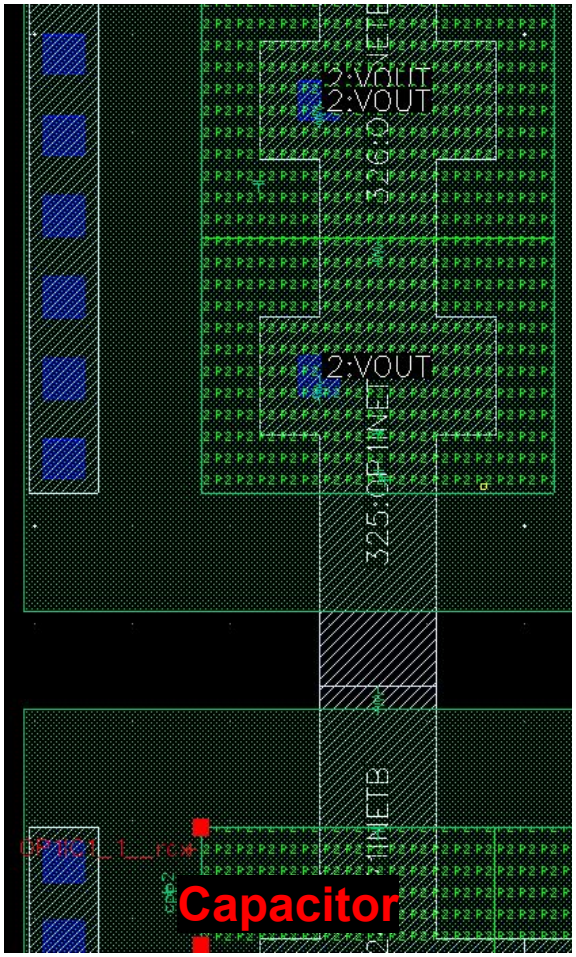


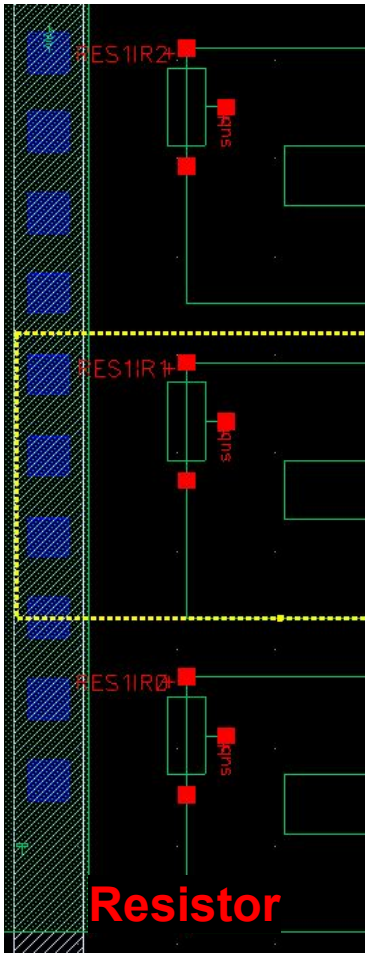


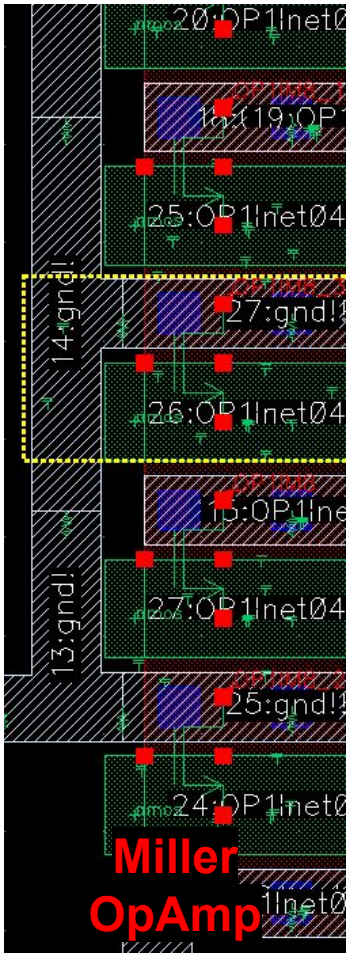
4.2 - DAC Design

Layout - Analog Extracted



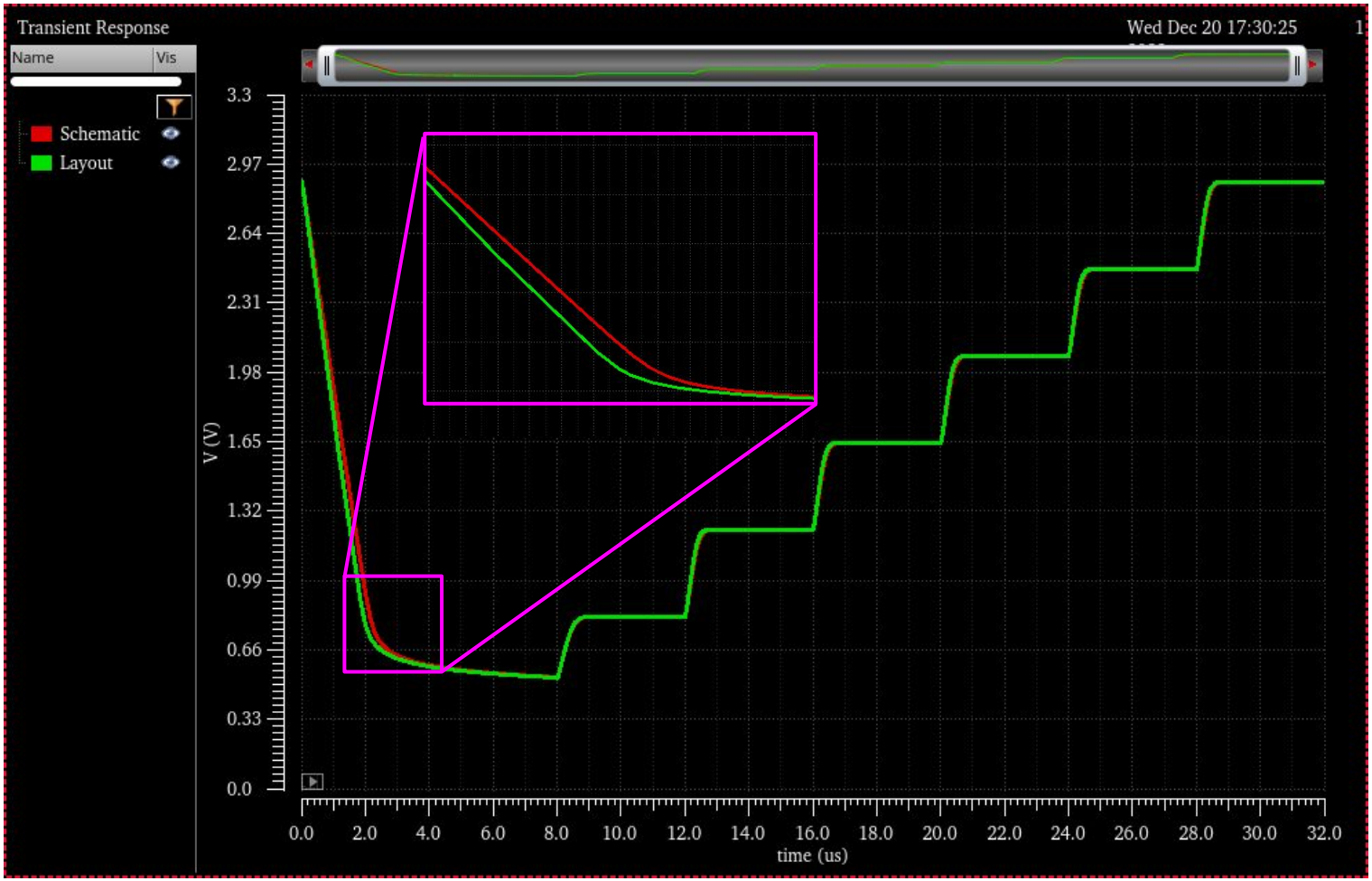






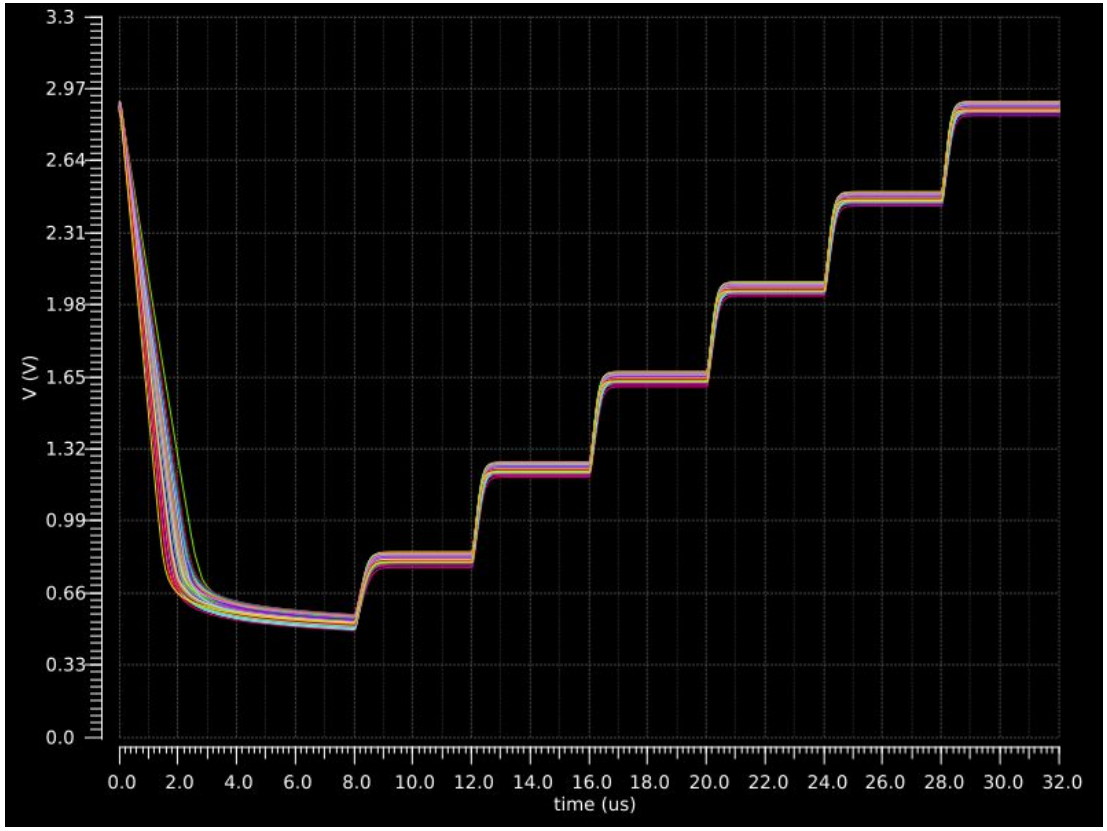
4.2 - DAC Design

Simulation - Layout vs. Schematic



4.2 - DAC Design

Simulation - Monte Carlo Analysis (Layout)



- Maximum deviation of voltage level: 68 mV
- Optimization potential
  - Resistors
  - Transistors
  - Capacitors

4.3 - DAC Design

Final Specs

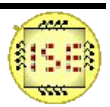
- **Area:** 78.825 um x 74.225 um = 0.00585 mm²
- **Static Power Consumption:** P = 3.3 V x 167.05 uA = 0.55 mW
- **Maximum Sampling Rate:** 378.63 kHz

5 - Conclusion

- Overview:
  - Introduction to a state-of-the-art tool for semiconductor chip fabrication
  - Design of an Operational Amplifier based on a specific design plan
  - Design and construction of a Digital-to-Analog Converter
  - Function simulation and verification
  - Layout implementation in 0.35 µm technology
  - Application of matched component techniques
  - Layout validation through simulation and Monte Carlo simulations

5 - Conclusion

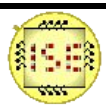
- Improvements:
  - Selection of a more sophisticated OpAmp layout for improved lower voltage representation
  - Mitigation of manufacturing variations impact on resistance divider voltage levels
  - Enhancement of bias circuit robustness



5 - Conclusion

Thank You for your attention!

Questions?



References

- Tesys Script
- Electronics 1/2 Script
- CMOS analog circuit design by Philip E. Allen and Douglas R. Holberg
- “Analog integrated circuit design” by Johns David and Martin Kenneth W.