

Analog MUX & Column Decoder Design for APS Matrix Readout

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TESYS Project, Summer Semester 2008

Under the guidance of

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&
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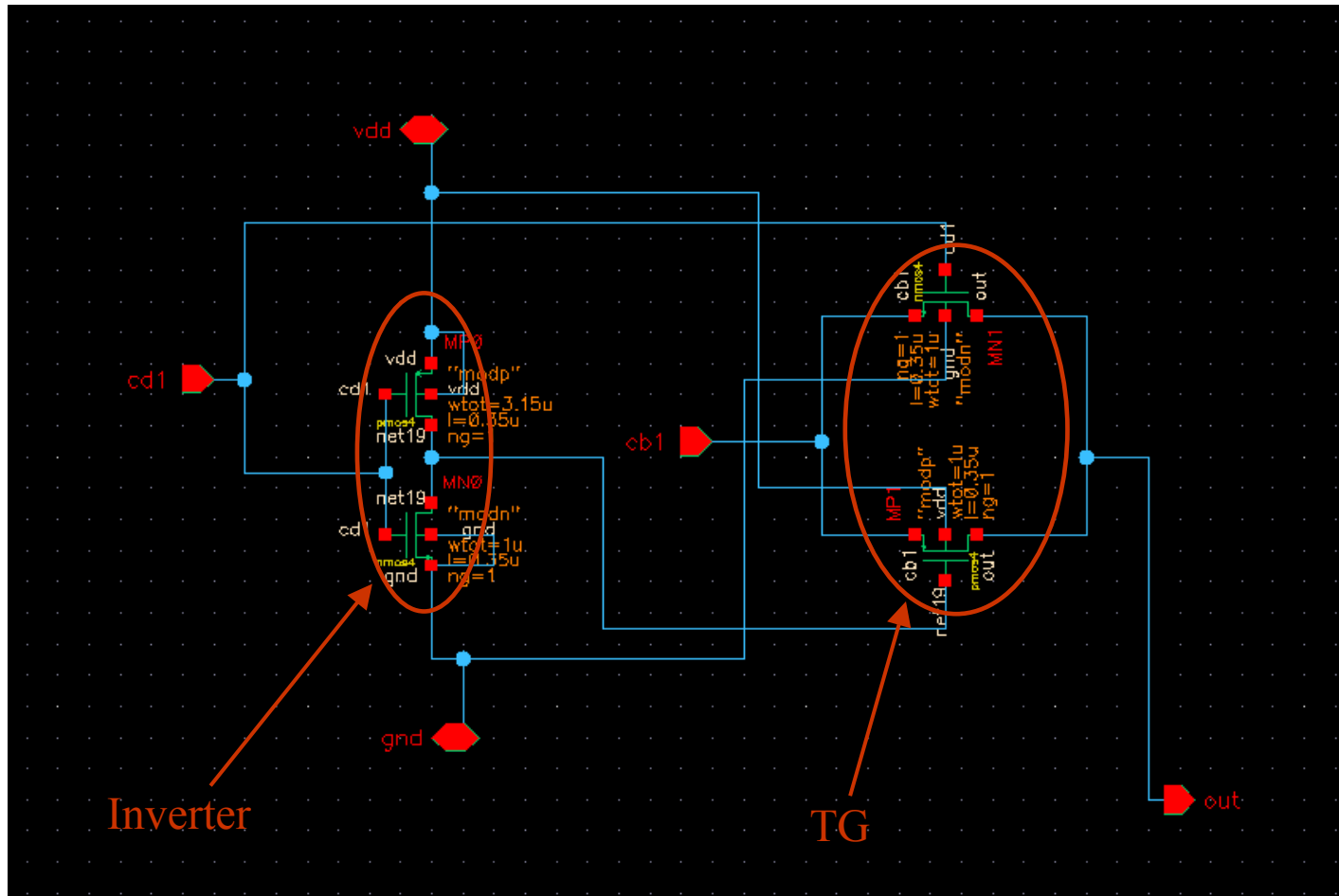
Overview of the Presentation

- Introduction
- Analog MUX Design
- Column Decoder Design
- Analog MUX and Decoder in APS
Matrix Simulation (Global Project)
- Global Project Overview (Source Mr. Juergen Hornberger)
- Results
- Conclusion
- Reference

Introduction

- Goal - design an Analog MUX and a 4-16 bit Column decoder for a APS sensor column output selection and read out
- Area constraint provided is $15\mu \times 300\mu$ for MUX and $40\mu \times 400\mu$ for Column Decoder
- The basic approach of Schematic, simulation, device sizing to Layout is followed
- Technology used is 0.35μ (4 Metal Layers) form Austriamicrosystems

Analog MUX Schematic (Single Cell)



Design Approximation for a Single Cell

➤ Inverter

P-MOS: $3.15\mu/0.35\mu$

N-MOS: $1\mu/0.35\mu$

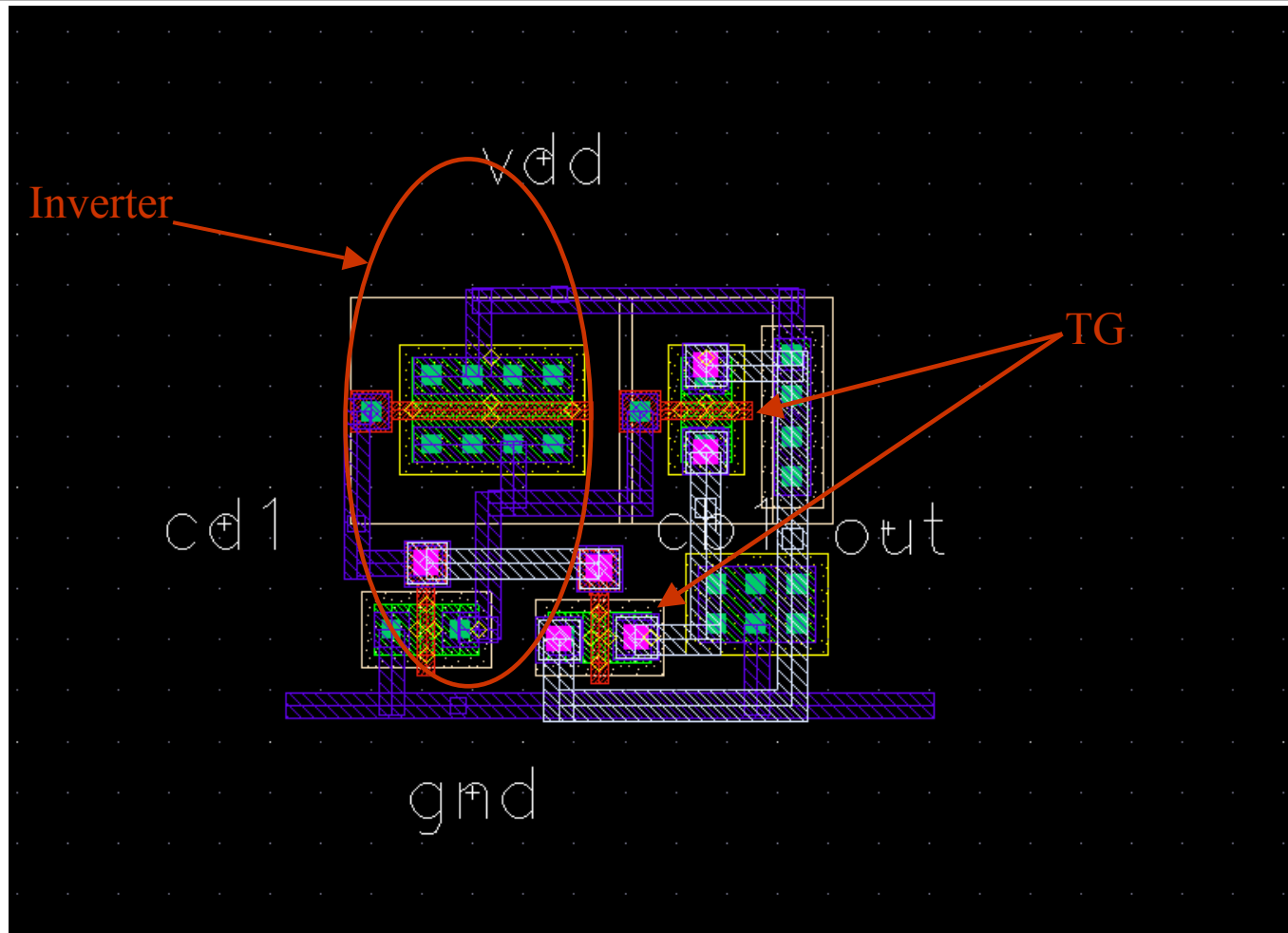
➤ Transmission Gate (TG)

P-MOS: $1\mu/0.35\mu$

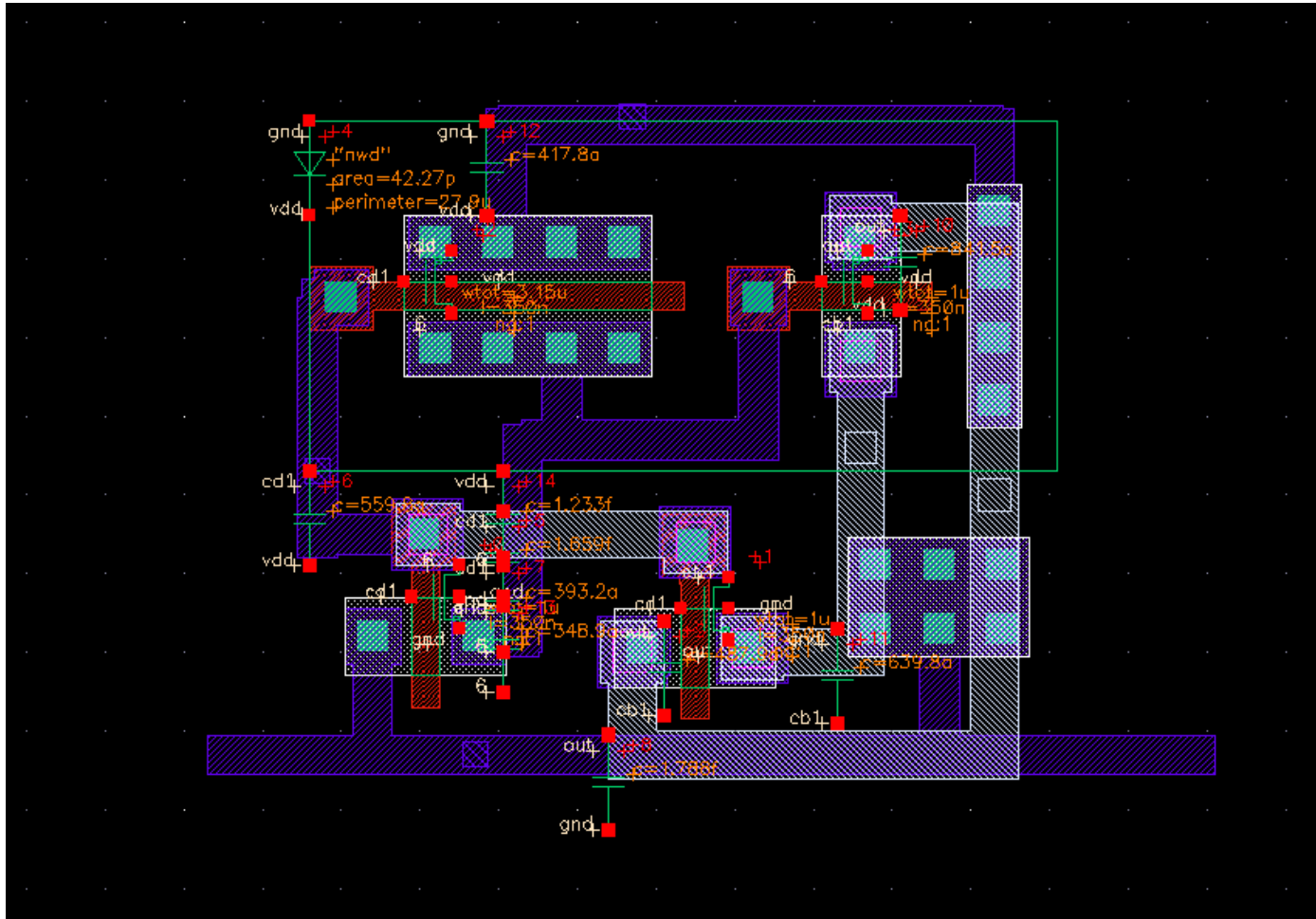
N-MOS: $1\mu/0.35\mu$

- TG acts as an analog switch, so it has to be kept small dimensions to reduce the delay also for a better readout time (W/L of TG is inversely proportional to read out time)

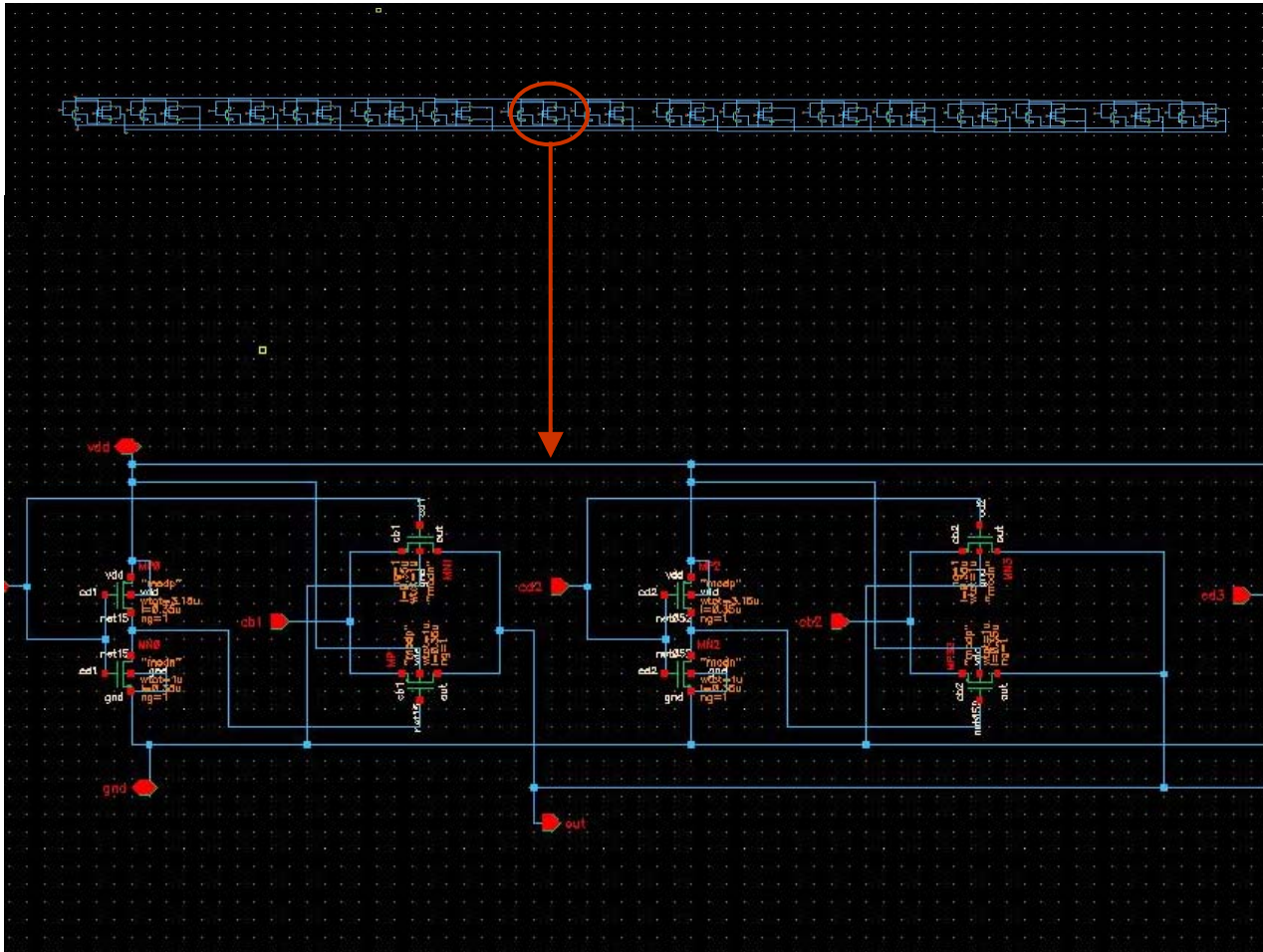
Analog MUX Single Cell Layout



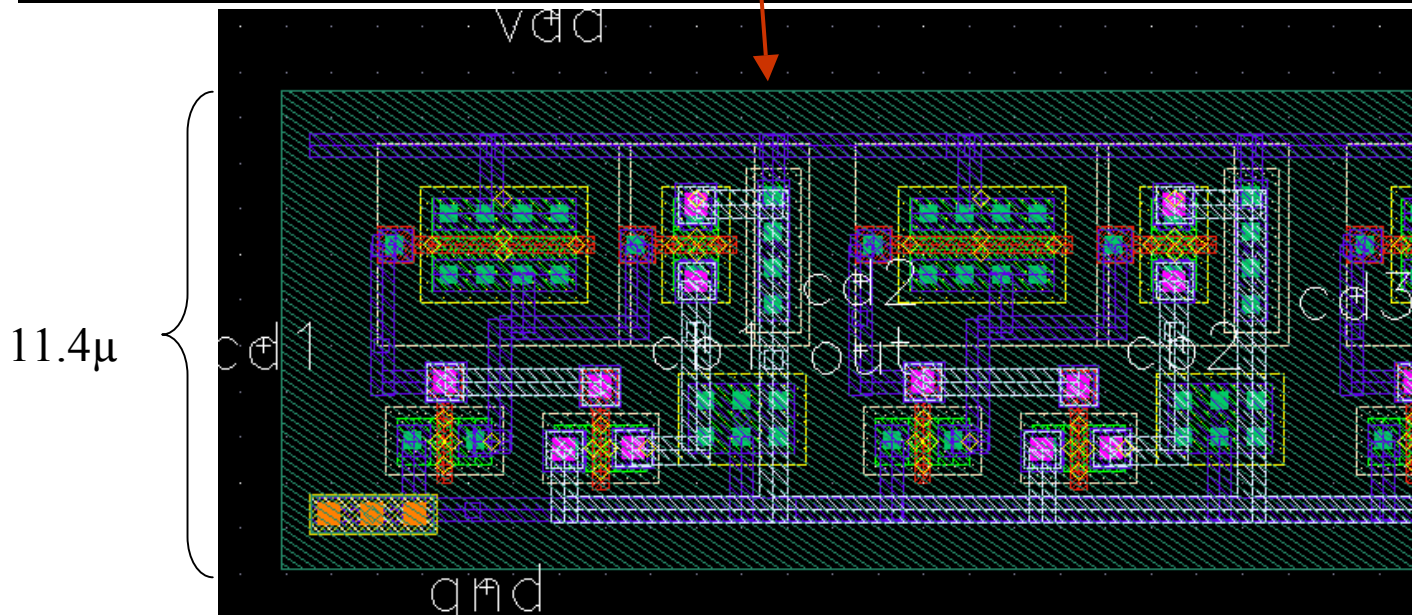
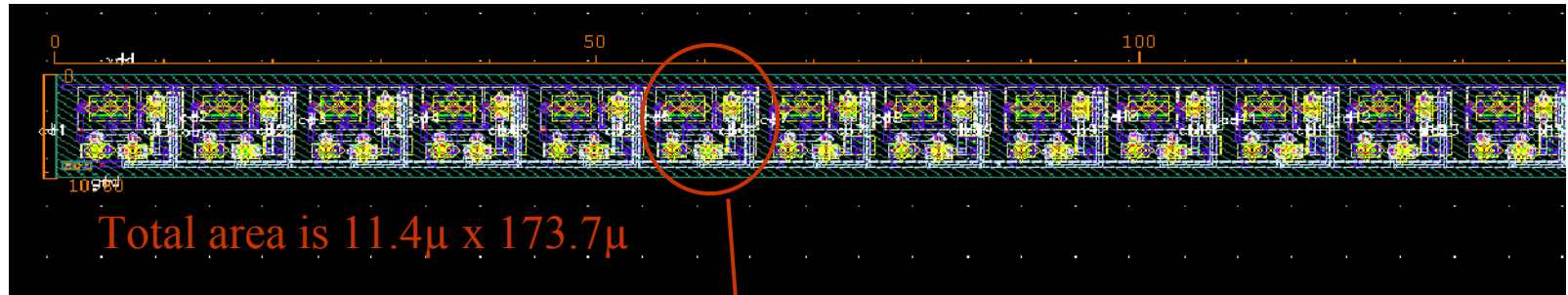
Analog MUX Single Cell Extracted



Analog MUX Schematic



Analog MUX Layout



LVS Check

```
/export/users/sens9/LVS/si.log
File Help 47
Warning: Unknown device "lat3" on a permuteDevice command.
Warning: Unknown device "vert15" on a permuteDevice command.
Warning: Unknown device "vert10" on a permuteDevice command.
Warning: Unknown device "vert5" on a permuteDevice command.
Warning: Unknown device "pmosm4" on a permuteDevice command.
Warning: Unknown device "rmosmh4" on a permuteDevice command.
Warning: Unknown device "rmosm4" on a permuteDevice command.
Warning: Unknown device "rmosh6" on a permuteDevice command.
Warning: Unknown device "rmosh4" on a permuteDevice command.
Warning: Unknown device "ng" on a permuteDevice command.
Warning: Unknown device "cvar" on a permuteDevice command.
Warning: Unknown device "csandwt" on a permuteDevice command.
Warning: Unknown device "cpoly" on a permuteDevice command.
Warning: Unknown device "zd2sm24" on a permuteDevice command.
Warning: Unknown device "pd" on a permuteDevice command.
Warning: Unknown device "nwd" on a permuteDevice command.
Warning: Unknown device "nd" on a permuteDevice command.

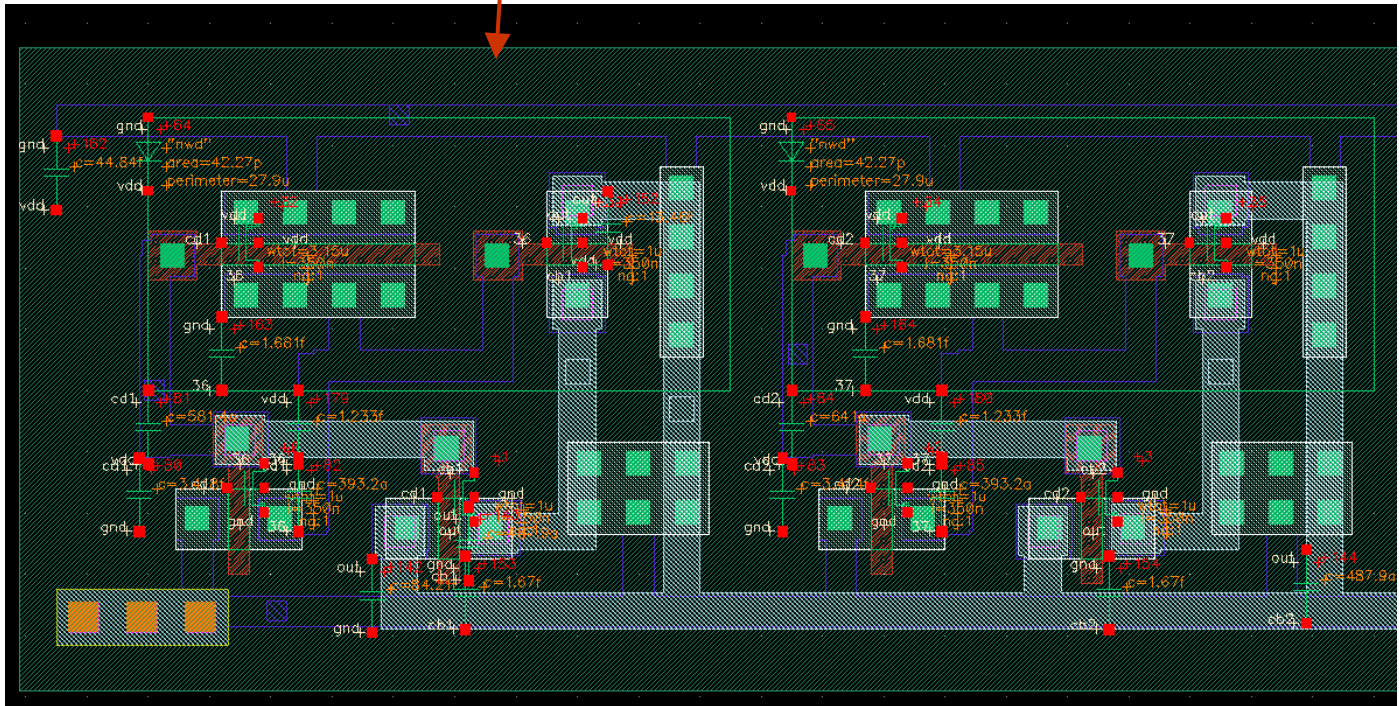
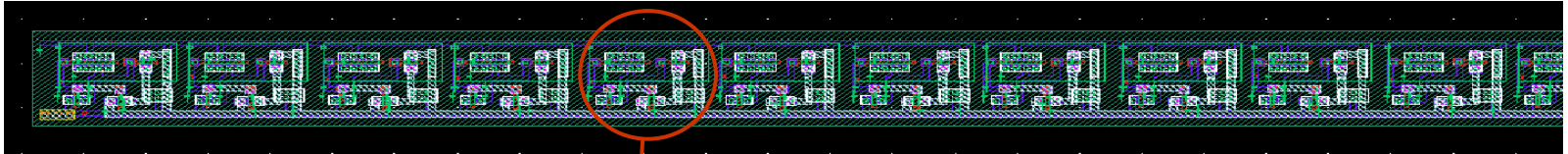
The net-lists match.

                layout schematic
                instances
un-matched      0      0
rewired         0      0
size errors     0      0
pruned         0      0
active         64     64
total          64     64

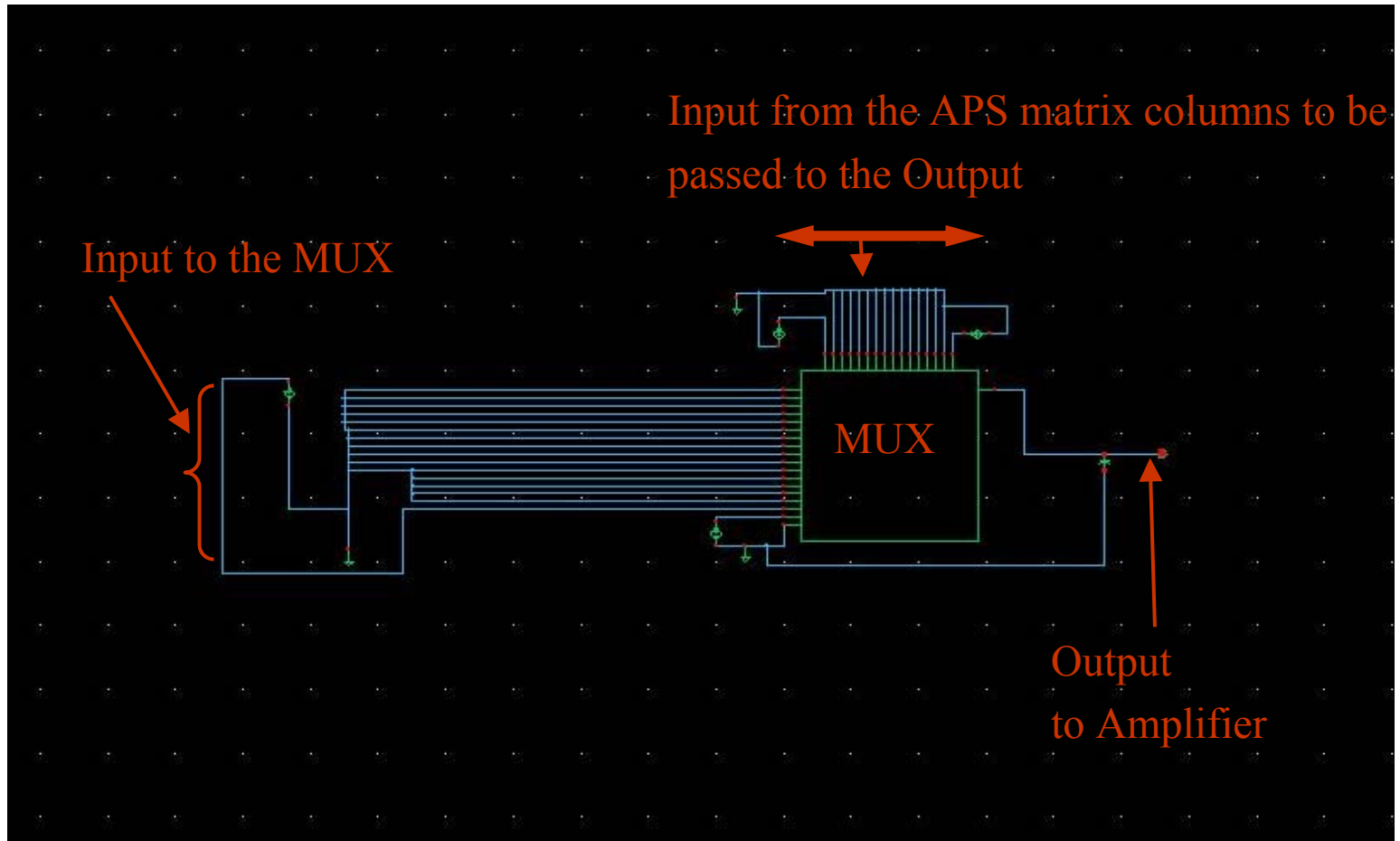
                nets
un-matched      0      0
merged         0      0
pruned         0      0
active         51     51
total          51     51

                terminals
un-matched      0      0
matched but
different type  0      0
total           35     35
End comparison: Nov 14 17:13:00 2008
```

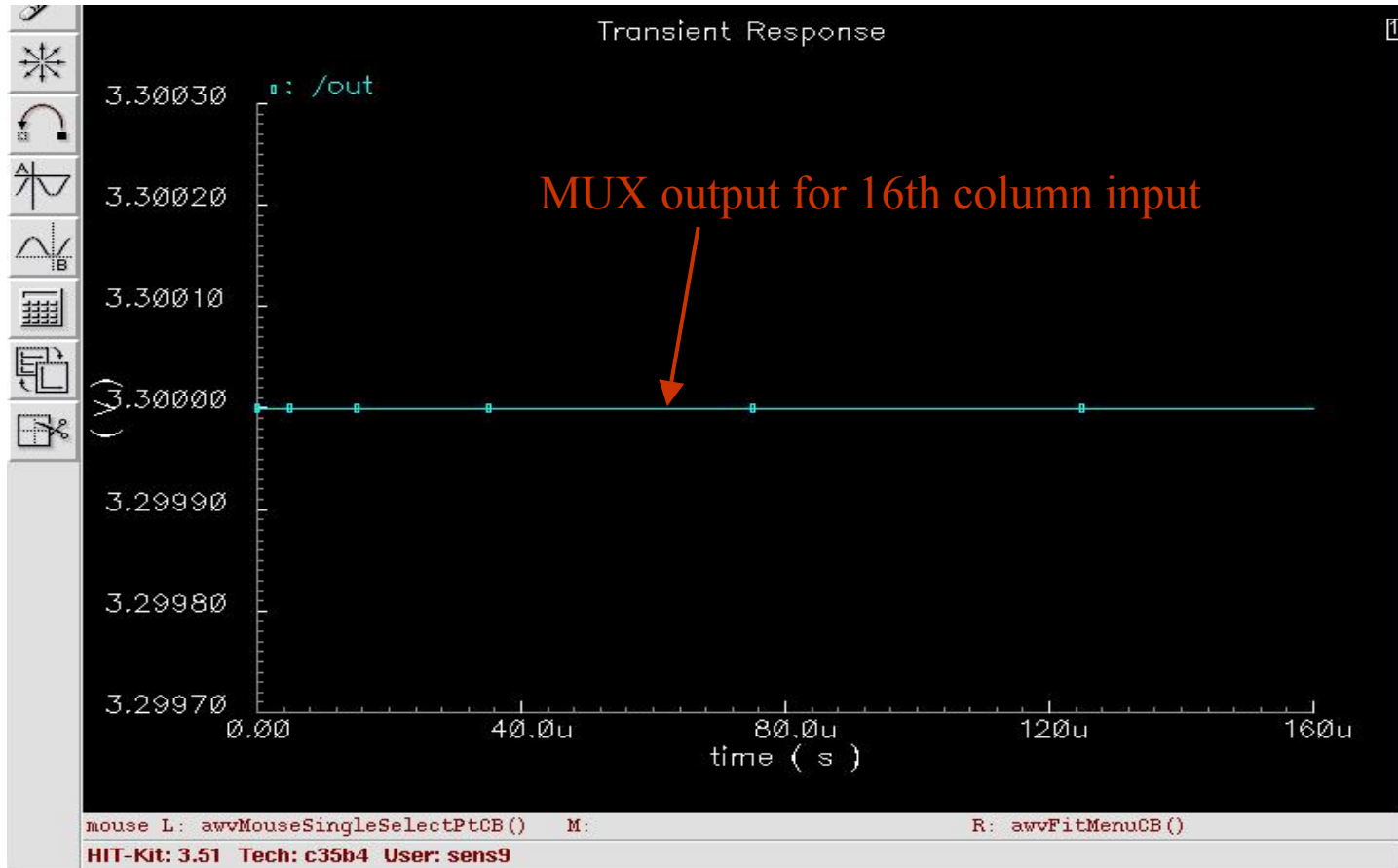
Analog MUX Extracted



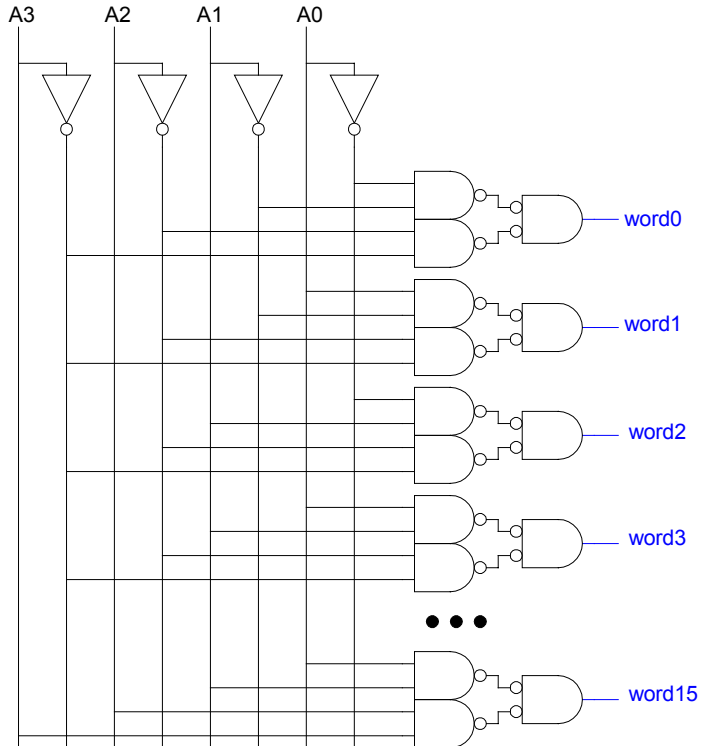
Analog MUX Simulation Set Up



Simulation Output (Extracted)



Decoder Design



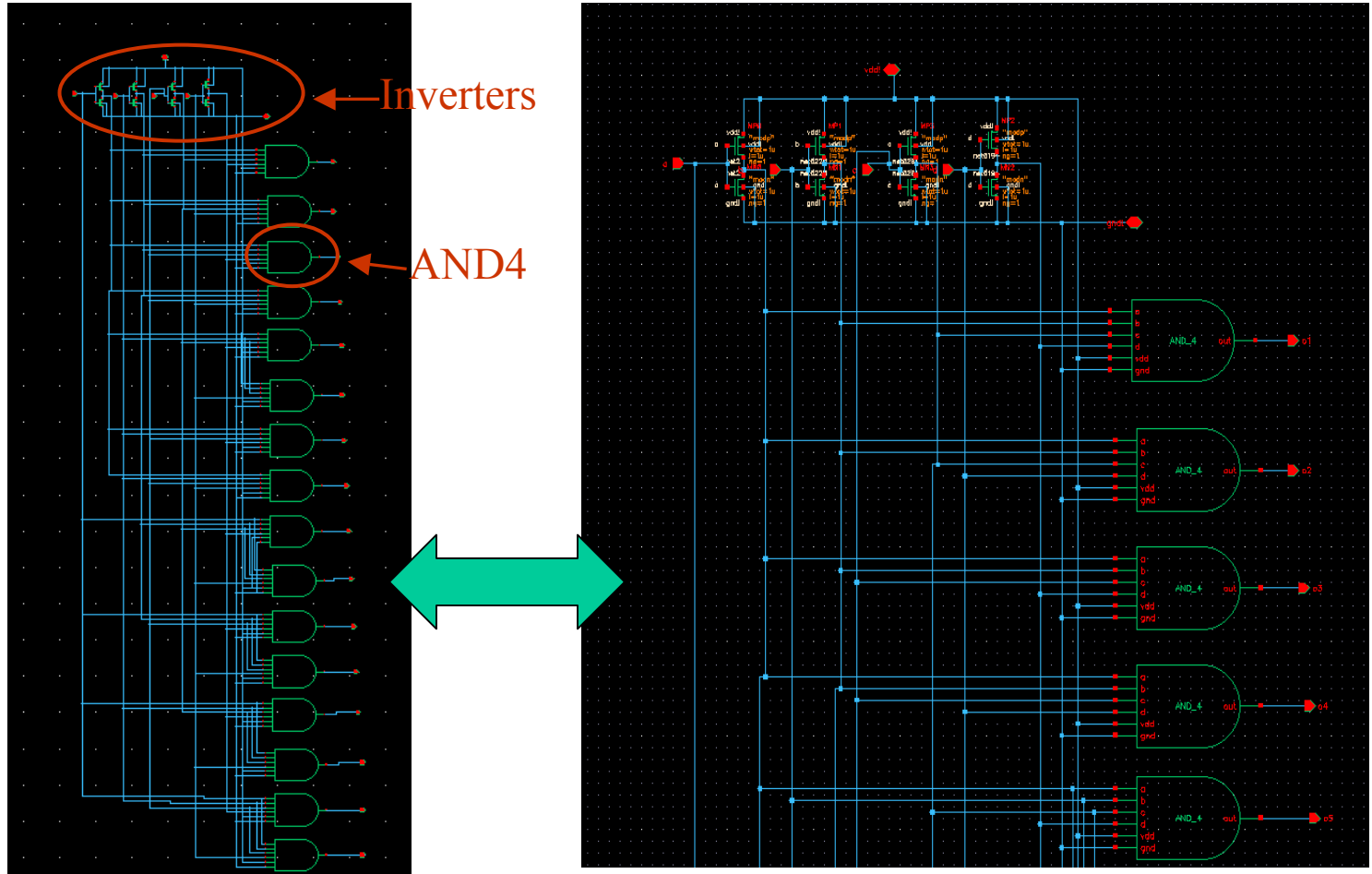
Truth Table

| A | B | C | D | Out |
|---|---|---|---|------------------|
| 0 | 0 | 0 | 0 | 0000000000000001 |
| 0 | 0 | 0 | 1 | 0000000000000010 |
| 0 | 0 | 1 | 0 | 0000000000000100 |
| 0 | 0 | 1 | 1 | 0000000000001000 |
| : | : | : | : | : |
| : | : | : | : | : |
| : | : | : | : | : |
| 1 | 1 | 1 | 0 | 0100000000000000 |
| 1 | 1 | 1 | 1 | 1000000000000000 |

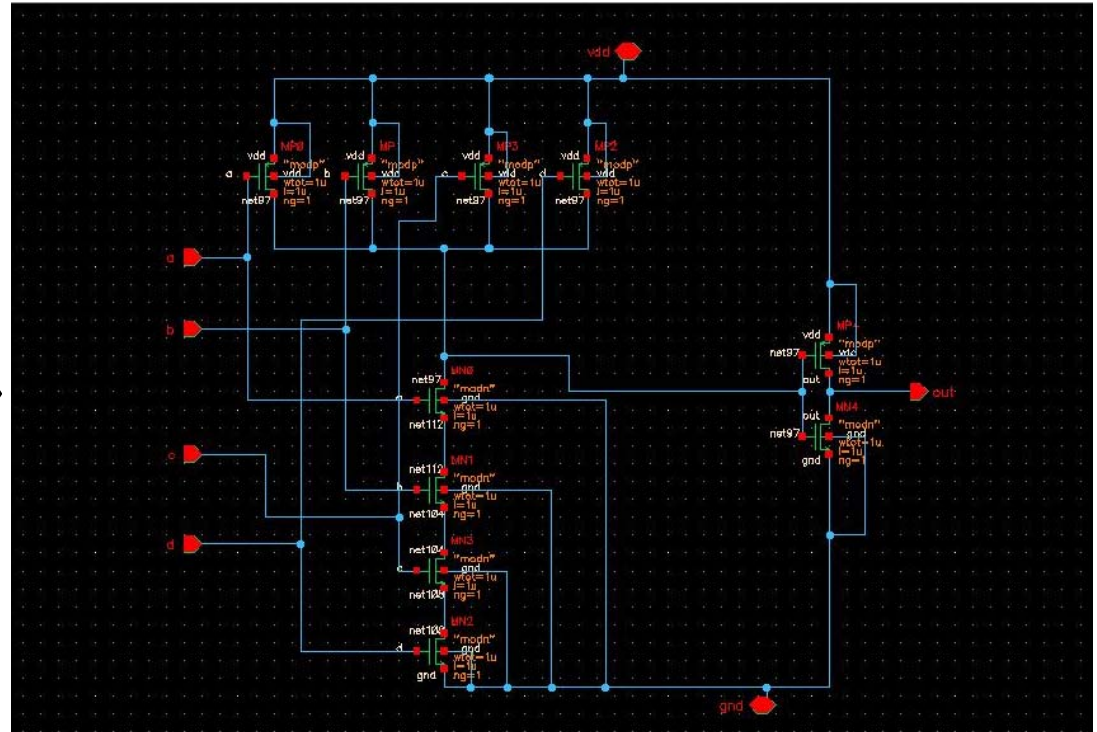
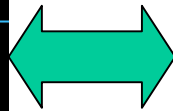
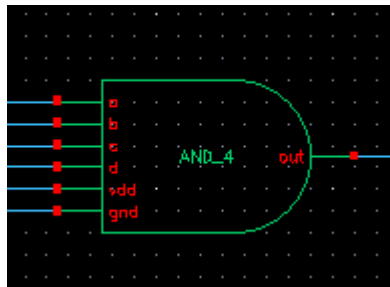
Design Approximations

- The geometrical constraint (area constraint) provided by Global layout designer was $40\mu \times 400\mu$
- Also the plan of including an ADC to the Global layout requires the Decoder design to be made as compact as possible
- The W/L for each transistor is made $1\mu / 1\mu$ for ensuring enough driving strength (to reduce offset of AND4 for 0 at the input)

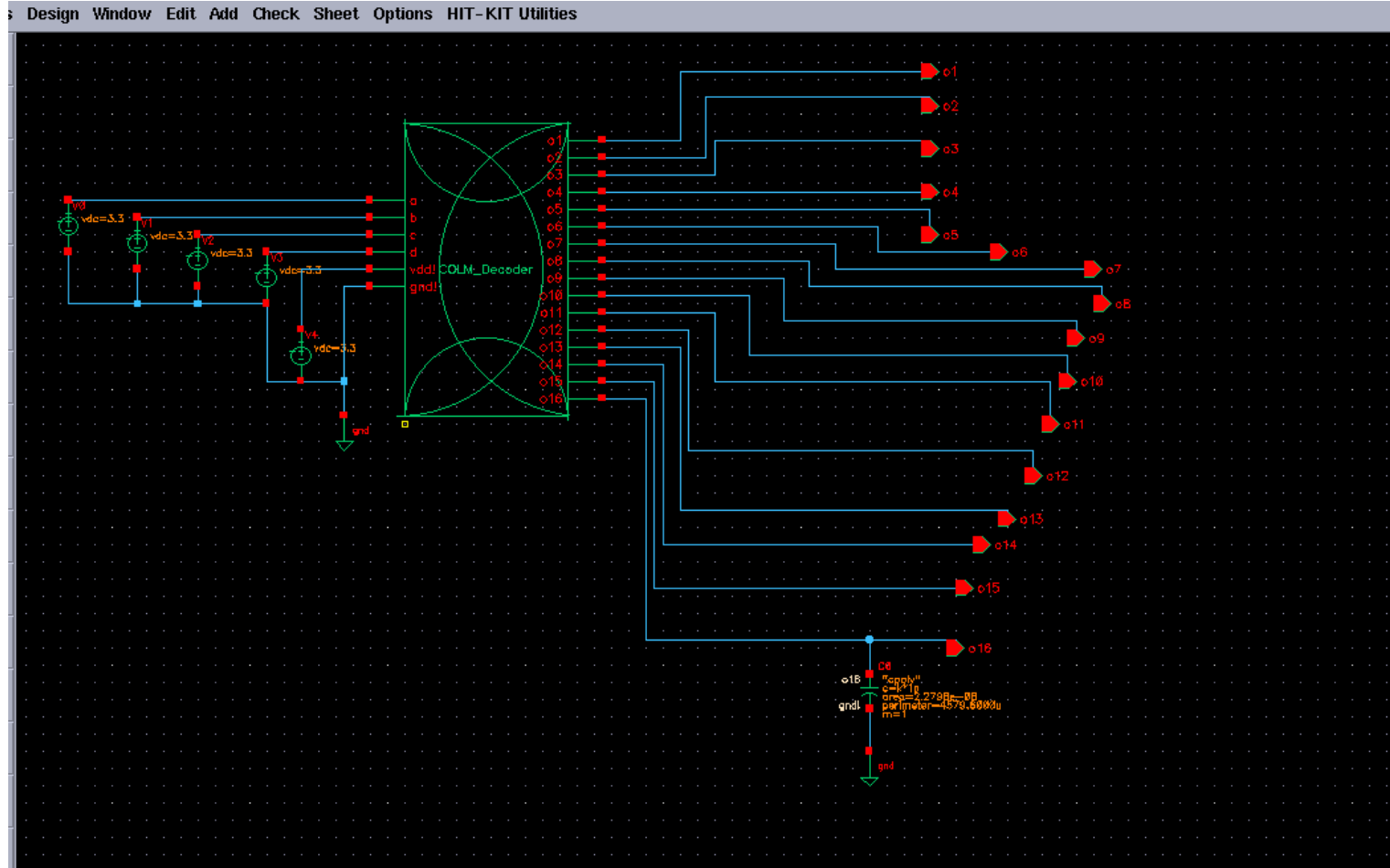
Decoder Design (Schematic)



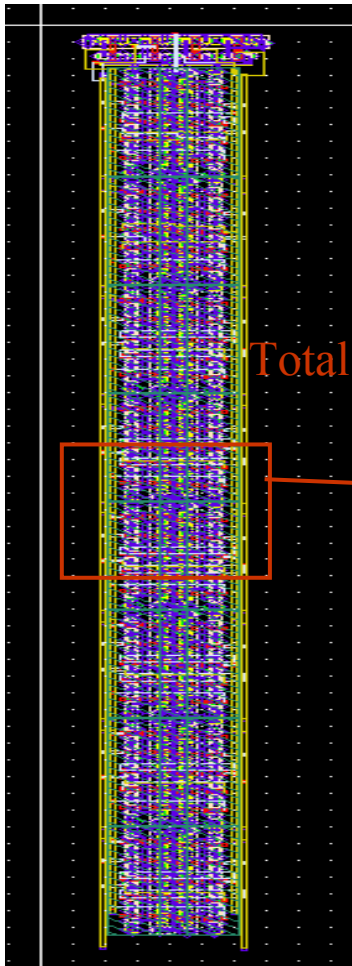
Decoder Schematic (AND4)



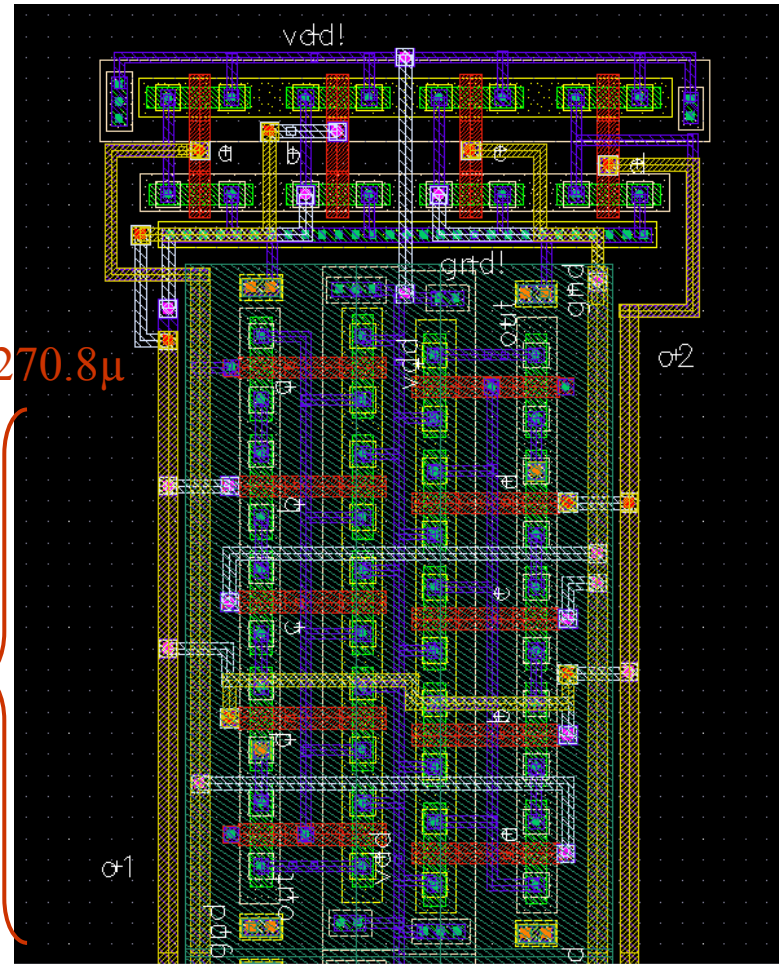
Decoder Simulation Set Up



Decoder Layout



Total area is $30.1\mu \times 270.8\mu$



LVS Check

```
File /export/users/sens9/LVS/si.log
Warning: Unknown device "lat3" on a permuteDevice command.
Warning: Unknown device "vert15" on a permuteDevice command.
Warning: Unknown device "vert10" on a permuteDevice command.
Warning: Unknown device "vert5" on a permuteDevice command.
Warning: Unknown device "pmosm4" on a permuteDevice command.
Warning: Unknown device "rmosmh4" on a permuteDevice command.
Warning: Unknown device "rmosm4" on a permuteDevice command.
Warning: Unknown device "rmosh6" on a permuteDevice command.
Warning: Unknown device "rmosh4" on a permuteDevice command.
Warning: Unknown device "ng" on a permuteDevice command.
Warning: Unknown device "cvar" on a permuteDevice command.
Warning: Unknown device "csandwt" on a permuteDevice command.
Warning: Unknown device "cpoly" on a permuteDevice command.
Warning: Unknown device "zd2sm24" on a permuteDevice command.
Warning: Unknown device "pd" on a permuteDevice command.
Warning: Unknown device "nwd" on a permuteDevice command.
Warning: Unknown device "nd" on a permuteDevice command.

The net-lists match.

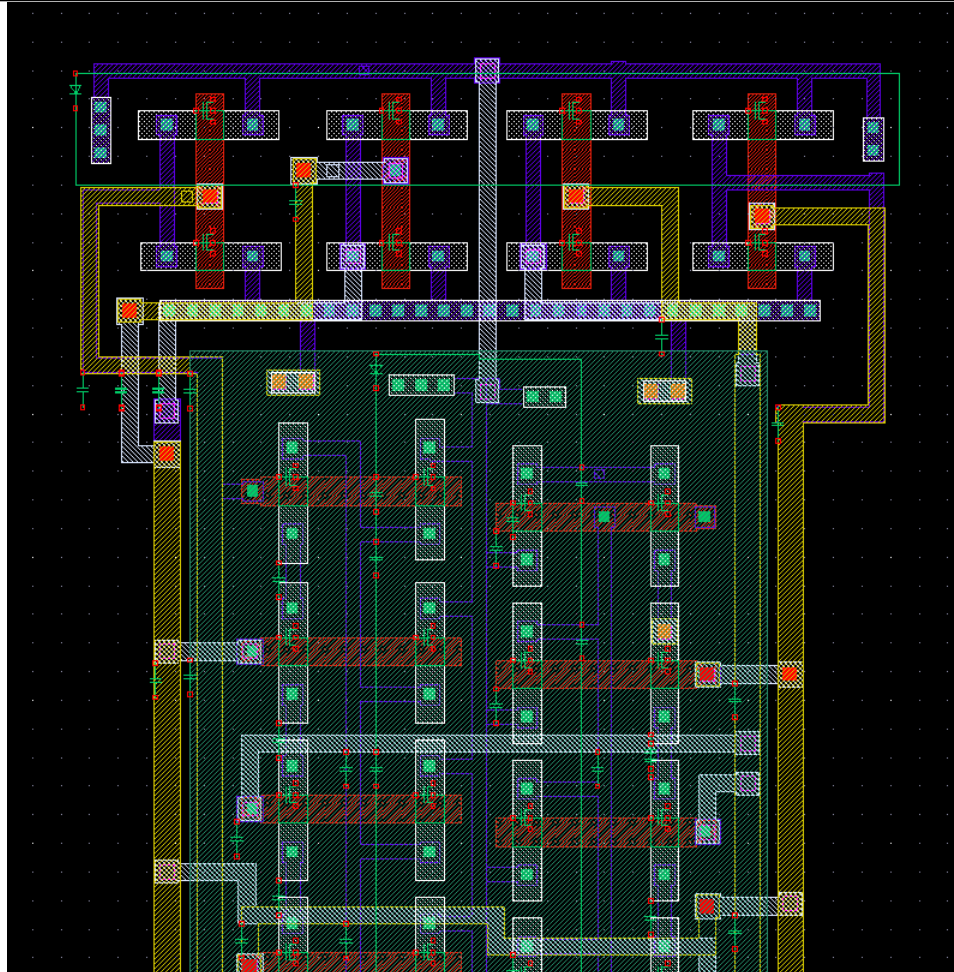
                layout schematic
                instances
un-matched          0      0
rewired             0      0
size errors         0      0
pruned              0      0
active              168    168
total                168    168

                nets
un-matched          0      0
merged              0      0
pruned              0      0
active              90     90
total                90     90

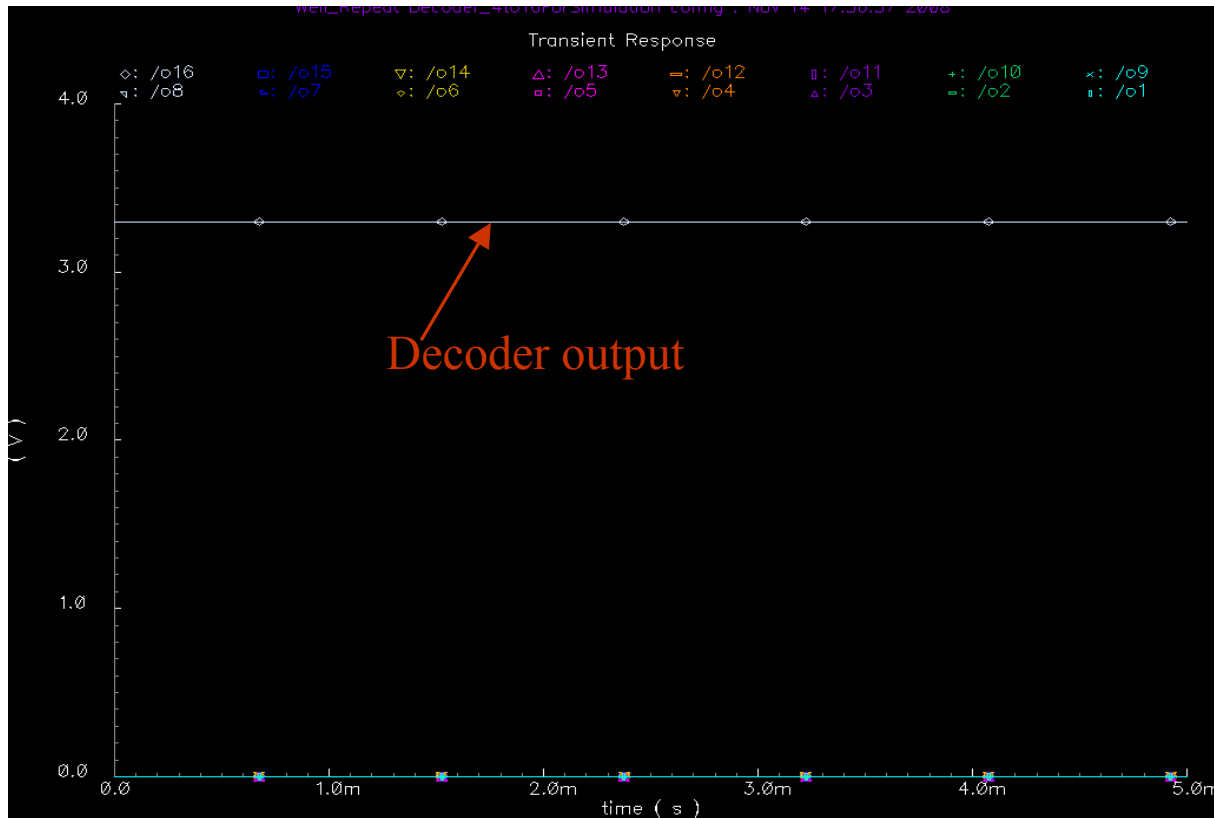
                terminals
un-matched          0      0
matched but
different type      0      0
total                22     22
End comparison:      Nov 14 17:14:34 2008

Comparison program completed successfully.
```

Decoder Extracted View

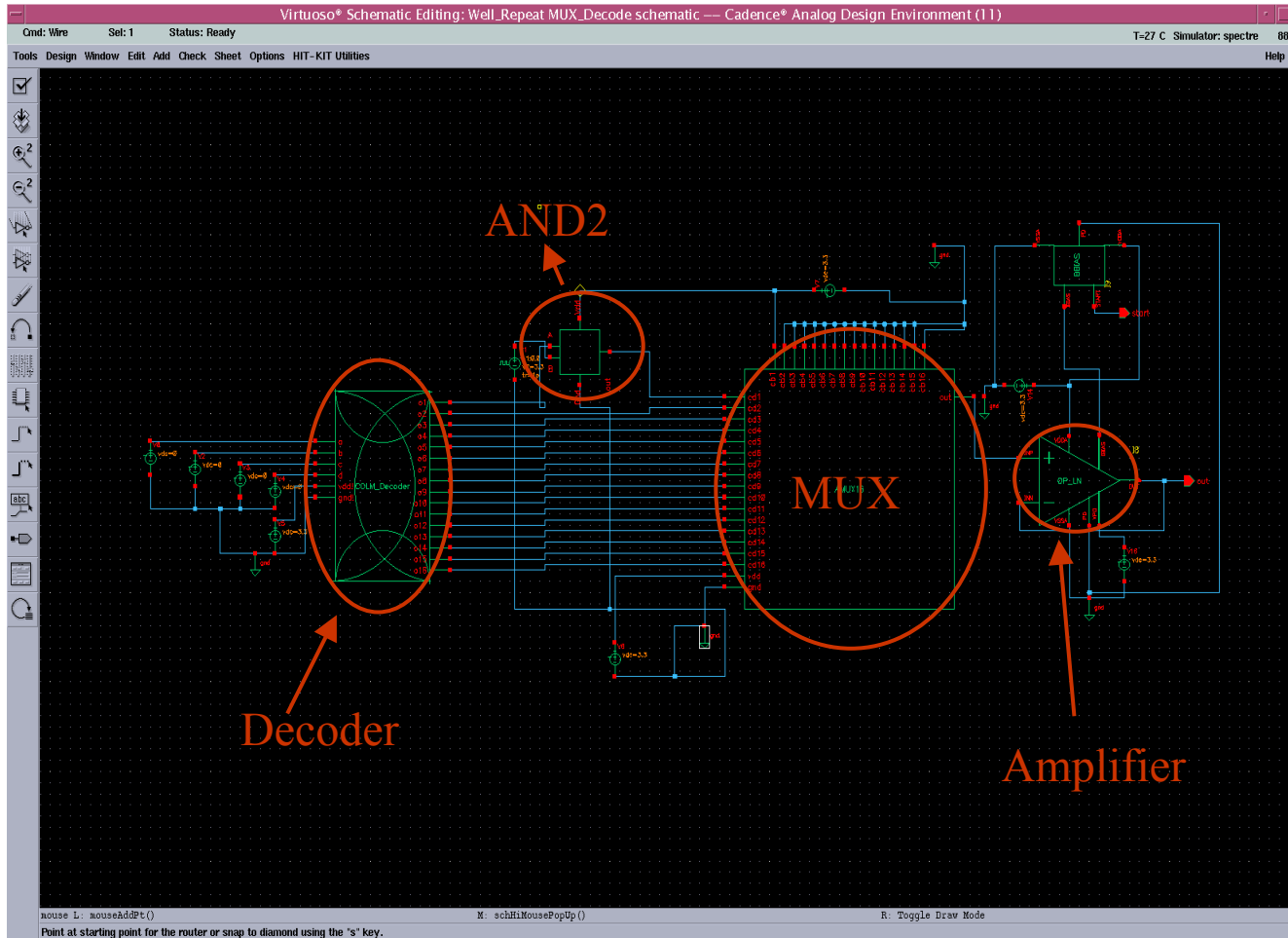


Decoder Simulation (Extracted)

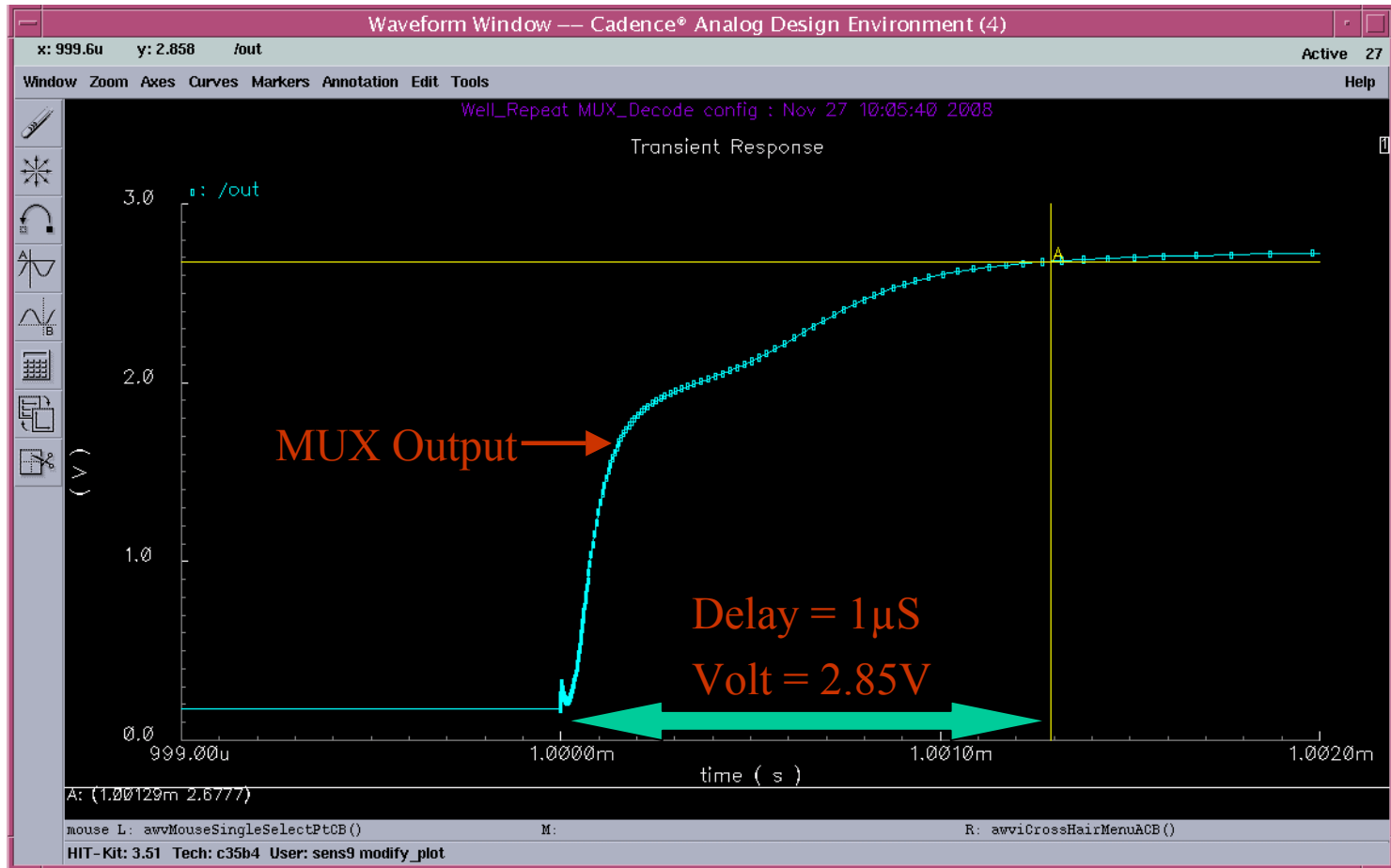


Out put at 16th output pin

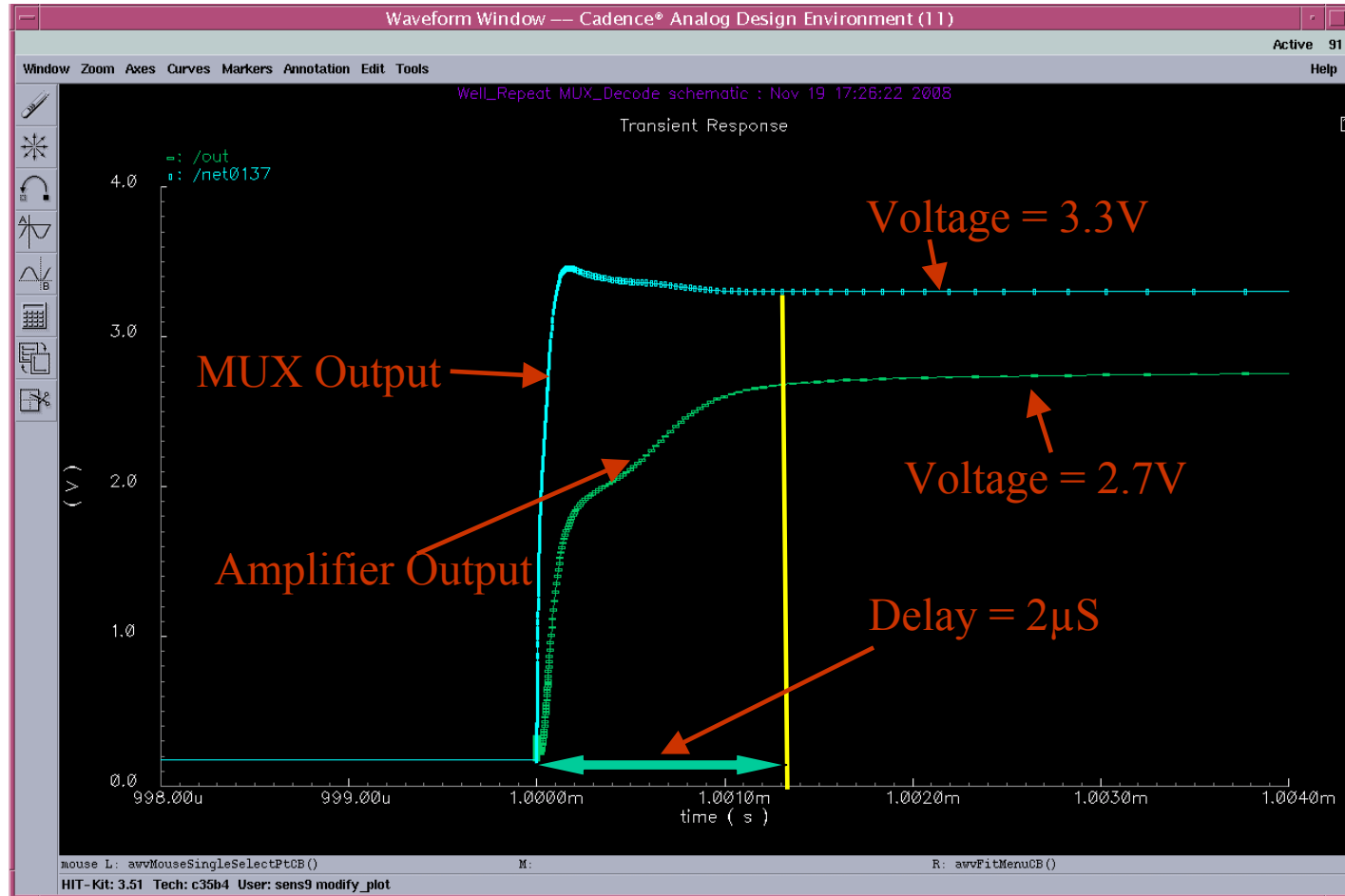
Delay analysis (Schematic)



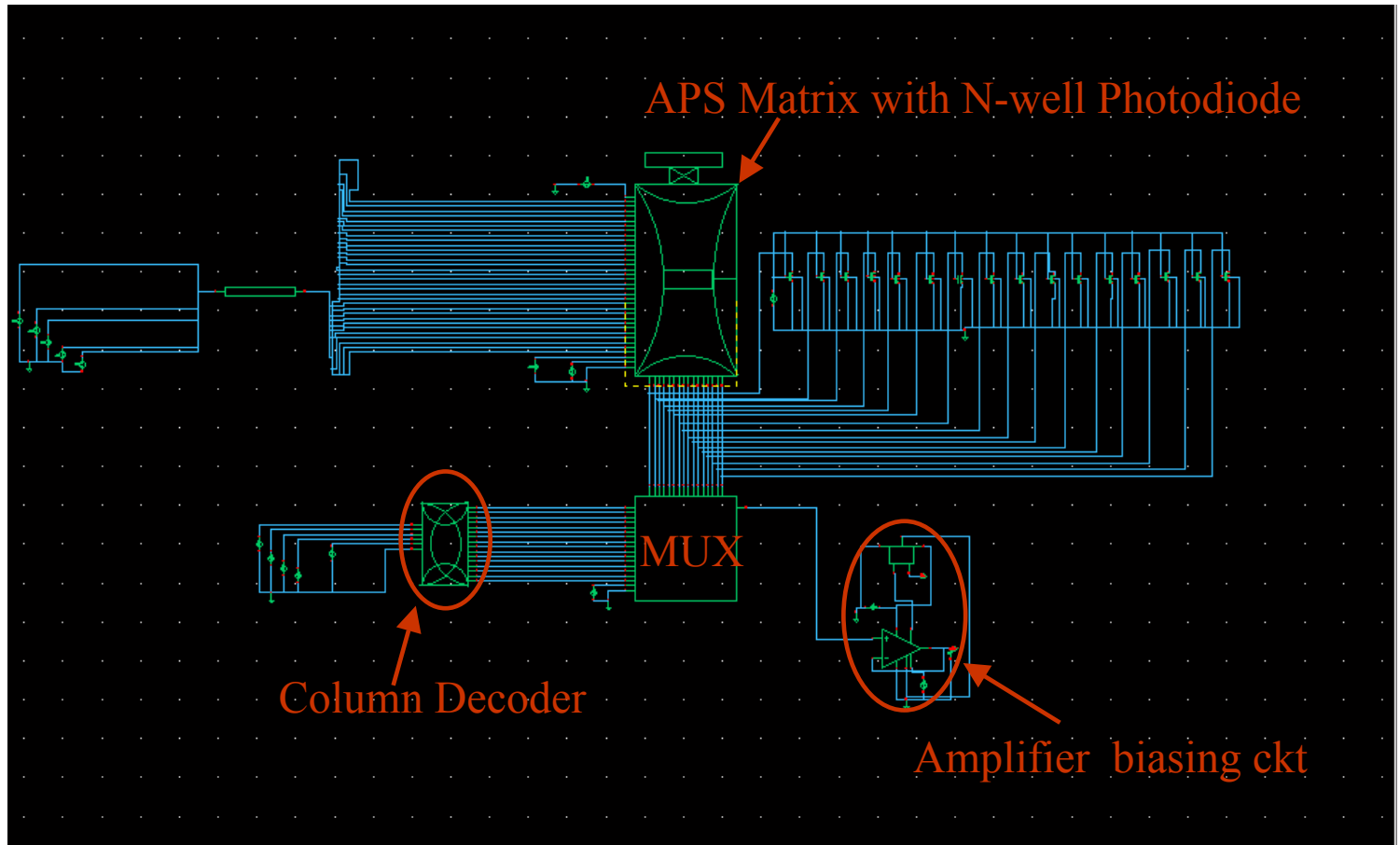
Simulation with a Load Capacitance (C=0pF)



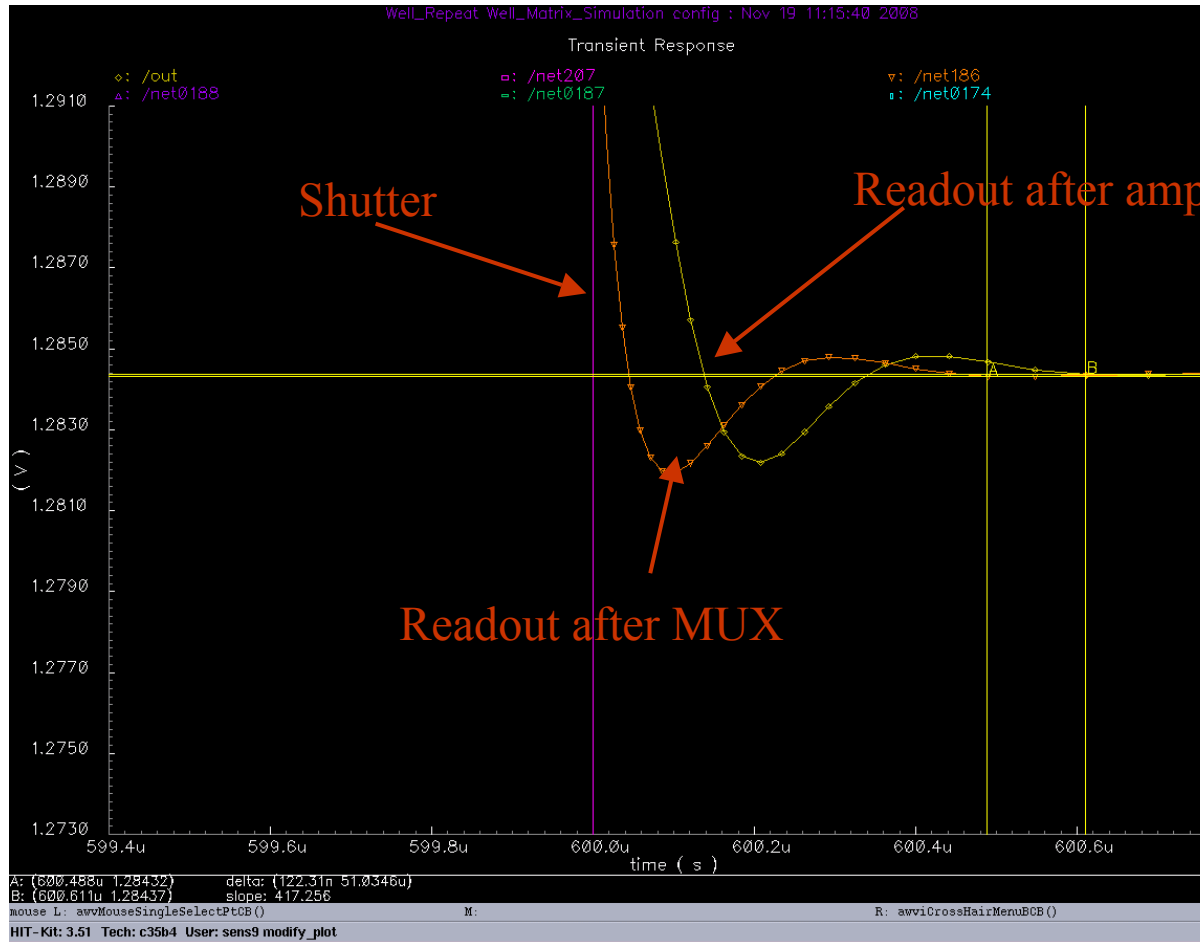
Simulation with a Load Capacitance (C=15pF)



APS Matrix simulation with MUX & Decoder (Schematic)

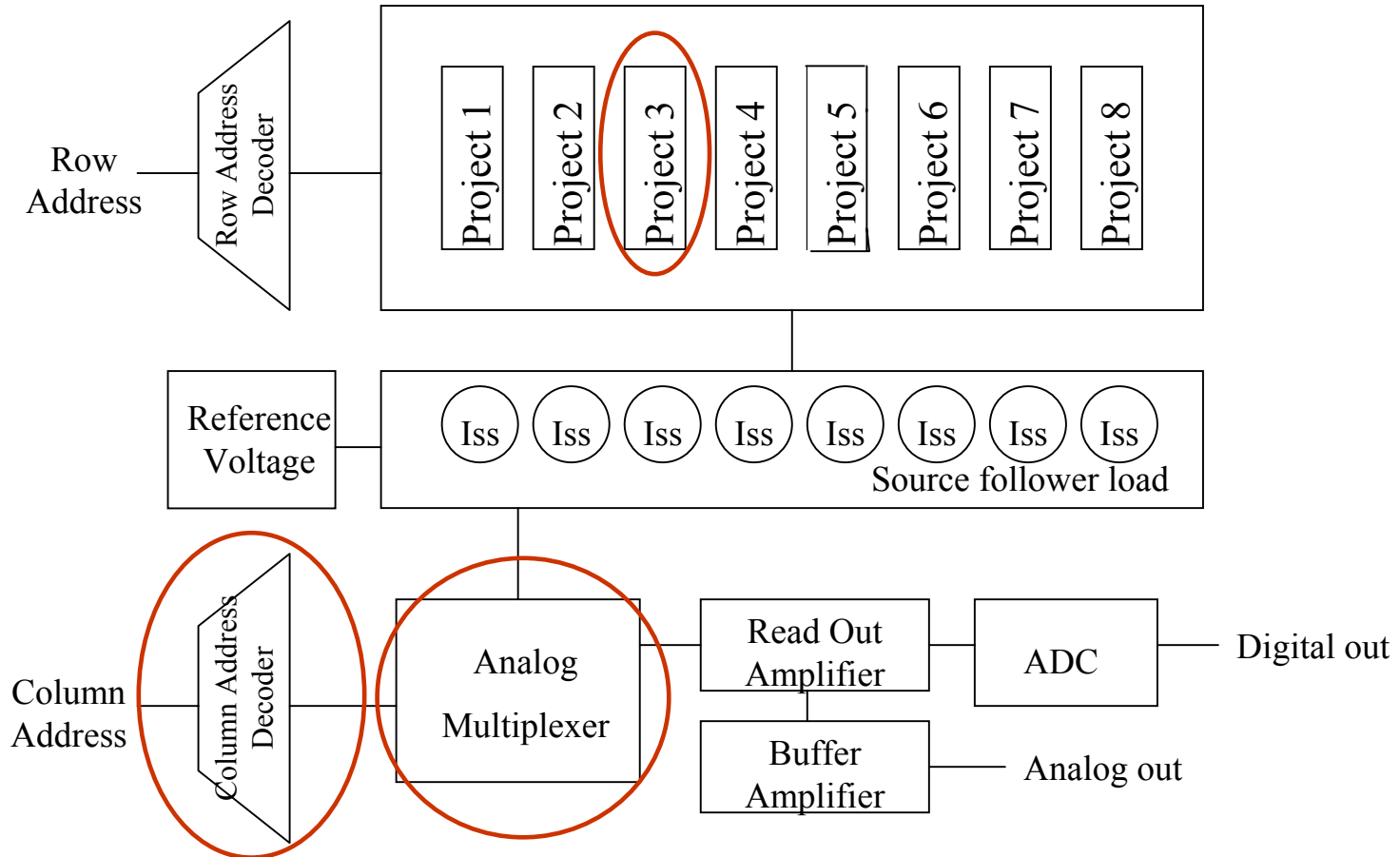


APS matrix Readout time measurement (Extracted)

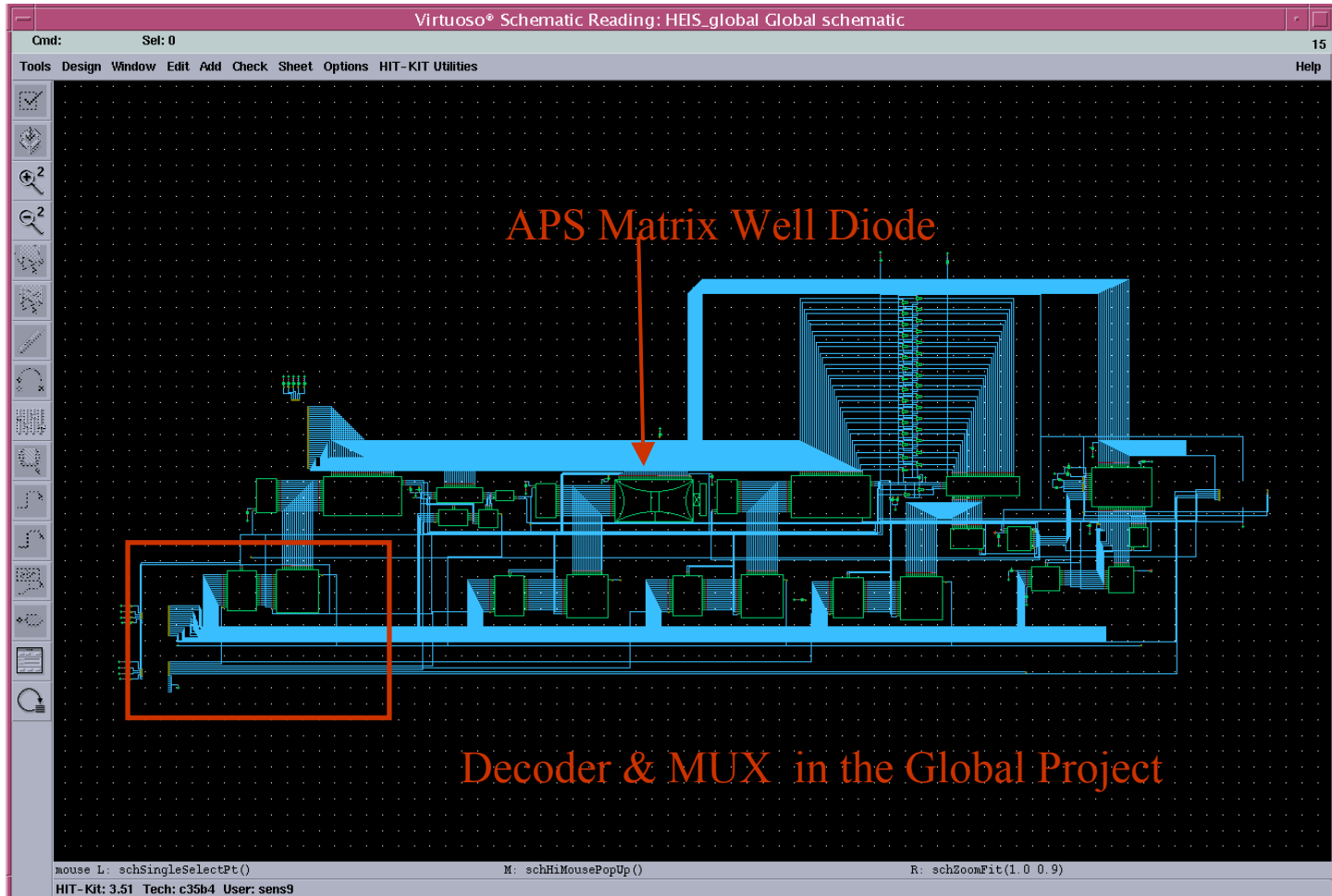


Readout time
After MUX=500nS
After Amp =600nS

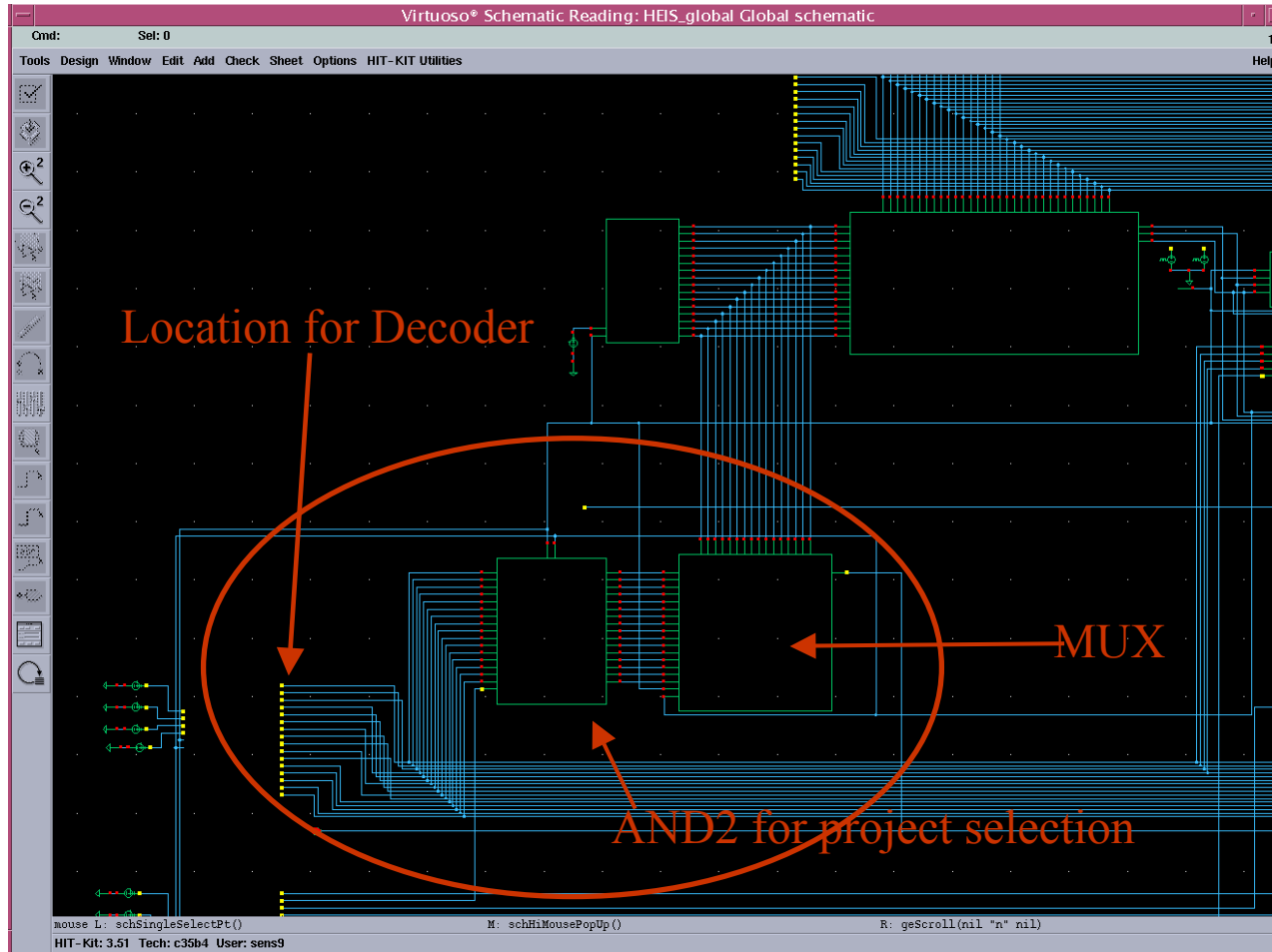
Global Project



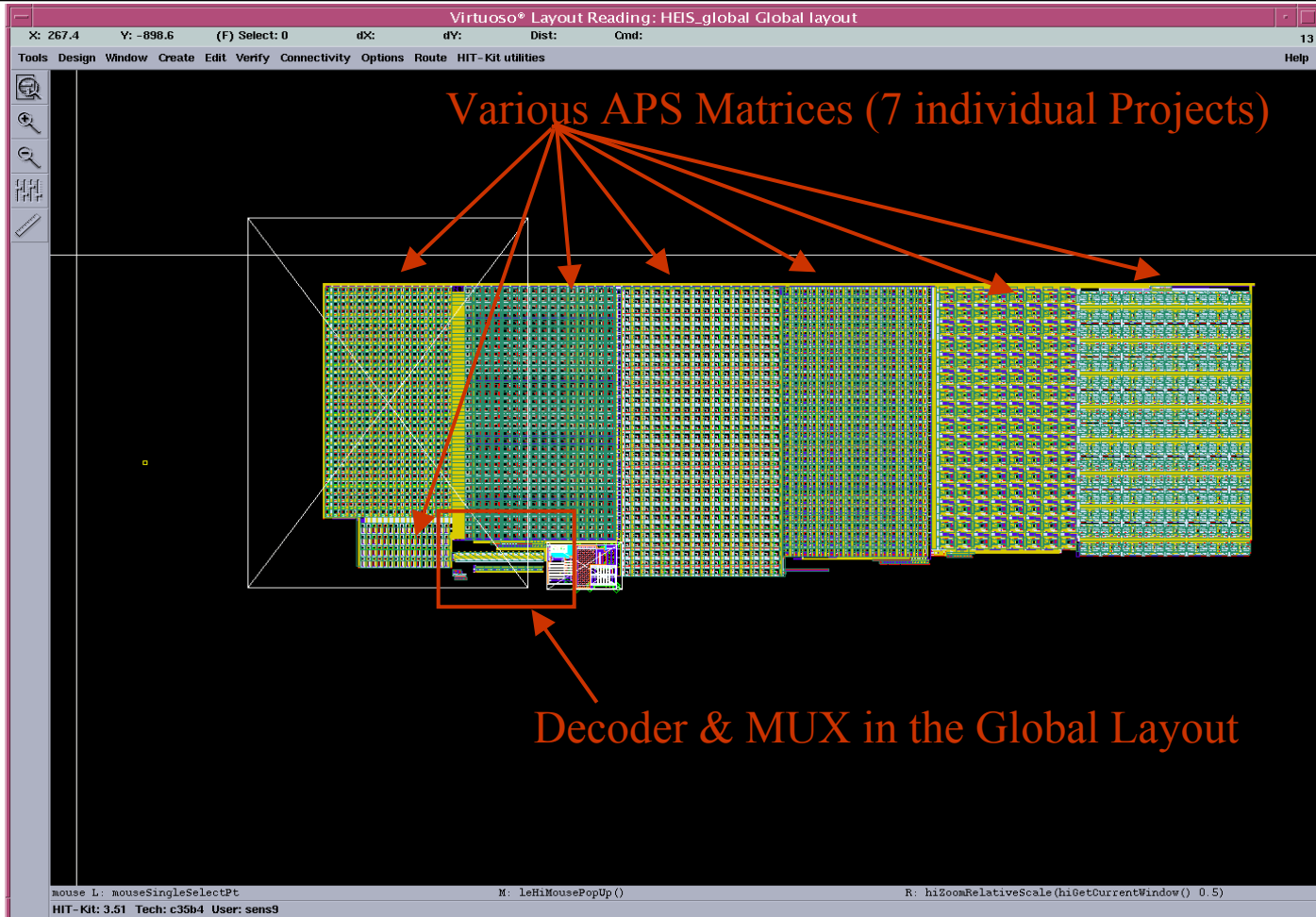
Global Project (Schematic)



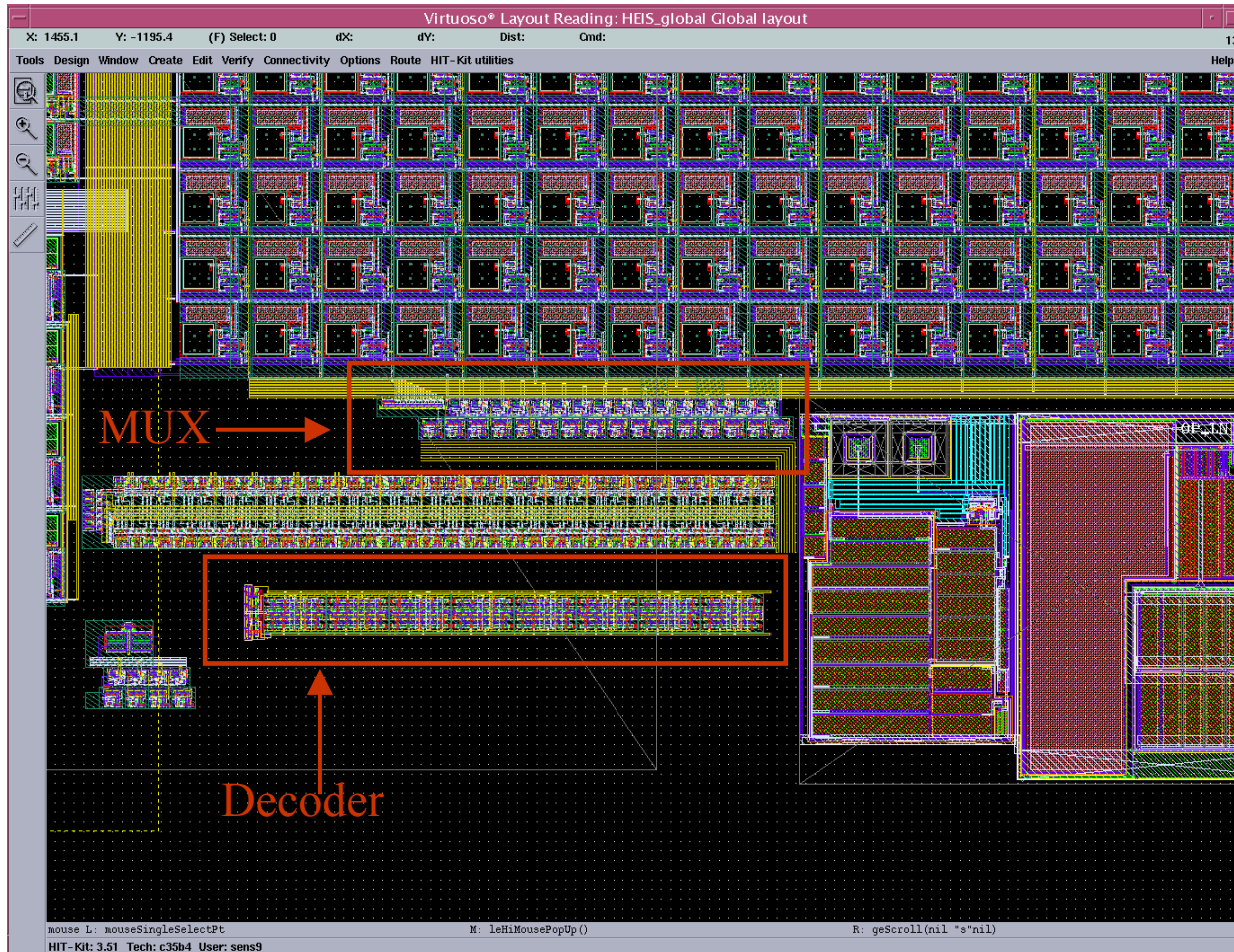
Global Project (Schematic)



Global Project (Layout)



Global Project (Layout)



Results

- Column Decoder & Analog MUX are successfully designed and tested with an APS matrix
- Readout time obtained are, 500nS (after MUX) & 600nS (after Amplifier)
- Total design area for MUX is $11.4\mu \times 173.7\mu$
- Total Design area for Decoder is $30.1\mu \times 270.8\mu$
- Delay for the switching from 0 to 3.3V for MUX & Decoder are $1\mu\text{S}$ and $2\mu\text{S}$ respectively
- Approximate Frame rate obtained is 270.12 FPS
- Output voltage = 1.18V (for $I_{\text{photo}}=500\text{pA}$)

Conclusion

- An analog MUX and Column Decoder are successfully designed for effective use in APS sensor Readout
- Readout time obtained by inclusion of the designed components are almost same as the results obtained by using standard cells for simulation.
- Aspect ratios are kept $1\mu/1\mu$ in Decoder design in order to save area (for inclusion of ADC in the global layout)
- A better and compact designing may be obtained by careful placing and routing of the components at the cost of increase in area and delay

Reference

- Lecture slides of HEIS and TESYS by Prof. Andreas Koenig (TU Kaiserslautern)
- Lecture slides from Harvey Mudd College (Introduction to CMOS VLSI Design)
- Digital Integrated Circuits, Jan M. Rabaey
- www.wikipedia.org

MUX & Decoder Design

Thank You For Your Attention !