TECHNISCHE UNIVERSITÄT KAISERSLAUTERN

Institute of
Cognitive Integrated Sensor Systems

Department of Electrical and Computer Engineering

Semester Project in TESYS, 2022

3-bit Flash Analogue to Digital Converter Design and Layout in XFAB 0.35 um CMOS Technology'

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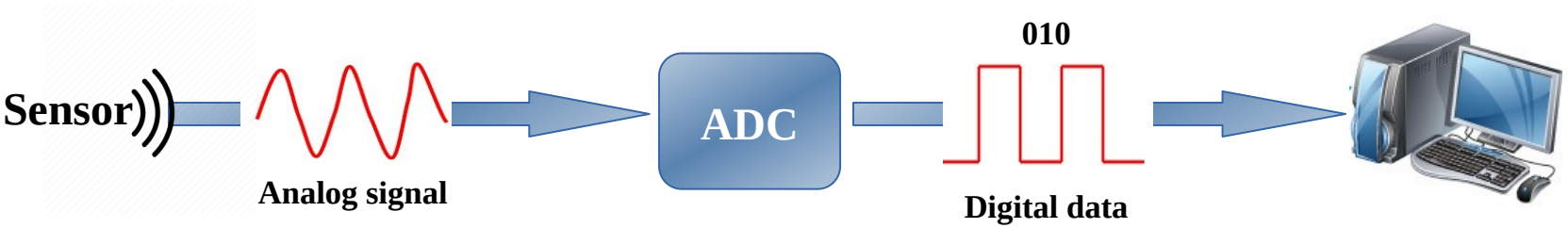
Outline

1. Introduction
   - *Motivation*
2. Parts of the Project
   - ✓ *Amira Ghezal* -*Chip floor-plan and top-level hierarchical layout*
     -*Comparator and Bias circuit layouts*
   - ✓ *Jad Halabi* -*Matched resistor: design and layout*
   - ✓ *Anand Joshy* -*Logic gates design and layout*
   - ✓ *Kamal Baghirli* -*Encoder design and layout using Logic gates*
3. Conclusion

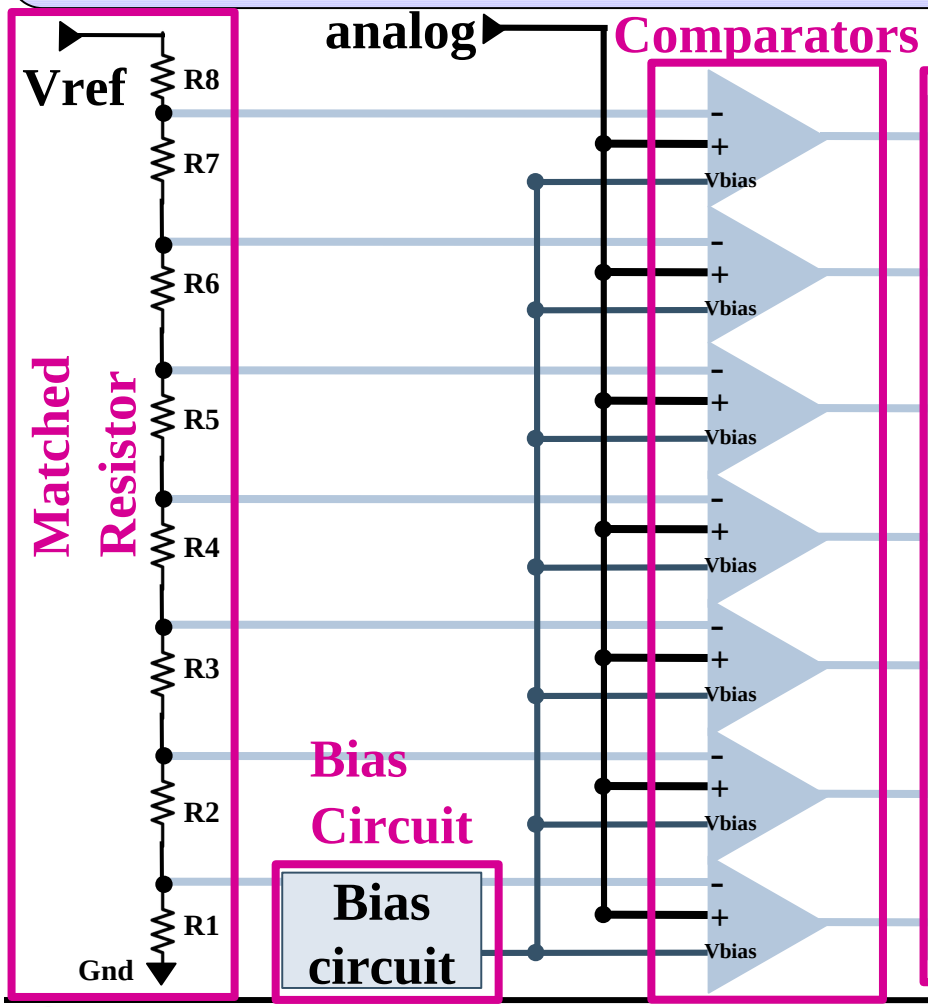
Motivation

- Analog signals are often fed into the computing systems for processing.
- As the computers can only handle digital data, there is a need to convert the analog data to a digital one.
- This project designs a Flash converter, which converts one word at a time (3-bit word in this case).



Parts of Project

Block diagram of a 3-Bit Flash ADC



A 3-bit flash ADC consists of:

- ✓ 2^{N-1} comparators: 7comparators
- ✓ 2^{N} number of matched resistors: 8 resistors
- ✓ An encoder

1. Matched Resistor

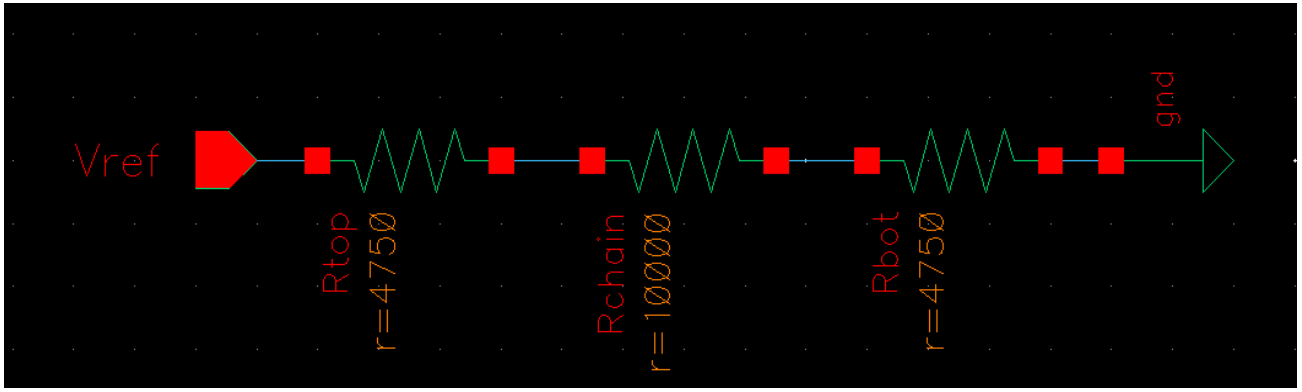
- Function: Provide fixed voltage levels to which an analog signal from a sensor will be compared
- Sensor output: 0~2V
- Comparator specification: CMR-/+=0.85 from supply rails with vdd=3.3V, which means the comparator works dependably in the range [0.8, 2.5V]
- The sensor and comparator working range did not match
- The best solution was to go back to the comparator design and extract new parameters for transistor widths
- We decided on an adhoc solution (next slide) because of time limitations

1. Matched Resistor

- The adhoc solution was to modify the matched resistor to alter the reference voltages in a way that matches the CMR of the comparators

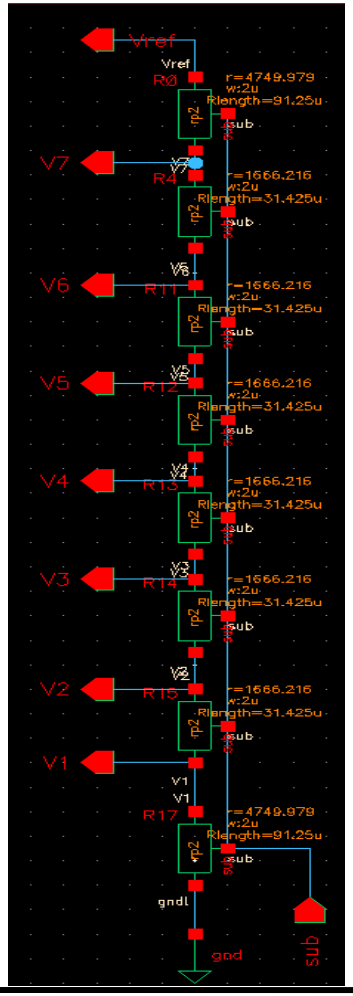
  ➡ Effects the full scale voltage (FSV)

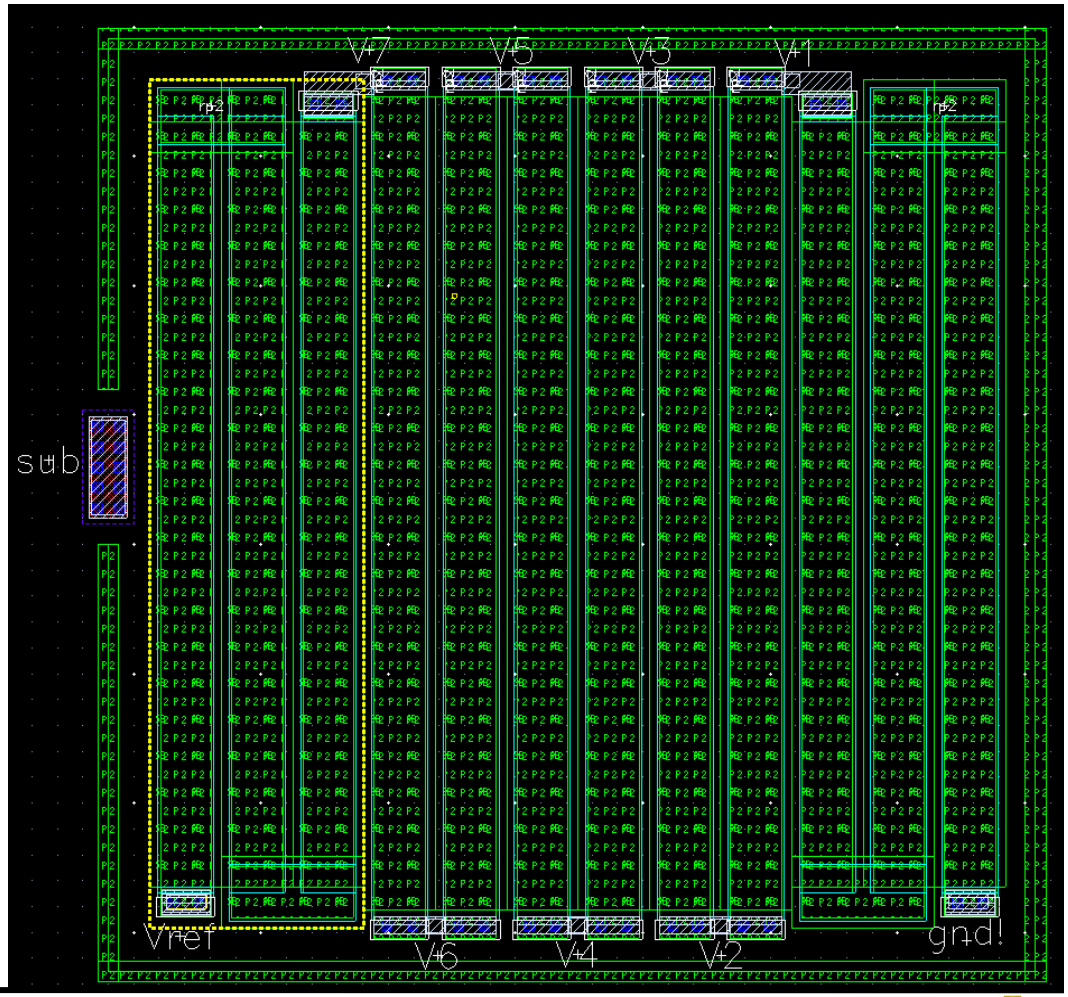
- The resistor chain was designed with two large resistors at the top and bottom of the chain



1. Matched Resistor

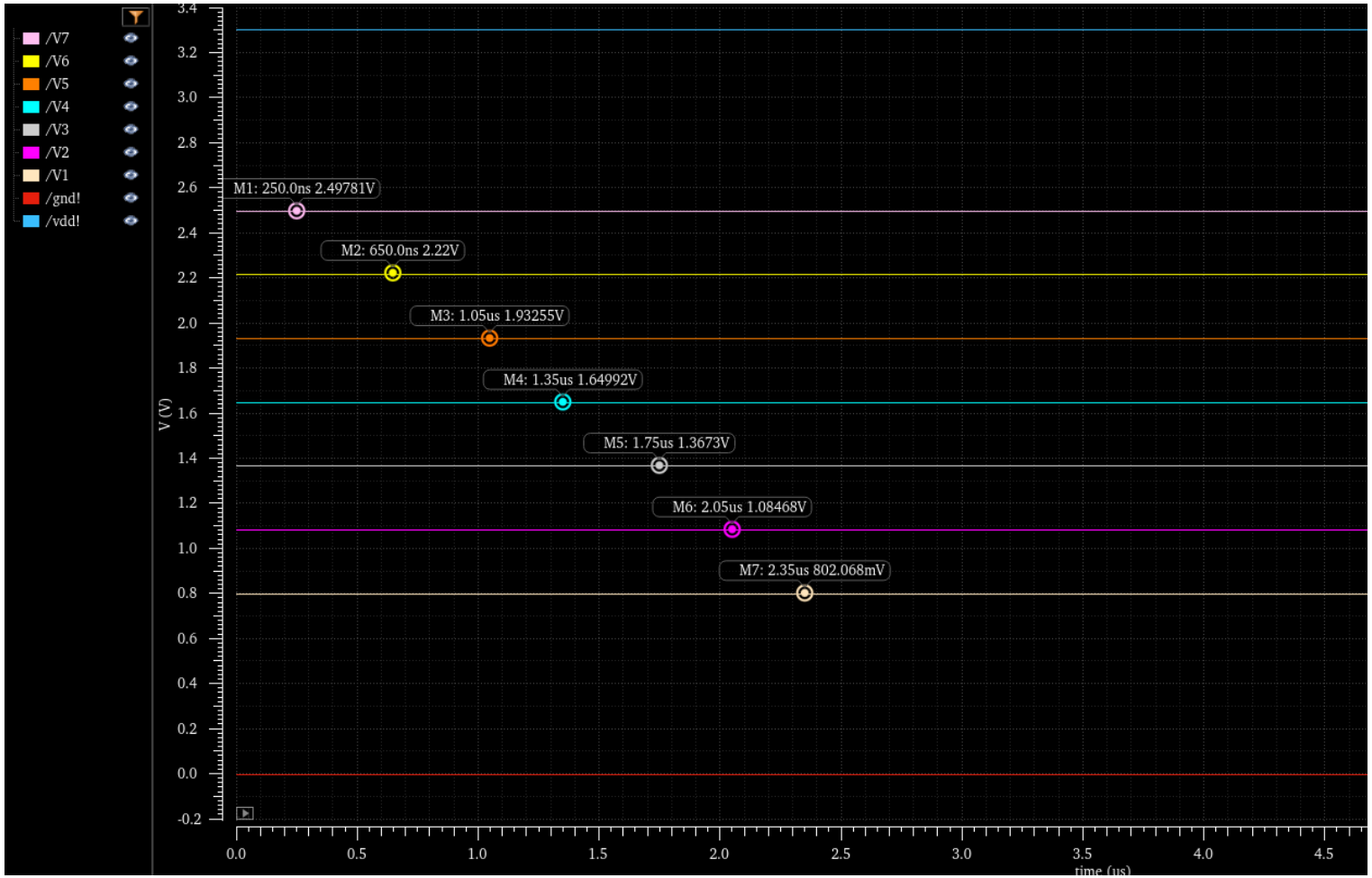
Schematic and Layout





1. Matched Resistor

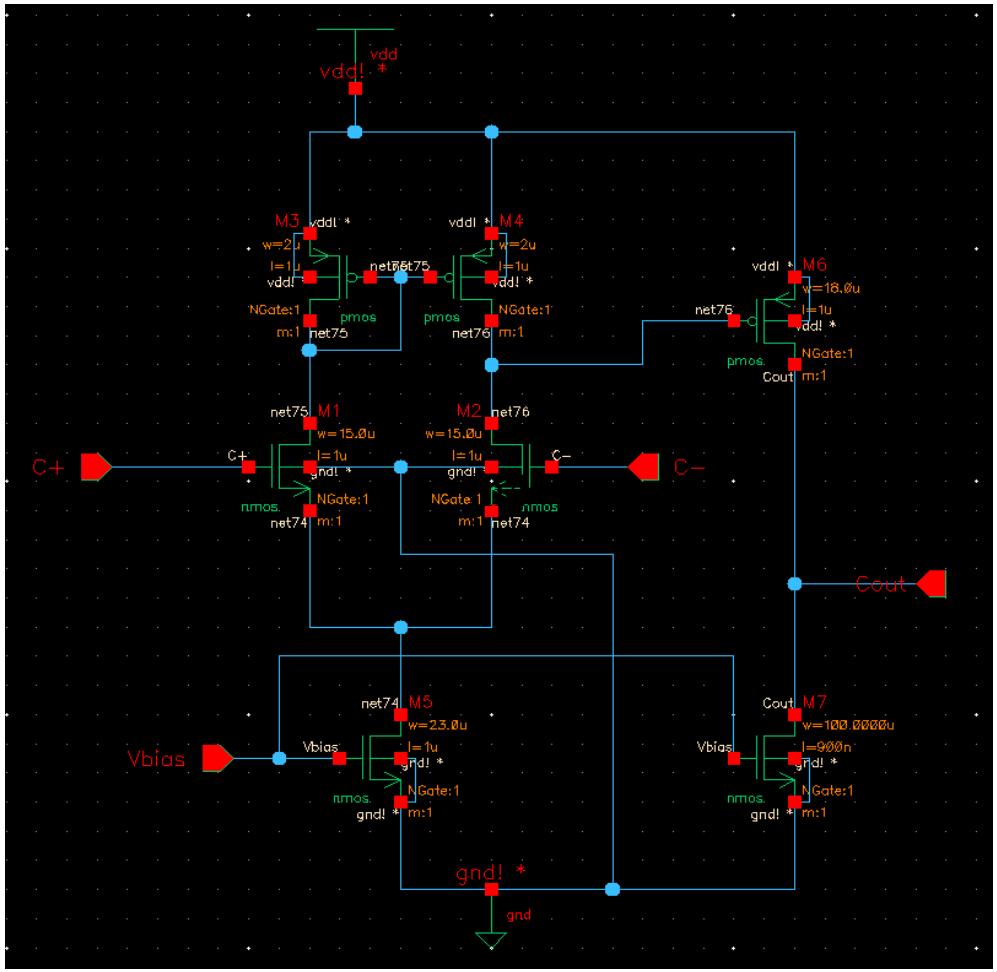
Reference voltage levels



2. Comparator

Schematic

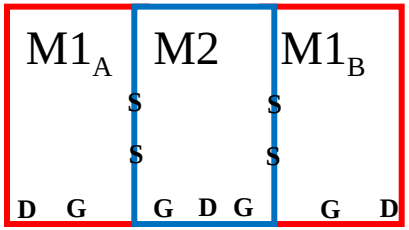
- Two stage comparator
- Transistor ratios are found during the lab session(design steps)



2. Comparator

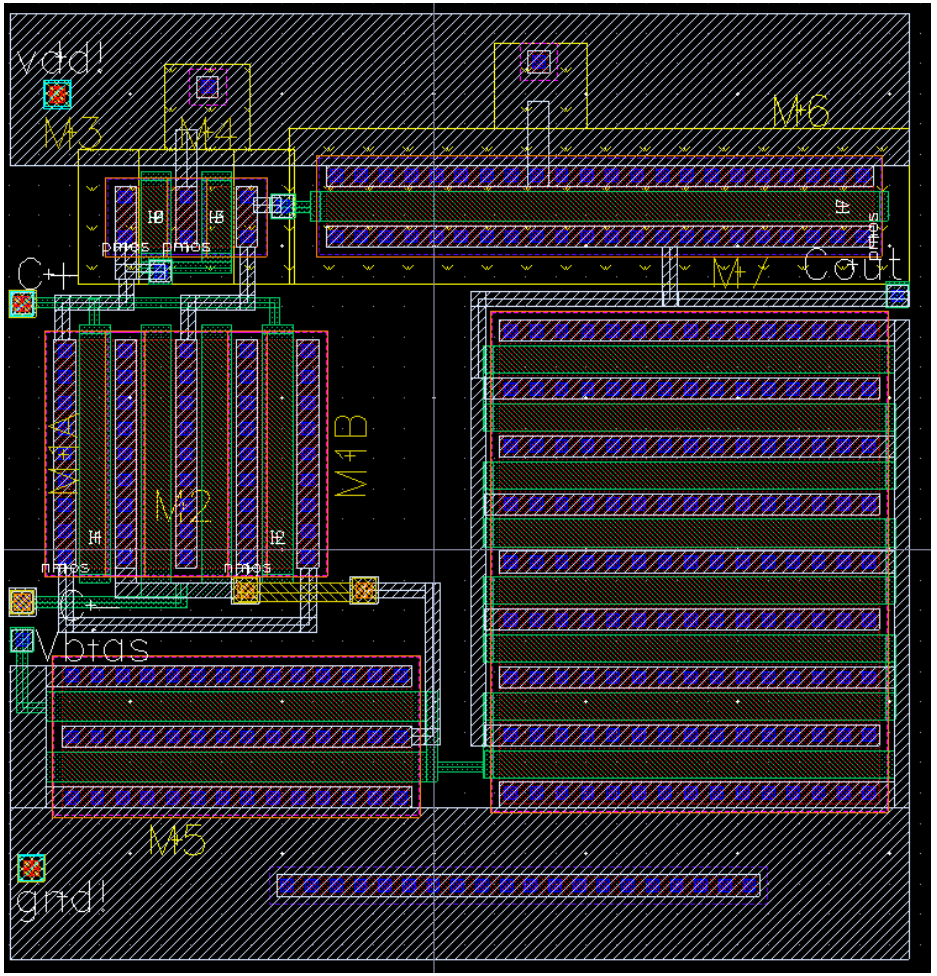
Layout

- **Merging the common source to reduce area**



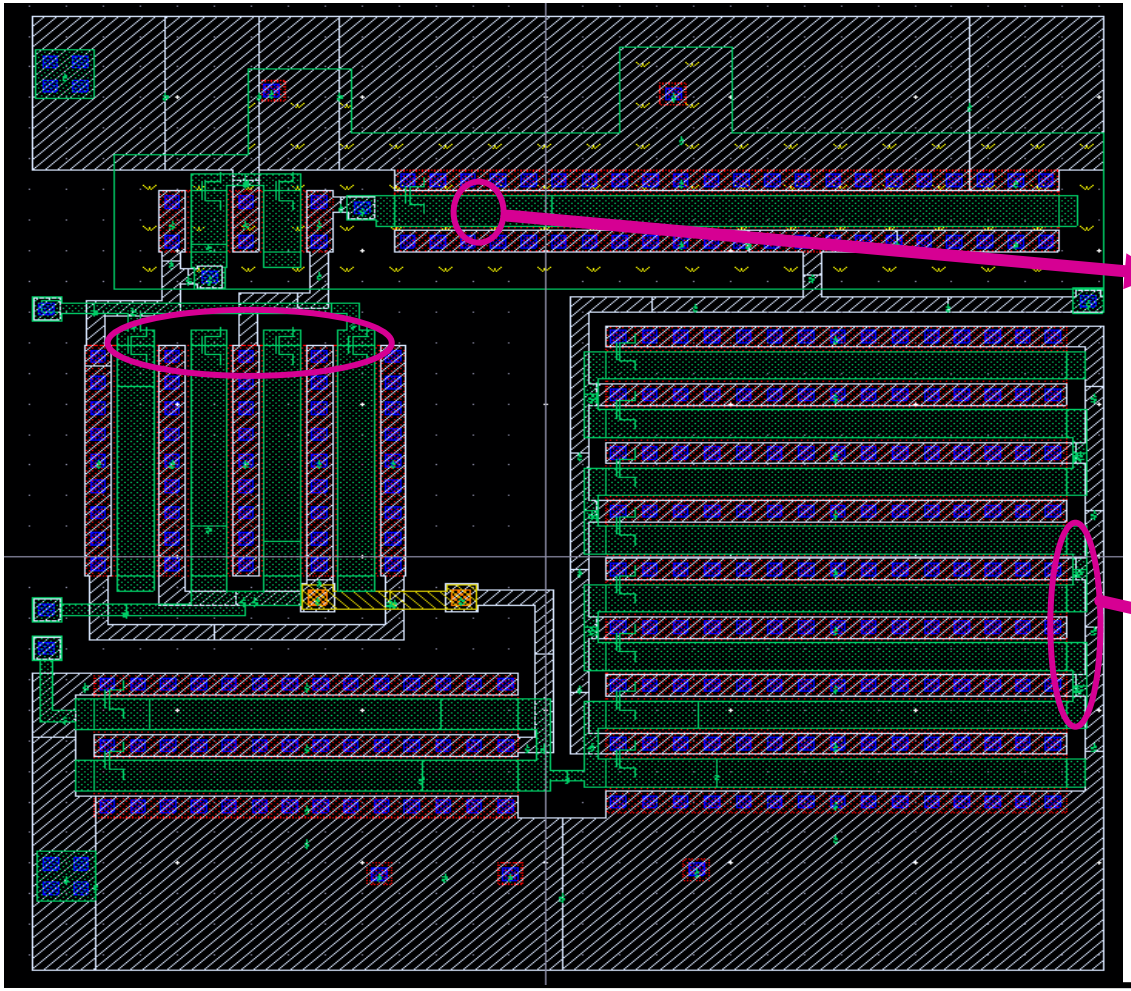
- **Simple interdigitized matching**

➢ More matching rules could be followed to improve the design

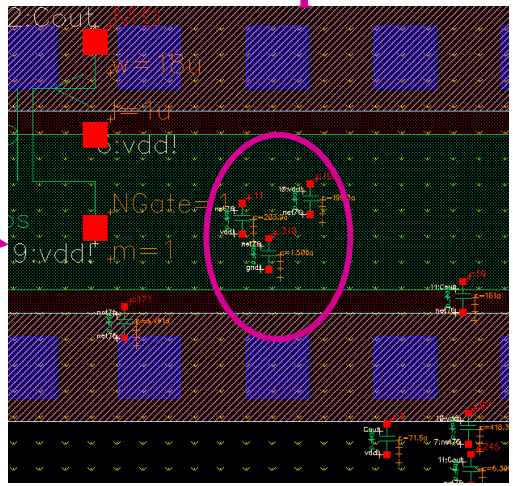


2. Comparator

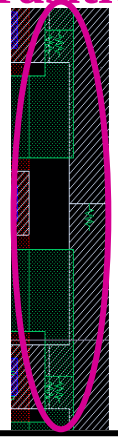
Analogue extracted view



Parasitic capacitor

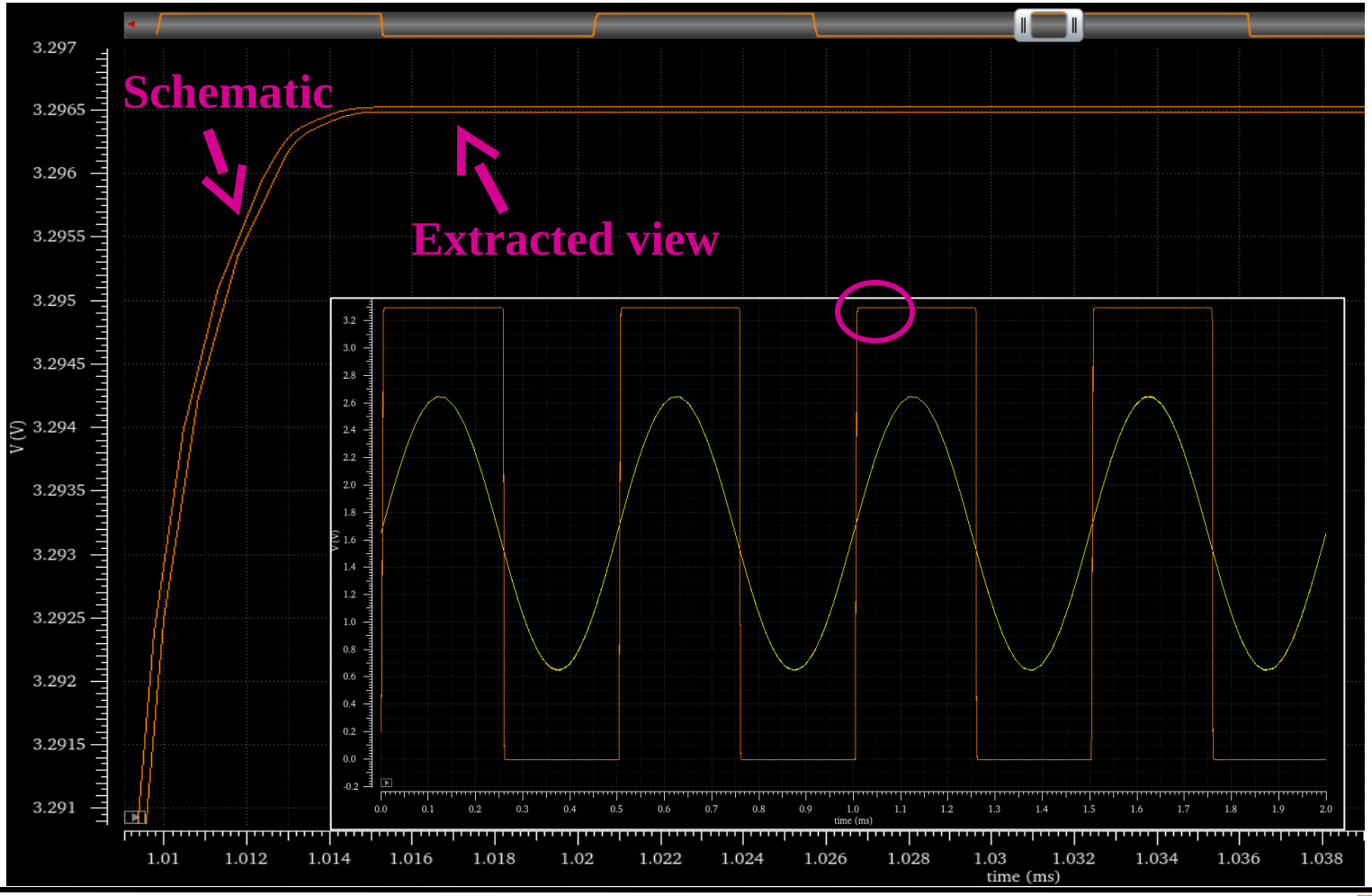


Parasitic resistor



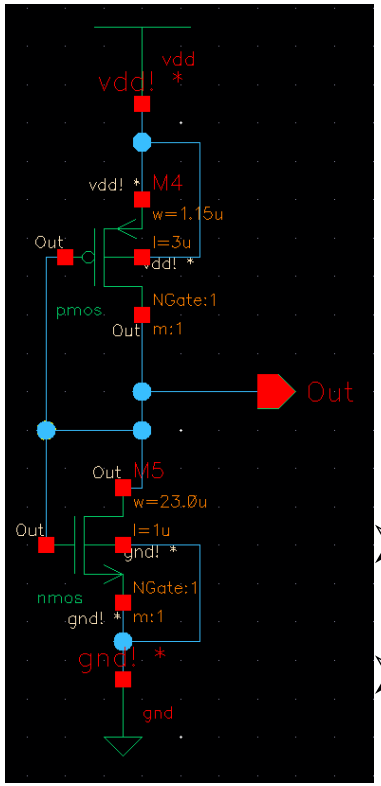
2. Comparator

Transient analysis



3. Bias Circuit

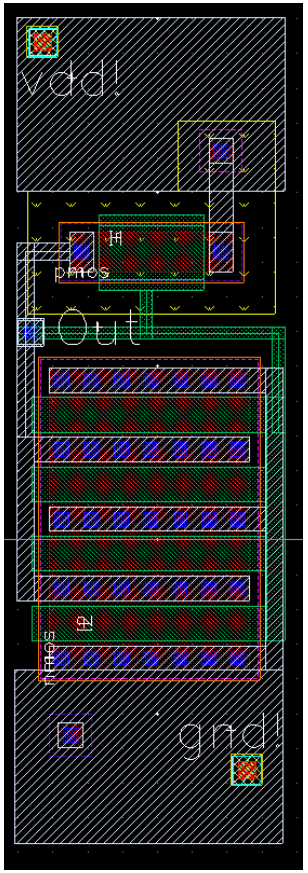
- **Schematic**



Current value Id from schematic	Current value Id from extracted view
NMOS (M5)	NMOS (M5)
20 uA	19.864 uA

- W/L ratio of the transistor M4 has tuned by simulation to achieve 20uA
- One bias cell is enough for the 7 comparators

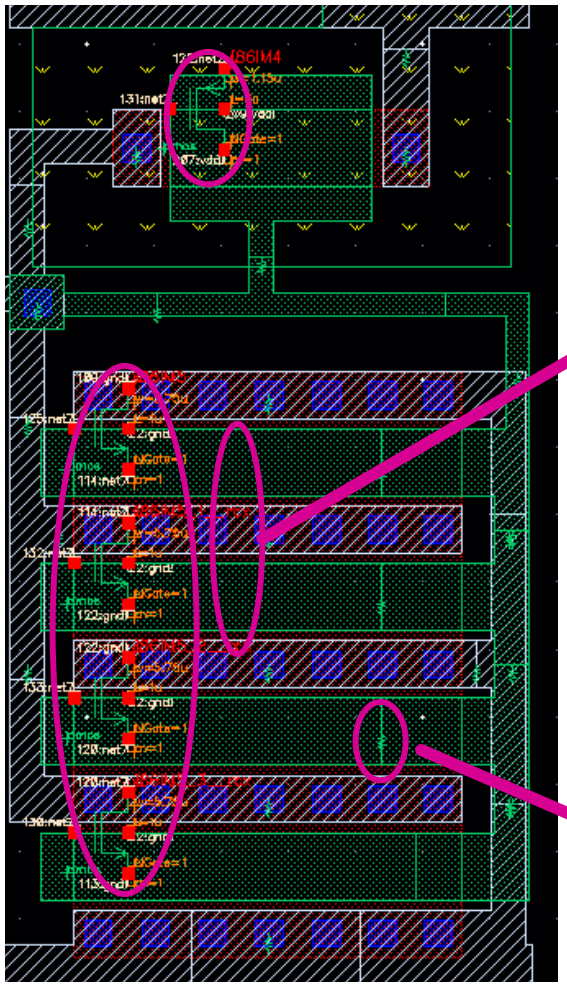
- **Layout**



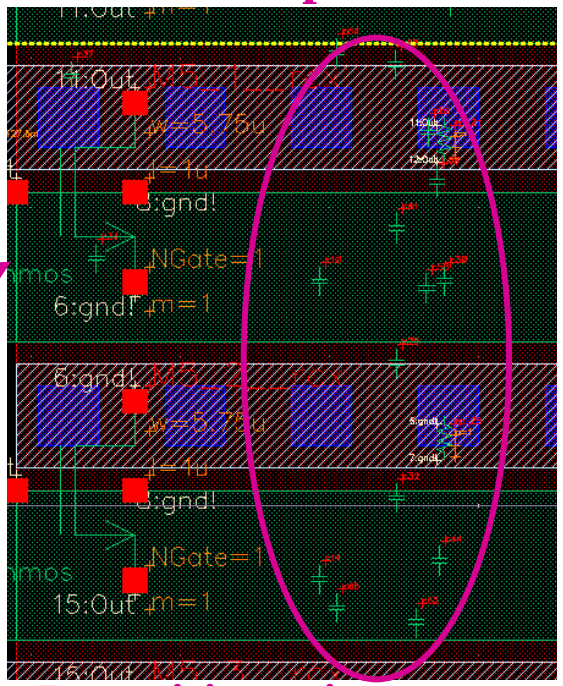
3. Bias Circuit

Analog extracted view

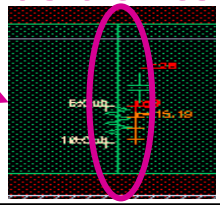
- RC extraction by Xfab values defaults



Parasitic capacitor



Parasitic resistor



4. Logic Gates and Encoder

Realization of encoder

- The behavioral model of the encoder in Verilog should be converted to a physical circuit.
- For this, firstly, the logic gates are created.
- Subsequently, the truth table of the Encoder is extracted, and using the created gates, the schematic and layout are built.
- The following slides follow the above-mentioned steps.

4. Logic Gates and Encoder

Encoder Verilog code implementation

```
//Verilog HDL for "TL22", "Encoder" "functional"


module Encoder (DataIn_i7, DataOut_o3);

  input [6:0] DataIn_i7;
  output [2:0]  DataOut_o3;
  reg    [2:0]  DataOut_o3;

always @(DataIn_i7)
begin
  casex (DataIn_i7)
    8'b1XXXXXX : DataOut_o3 = 7;
    8'b01XXXXX : DataOut_o3 = 6;
    8'b001XXXX : DataOut_o3 = 5;
    8'b0001XXX : DataOut_o3 = 4;
    8'b00001XX : DataOut_o3 = 3;
    8'b000001X : DataOut_o3 = 2;
    8'b0000001 : DataOut_o3 = 1;
    default : DataOut_o3 = 0;
  endcase
end
endmodule
```

4. Logic Gates and Encoder

- Logic gates are used as building blocks to realize the encoder operation.
- Encoder uses of NAND and NOT gates.
- Three different variants of NAND gate is used
  - 4 inputs to 1 output
  - 3 inputs to 1 output
  - 2 inputs to 1 output
- Encoder block, previously modelled using Verilog is illustrated using schematic and layout so as to represent it in manufacturable form.

4. Logic Gates and Encoder

Logic Gates Truth Tables

In1_ nand 4x1	In2_ nand 4x1	In3_ nand 4x1	In4_ nand 4x1	Out_ nand 4x1
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0

In1_ nand 3x1	In2_ nand 3x1	In3_ nand 3x1	Out_ nand 3x1
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

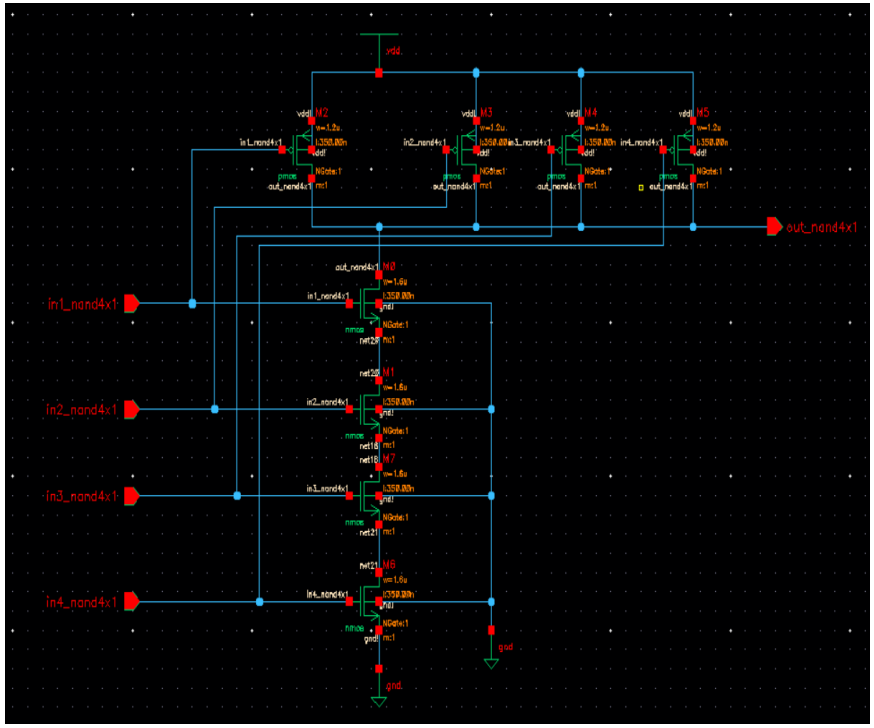
In1_ nand 2x1	In2_ nand 2x1	Out_ nand 2x1
0	0	1
0	1	1
1	0	1
1	1	0

inv_ input0	inv_ output
0	1
1	0

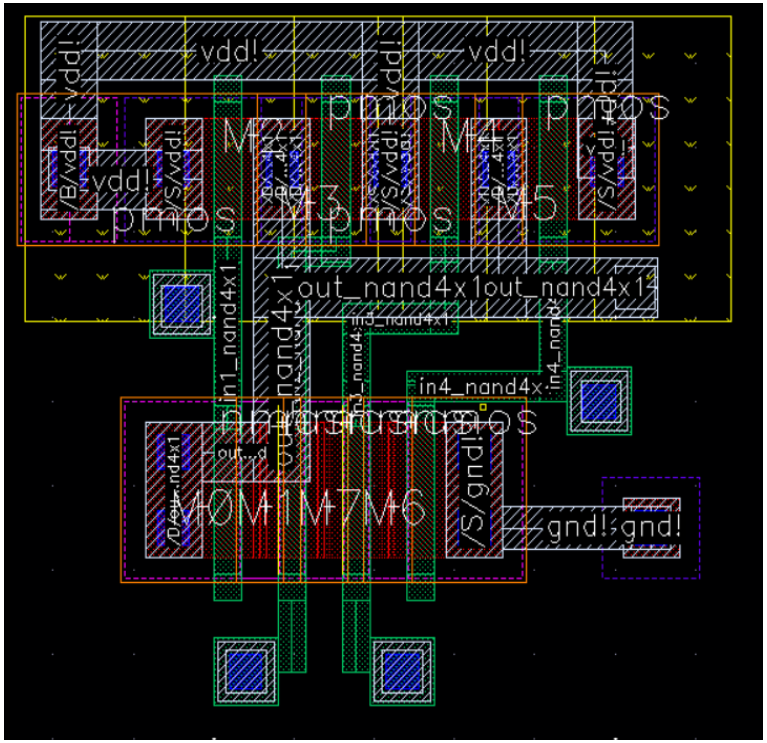
4. Logic Gates and Encoder

NAND4x1

- **Schematic**



- **Layout**



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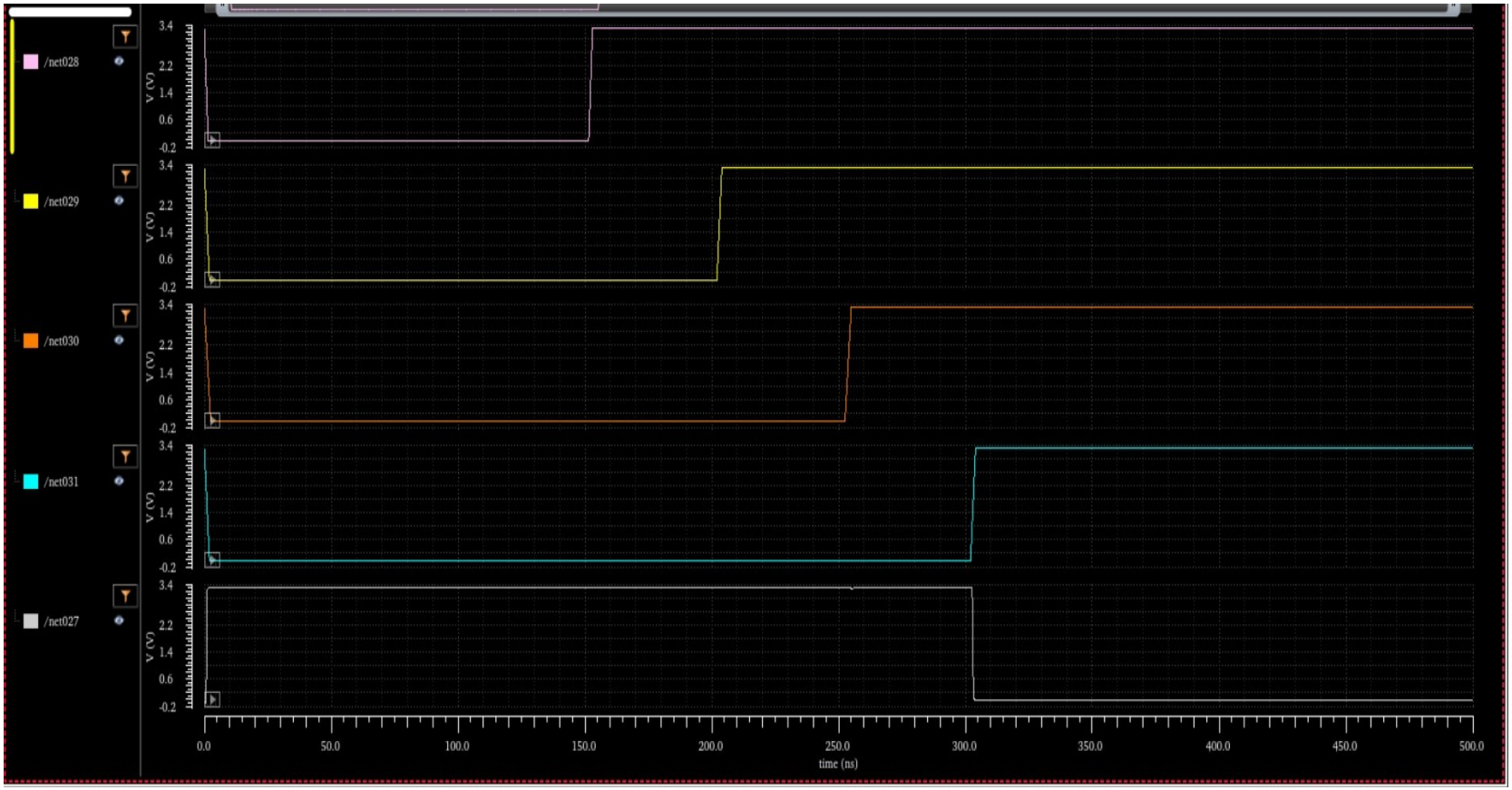
4. Logic Gates and Encoder

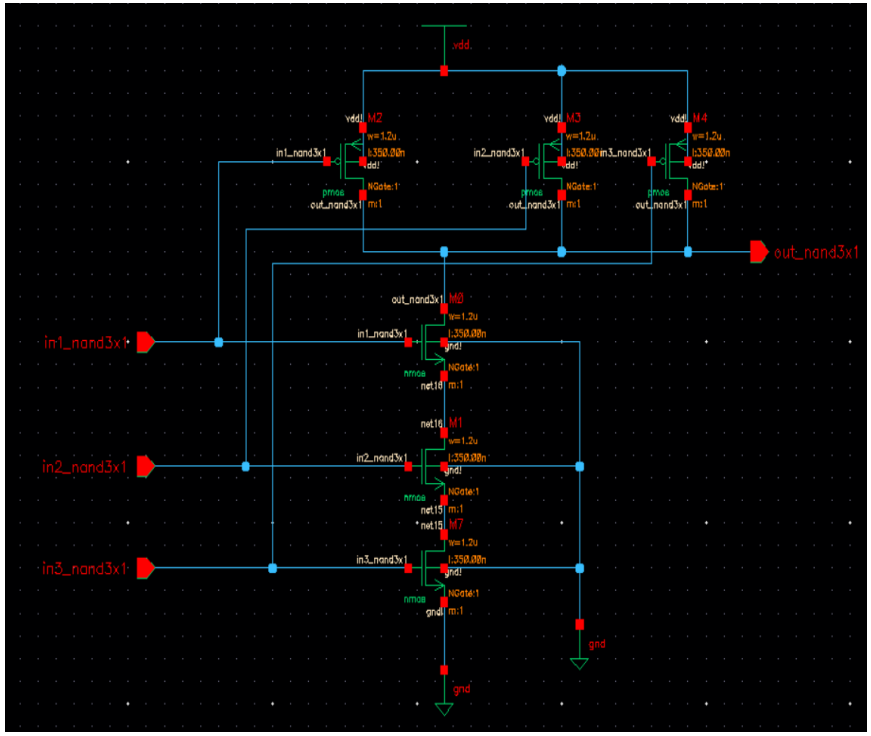
Transient Response (NAND4x1)



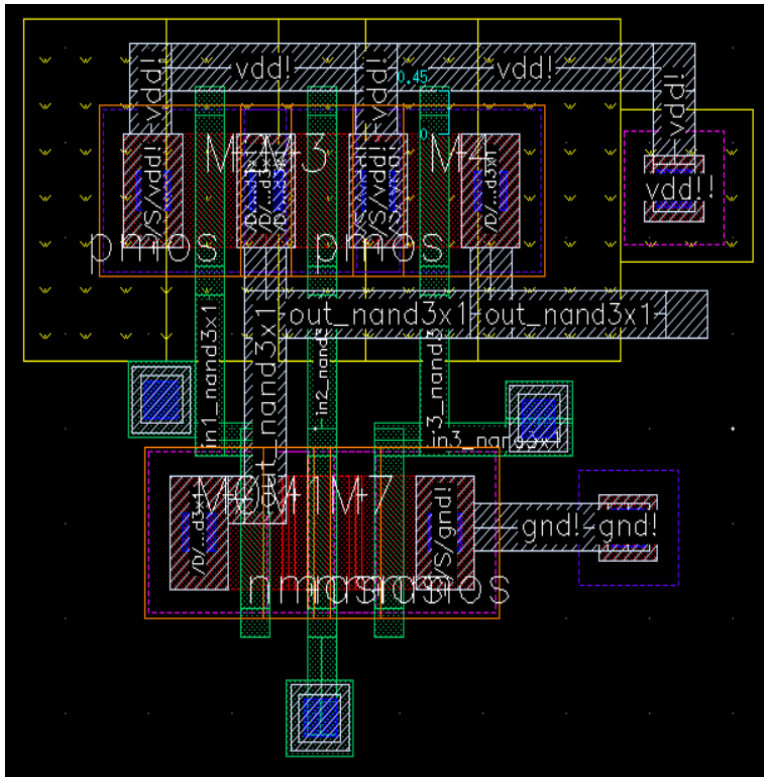
4. Logic Gates and Encoder

NAND3x1

- **Schematic**



- **Layout**



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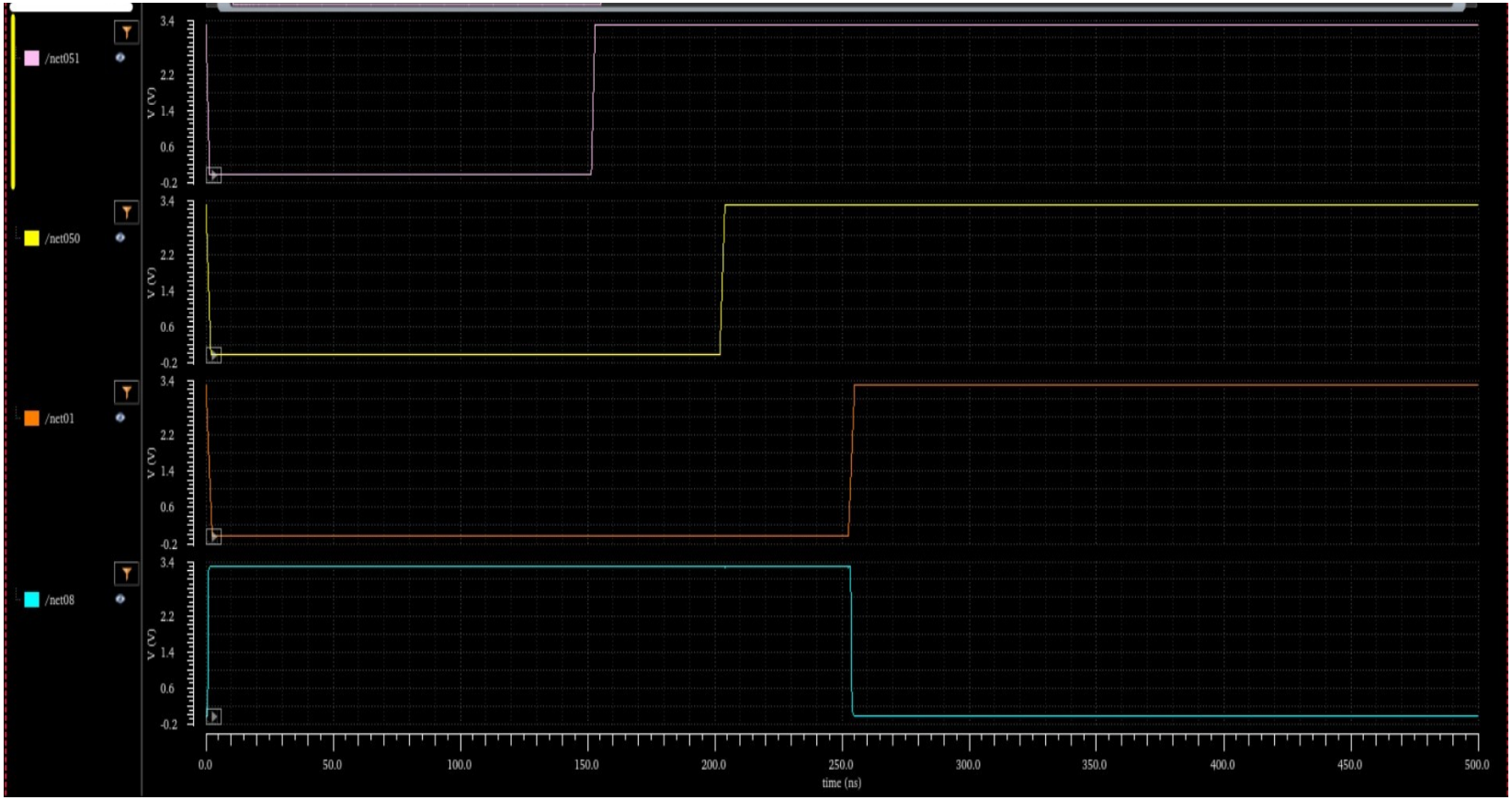
4. Logic Gates and Encoder

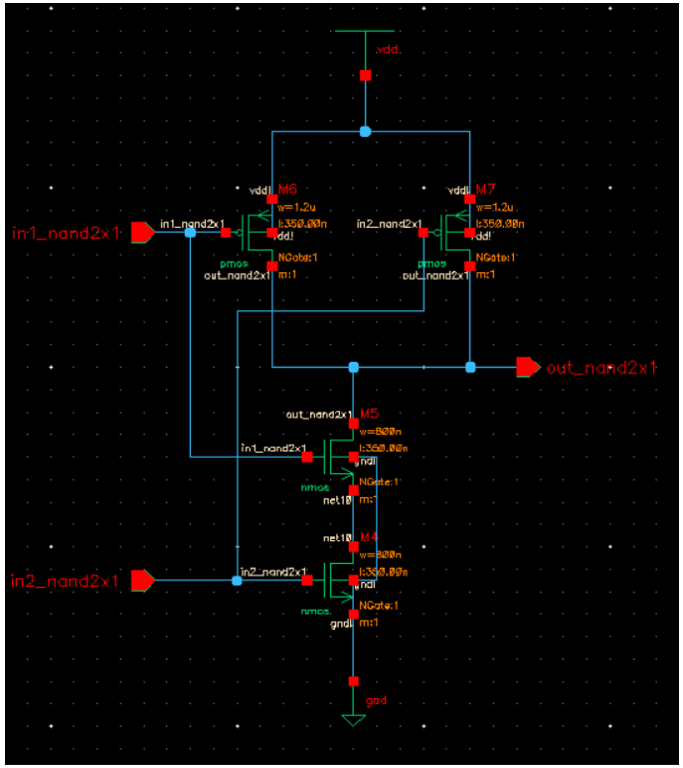
Transient Response (NAND3x1)



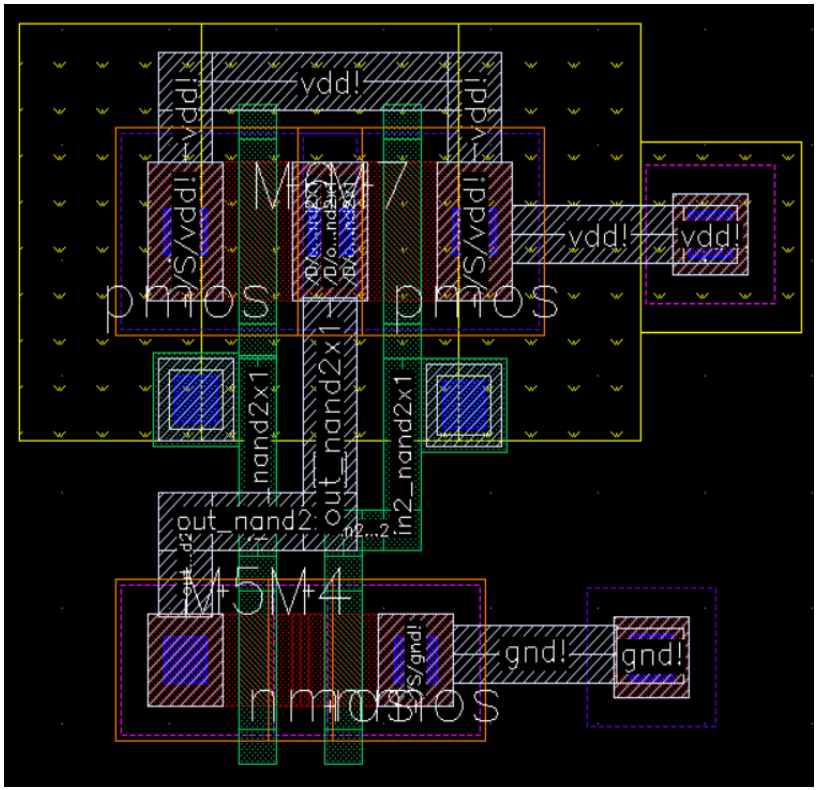
4. Logic Gates and Encoder

NAND2x1

- **Schematic**

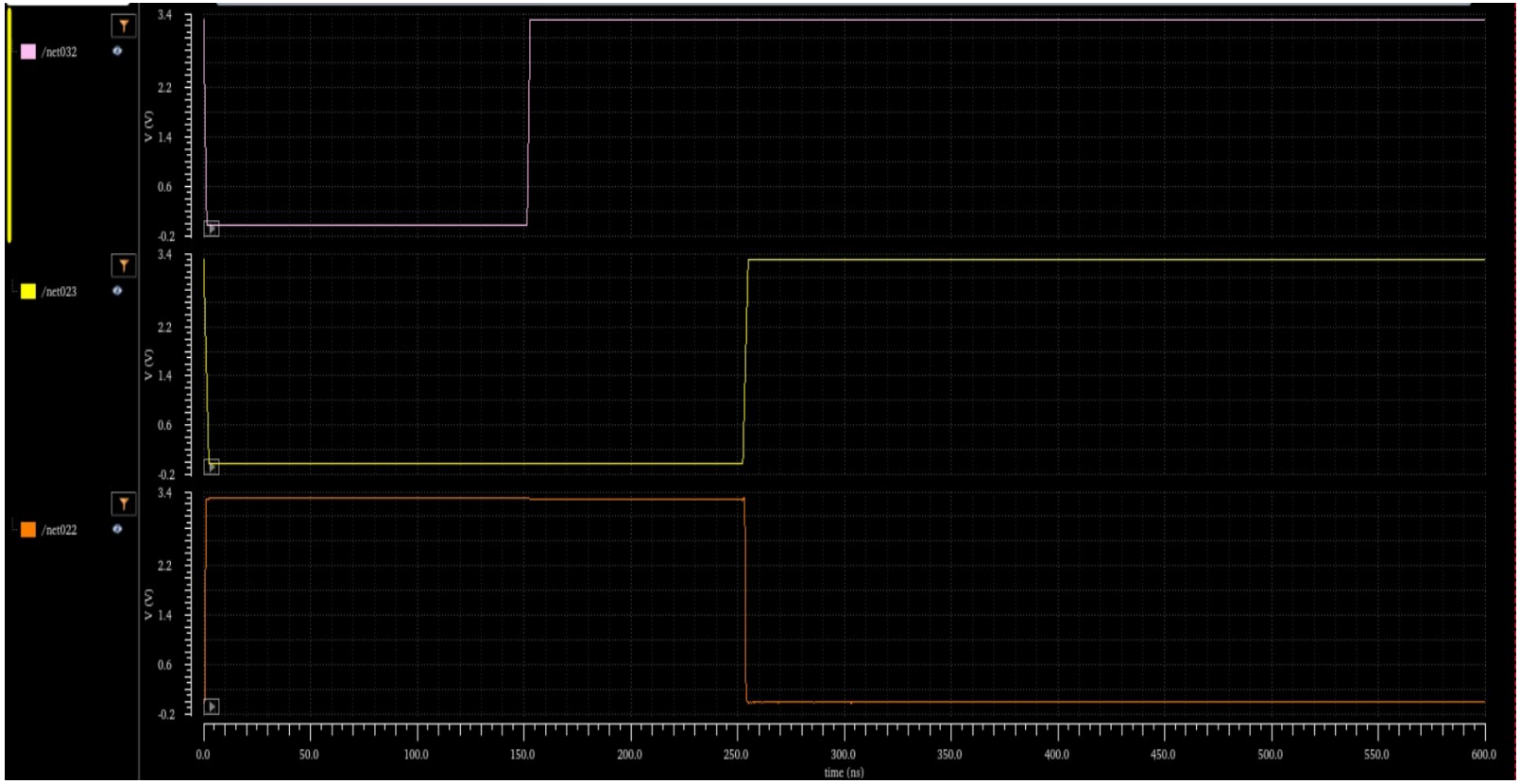


- **Layout**



4. Logic Gates and Encoder

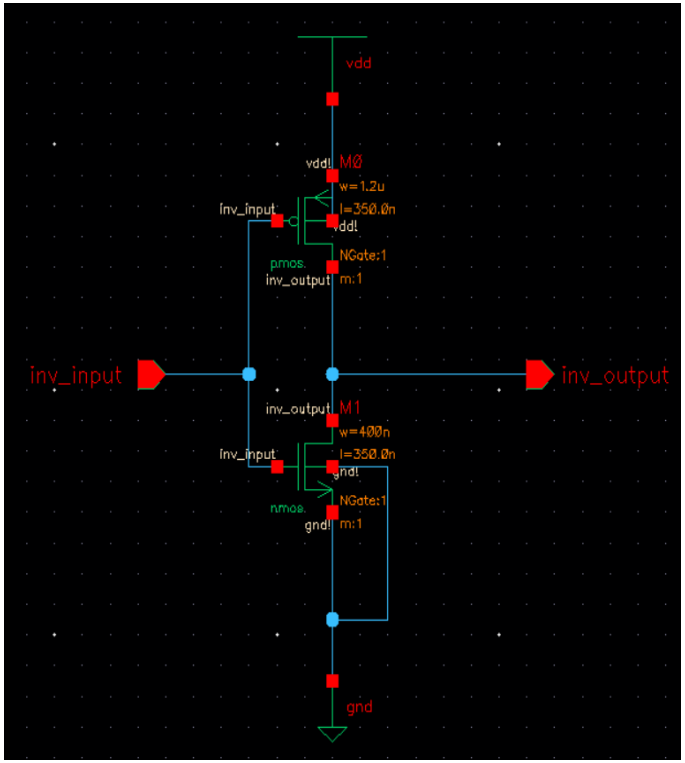
Transient Response (NAND2x1)



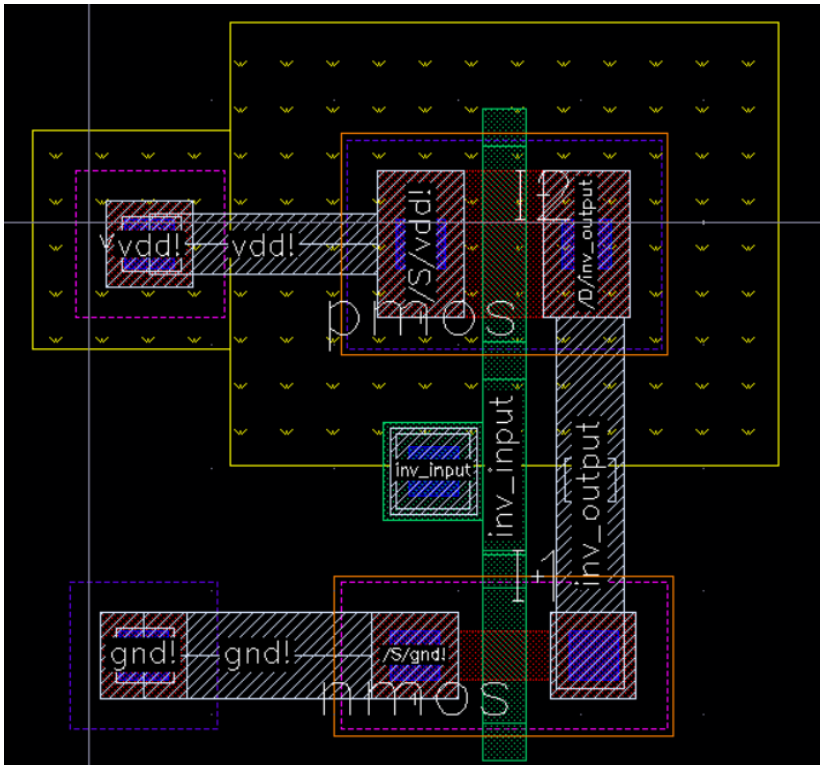
4. Logic Gates and Encoder

NOT

- **Schematic**

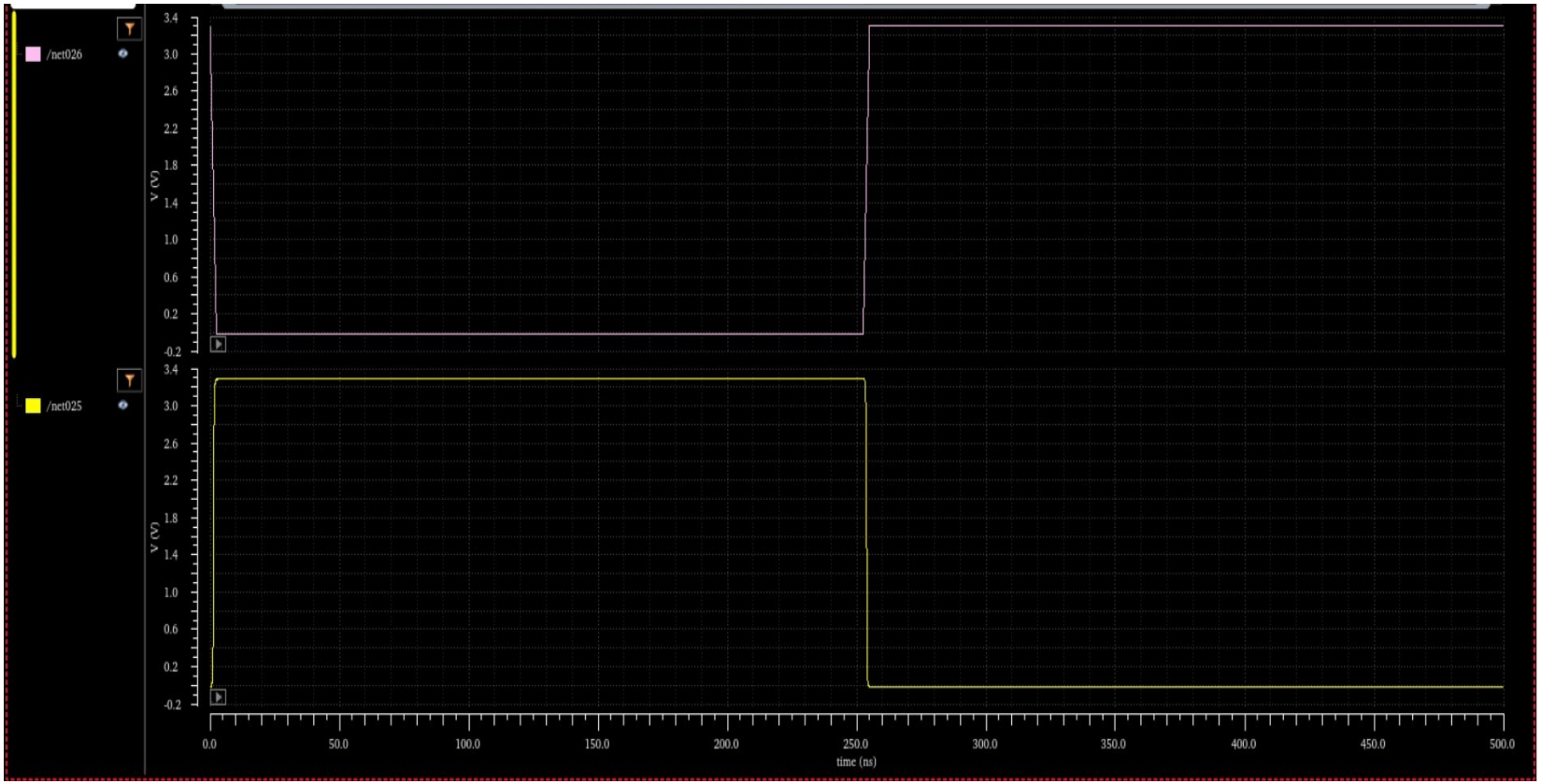


- **Layout**



4. Logic Gates and Encoder

Transient Response (NOT)



4. Logic Gates and Encoder

Encoder Truth Table

In7	In6	In5	In4	In3	In2	In1	Out2	Out1	Out0
0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	0	0	1
0	0	0	0	0	1	X	0	1	0
0	0	0	0	1	X	X	0	1	1
0	0	0	1	X	X	X	1	0	0
0	0	1	X	X	X	X	1	0	1
0	1	X	X	X	X	X	1	1	0
1	X	X	X	X	X	X	1	1	1

4. Logic Gates and Encoder

Logic functions

$$Q_2 = I_7 + I_6 + I_5 + I_4$$
$$Q_1 = \bar{I_7}\bar{I_6}\bar{I_5}\bar{I_4}\bar{I_3}I_2 + \bar{I_7}\bar{I_6}\bar{I_5}\bar{I_4}I_3 + \bar{I_7}I_6 + I_7$$
$$Q_0 = \bar{I_7}\bar{I_6}\bar{I_5}\bar{I_4}\bar{I_3}\bar{I_2}I_1 + \bar{I_7}\bar{I_6}\bar{I_5}\bar{I_4}I_3 + \bar{I_7}\bar{I_6}I_5 + I_7$$

The function can be simplified exploiting the Boolean identity:

$$\bar{A}B + A = A + B$$

4. Logic Gates and Encoder

Simplification

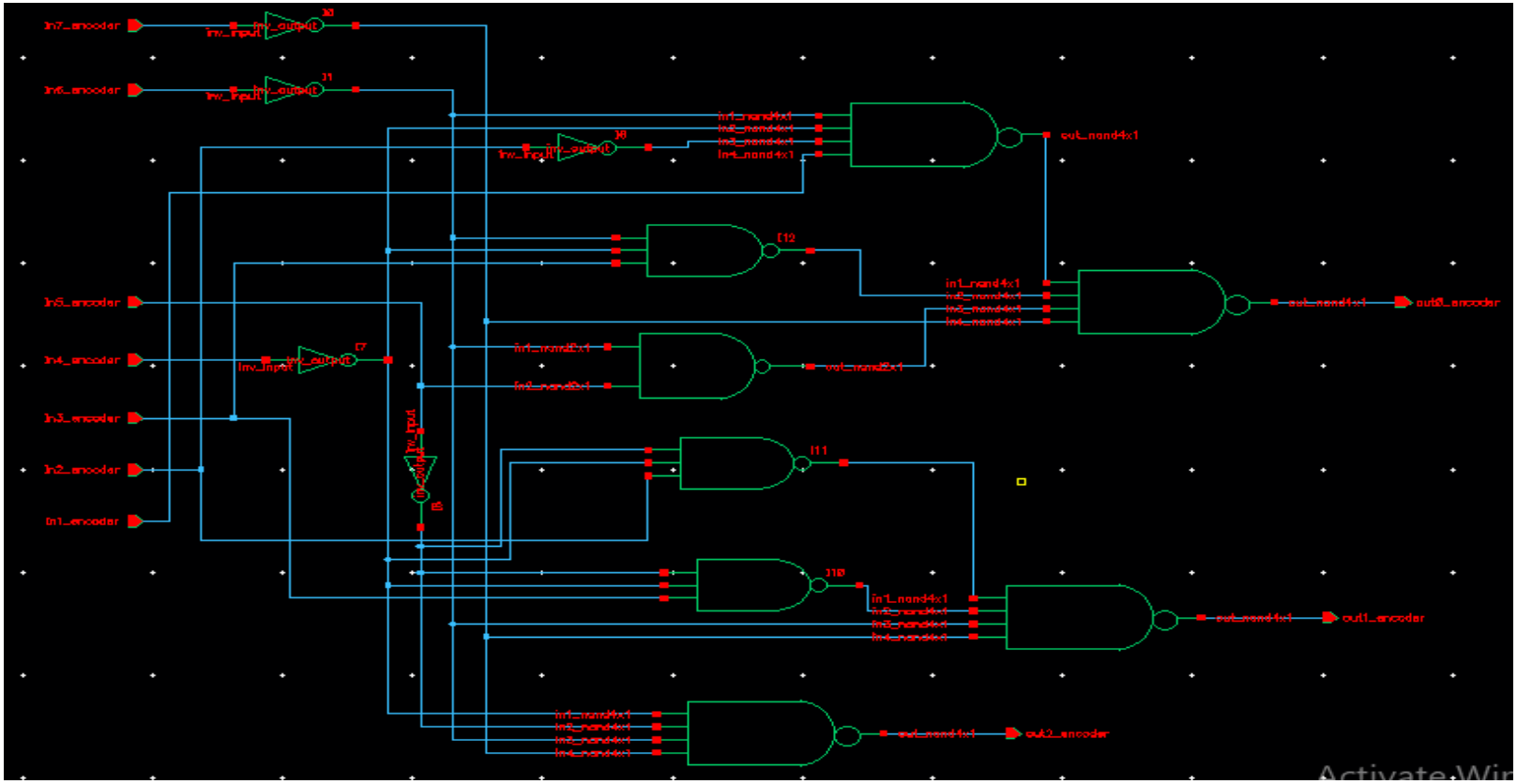
$$Q_2 = I_7 + I_6 + I_5 + I_4$$
$$Q_1 = \overline{I_5}\,\overline{I_4} I_2 + \overline{I_5}\,\overline{I_4} I_3 + I_6 + I_7$$
$$Q_0 = \overline{I_6}\,\overline{I_4}\,\overline{I_2} I_1 + \overline{I_6}\,\overline{I_4} I_3 + \overline{I_6} I_5 + I_7$$

Further manipulation using De Morgan's law, to realize it with only inverters and NAND gates:

$$Q_2 = \overline{\overline{I_7} \cdot \overline{I_6} \cdot \overline{I_5} \cdot \overline{I_4}}$$
$$Q_1 = \overline{\overline{\overline{I_5}\,\overline{I_4} I_2} \cdot \overline{\overline{I_5}\,\overline{I_4} I_3} \cdot \overline{I_6} \cdot \overline{I_7}}$$
$$Q_0 = \overline{\overline{\overline{I_6}\,\overline{I_4}\,\overline{I_2} I_1} \cdot \overline{\overline{I_6}\,\overline{I_4} I_3} \cdot \overline{\overline{I_6} I_5} \cdot \overline{I_7}}$$

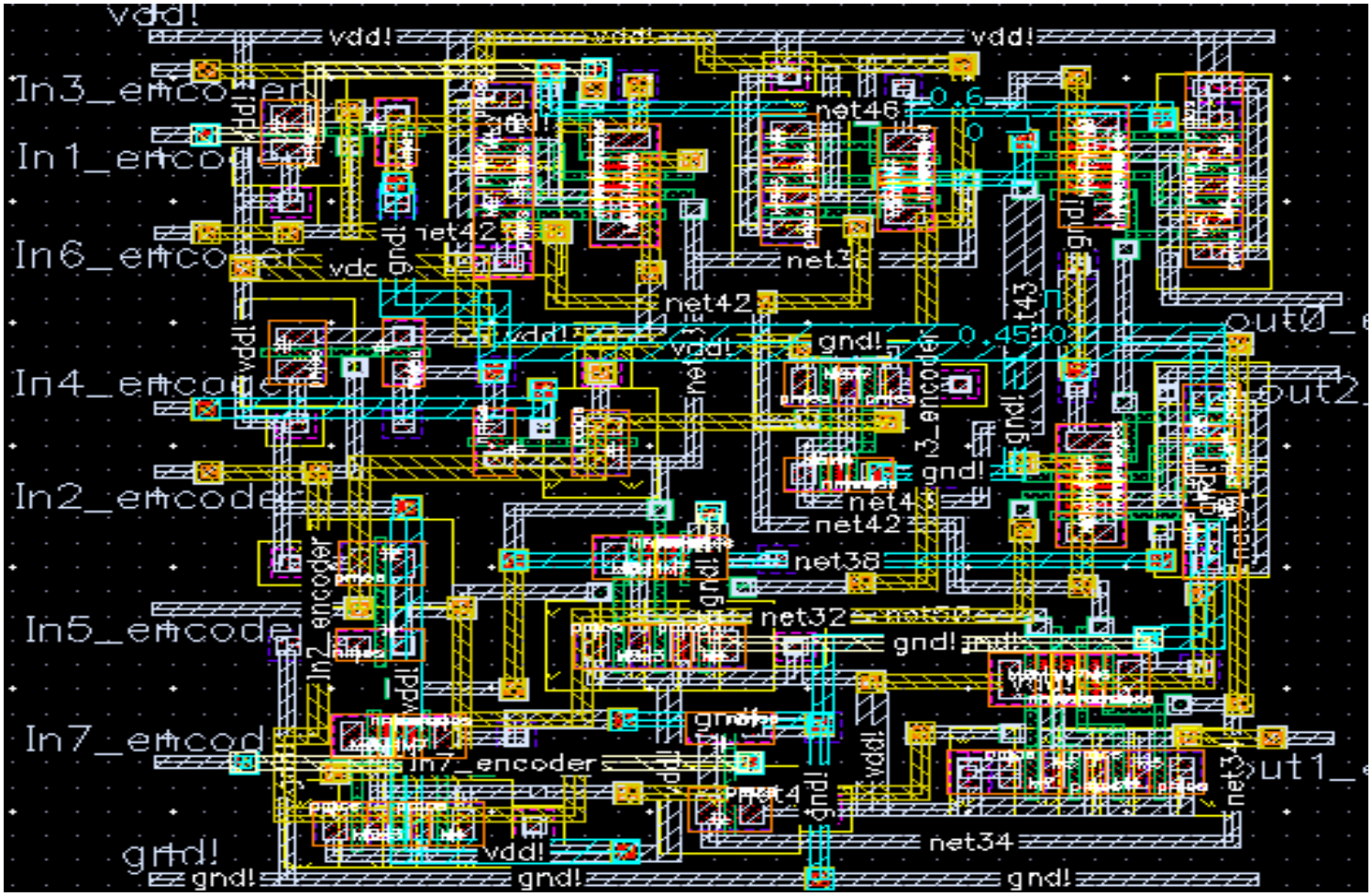
4. Logic Gates and Encoder

Schematic



4. Logic Gates and Encoder

Layout

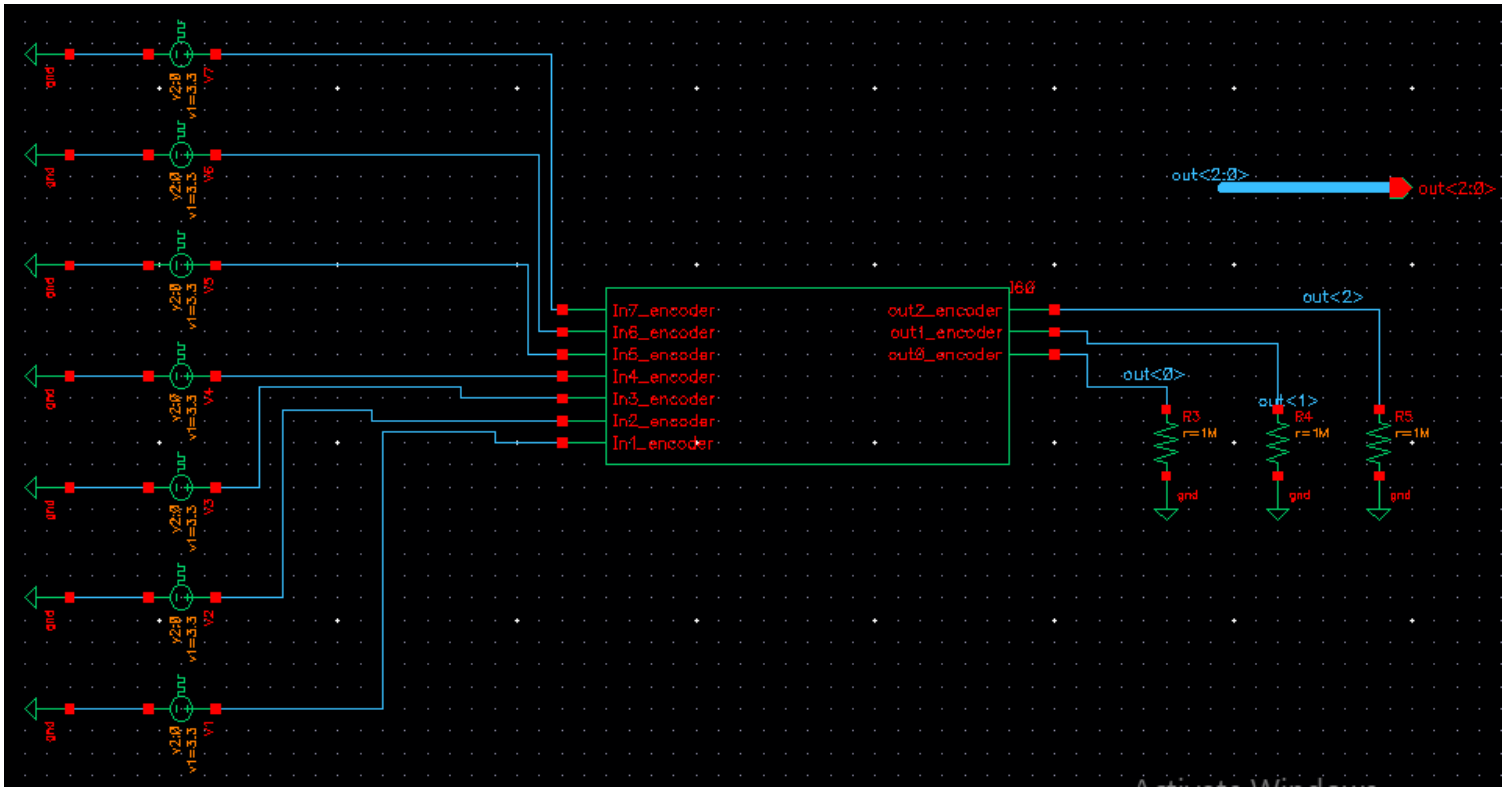


4. Logic Gates and Encoder

Transient analysis (Analog extracted view)

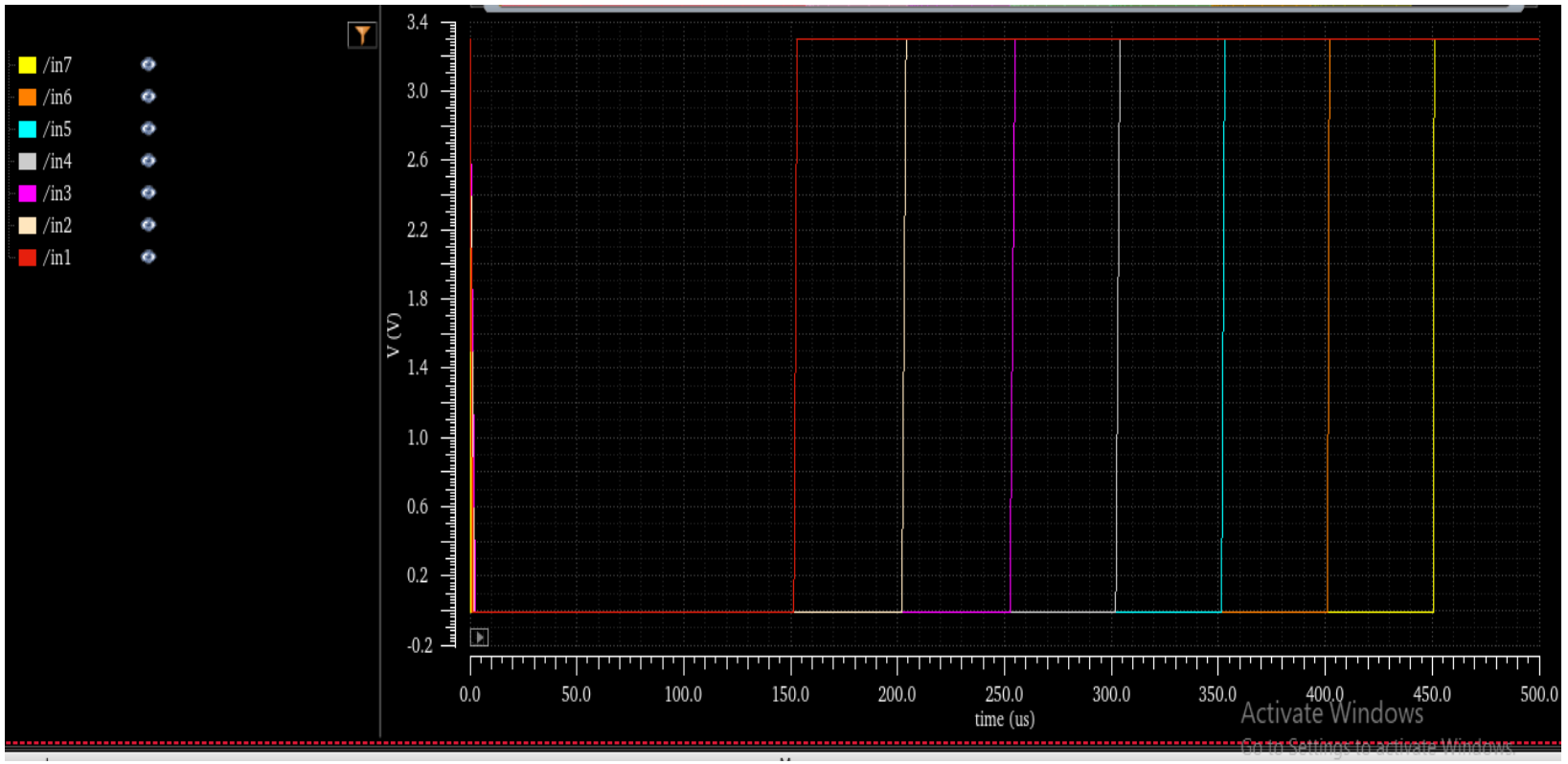
Frequency: 2 kHz

The inputs are switched from low to high in the order of their indices.



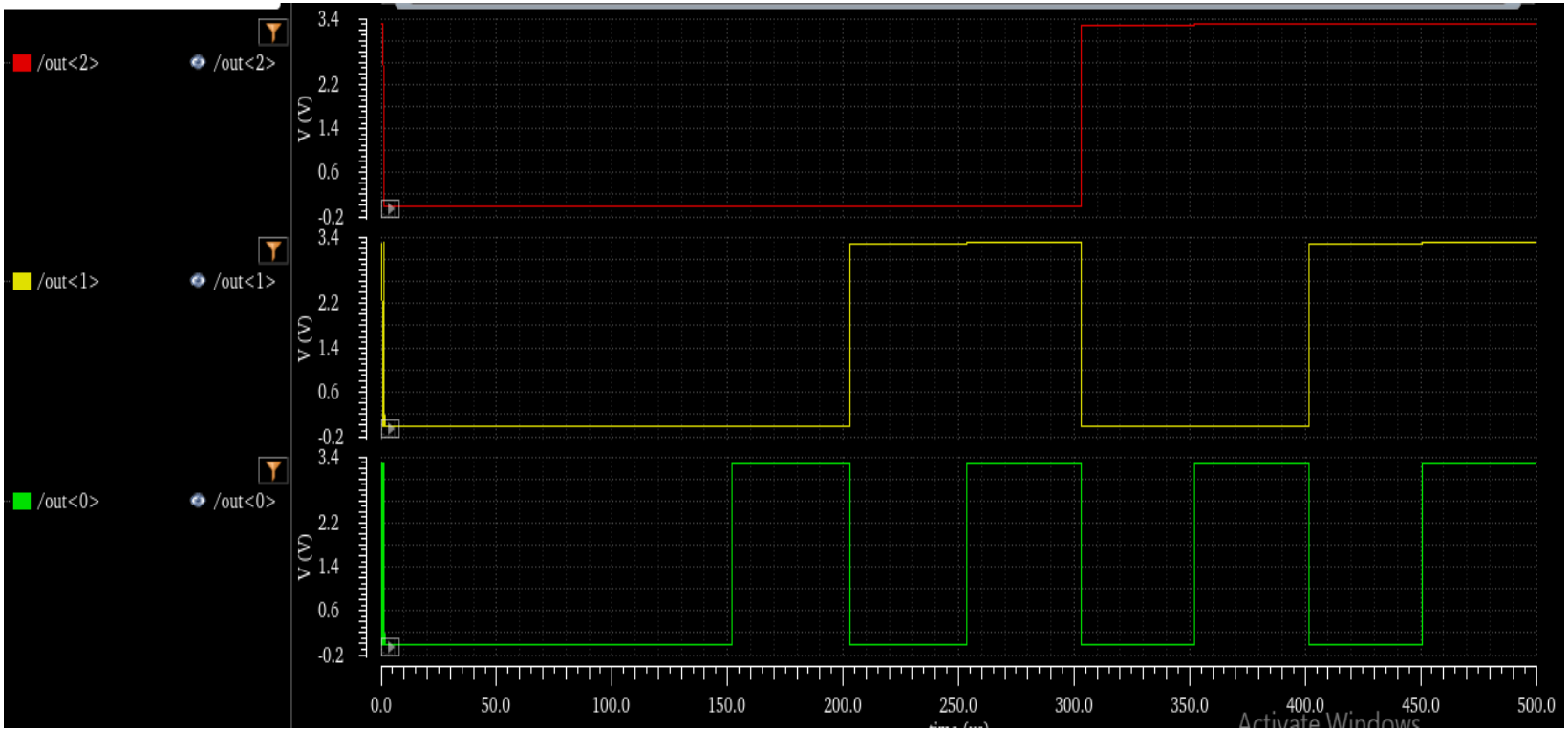
4. Logic Gates and Encoder

Transient analysis (Analog extracted view)



4. Logic Gates and Encoder

Transient analysis (Analog extracted view)

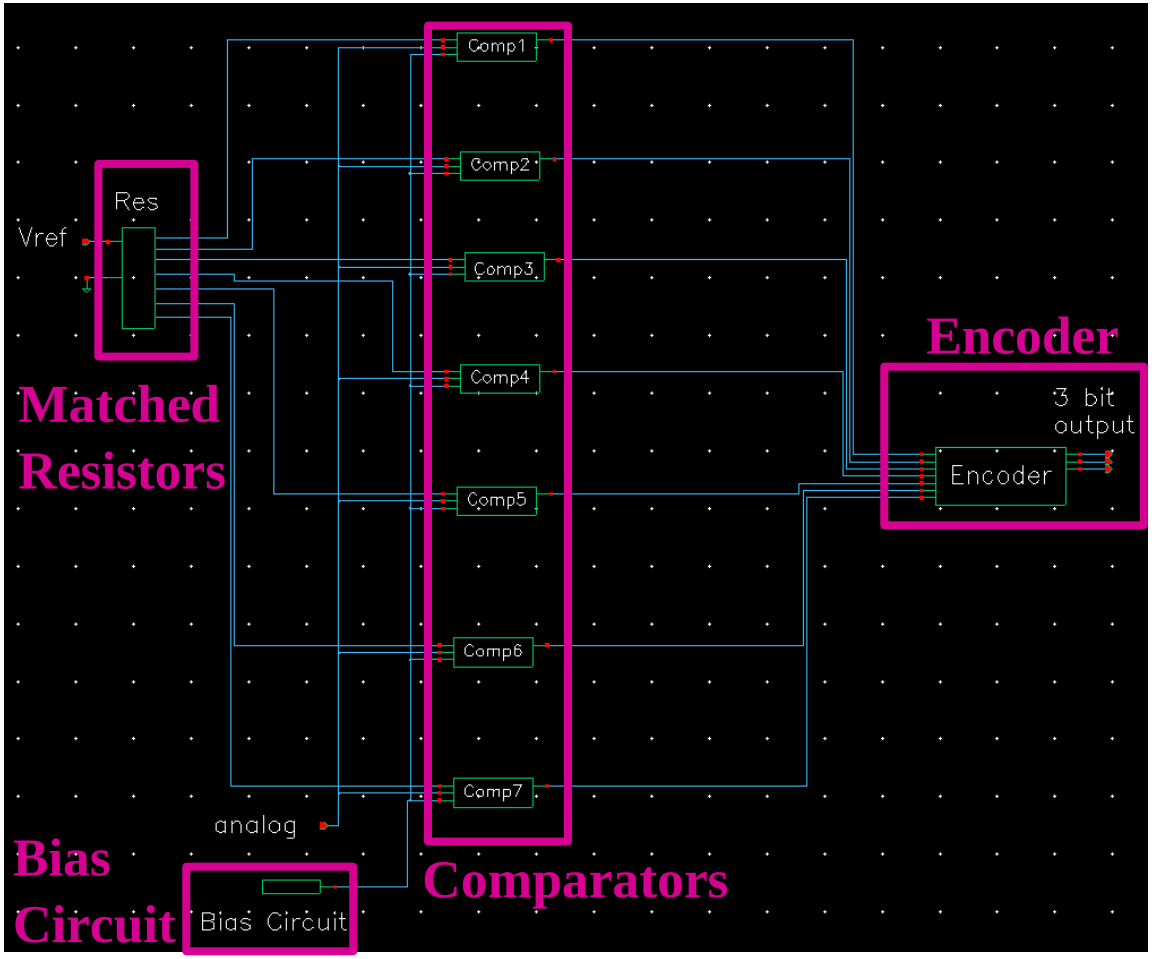


5. ADC

Top Hierarchical level Schematic

➢ **Design specifications:**

- Reference voltage: Vref=Vdd=3.3V
- Input voltage range : 3.3V and 0V
- Bias Current ≈ 20uA



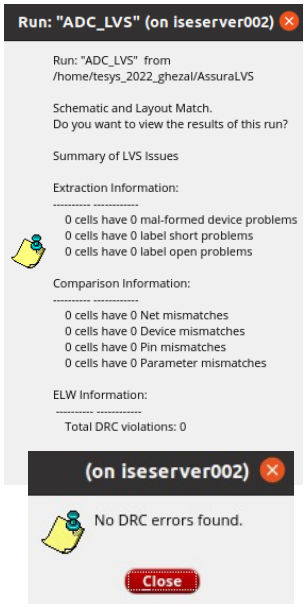
5. ADC

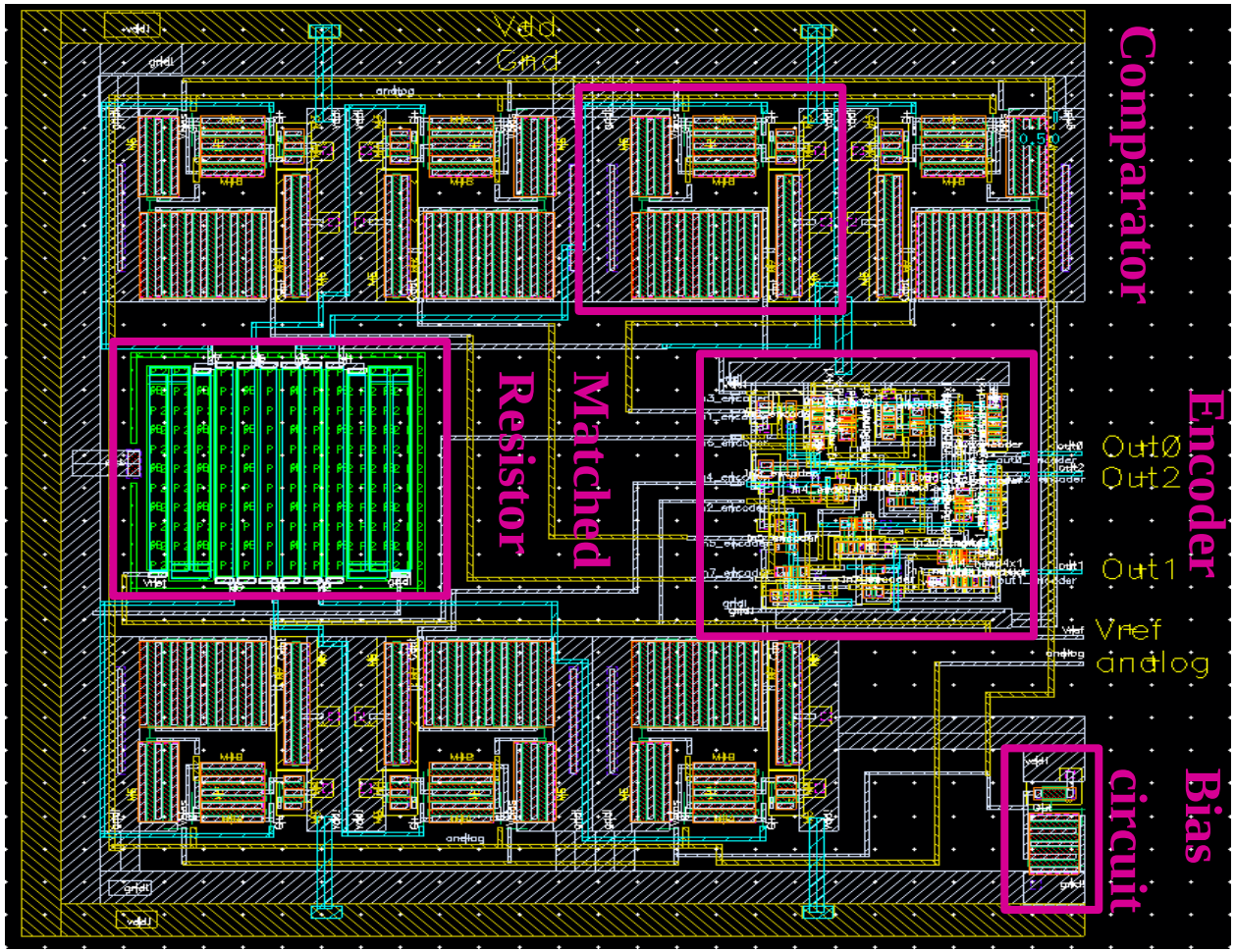
Layout

- Area of Flash cell:

134.575um x

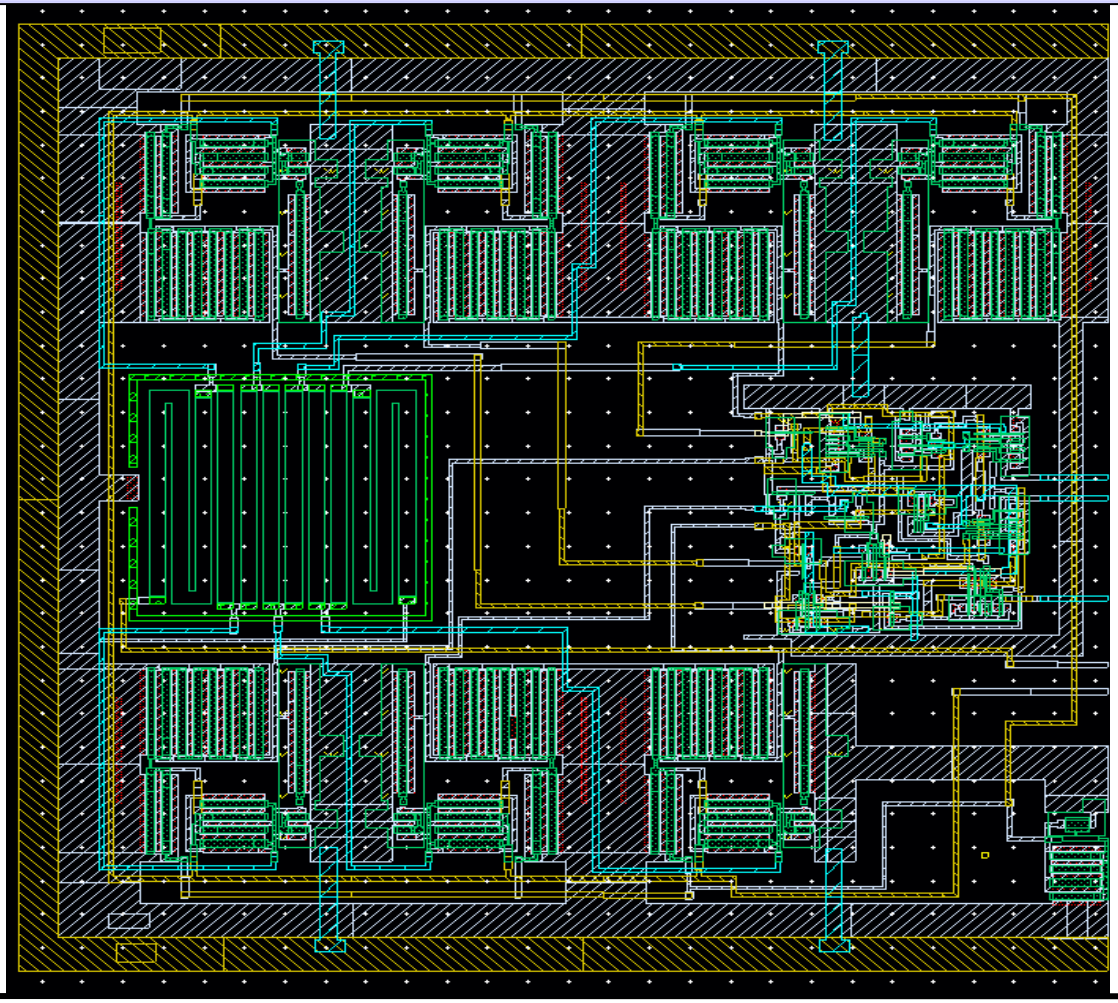
141.325um





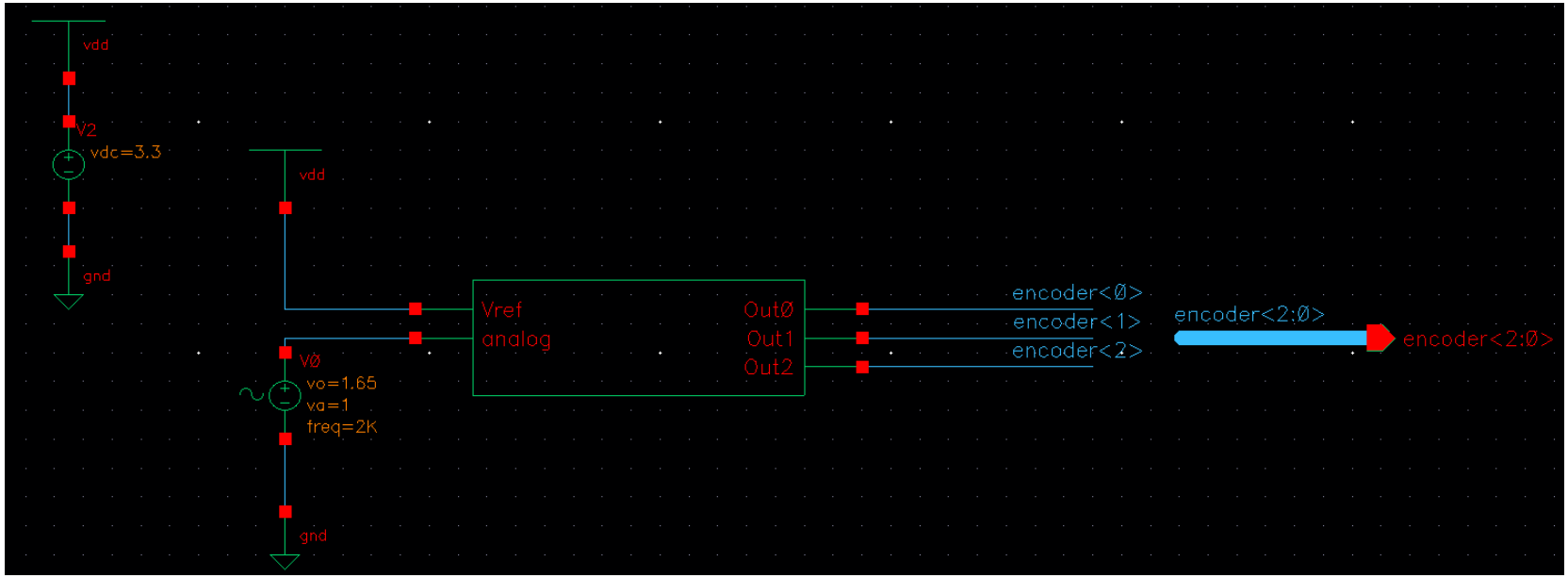
5. ADC

Analog extracted view



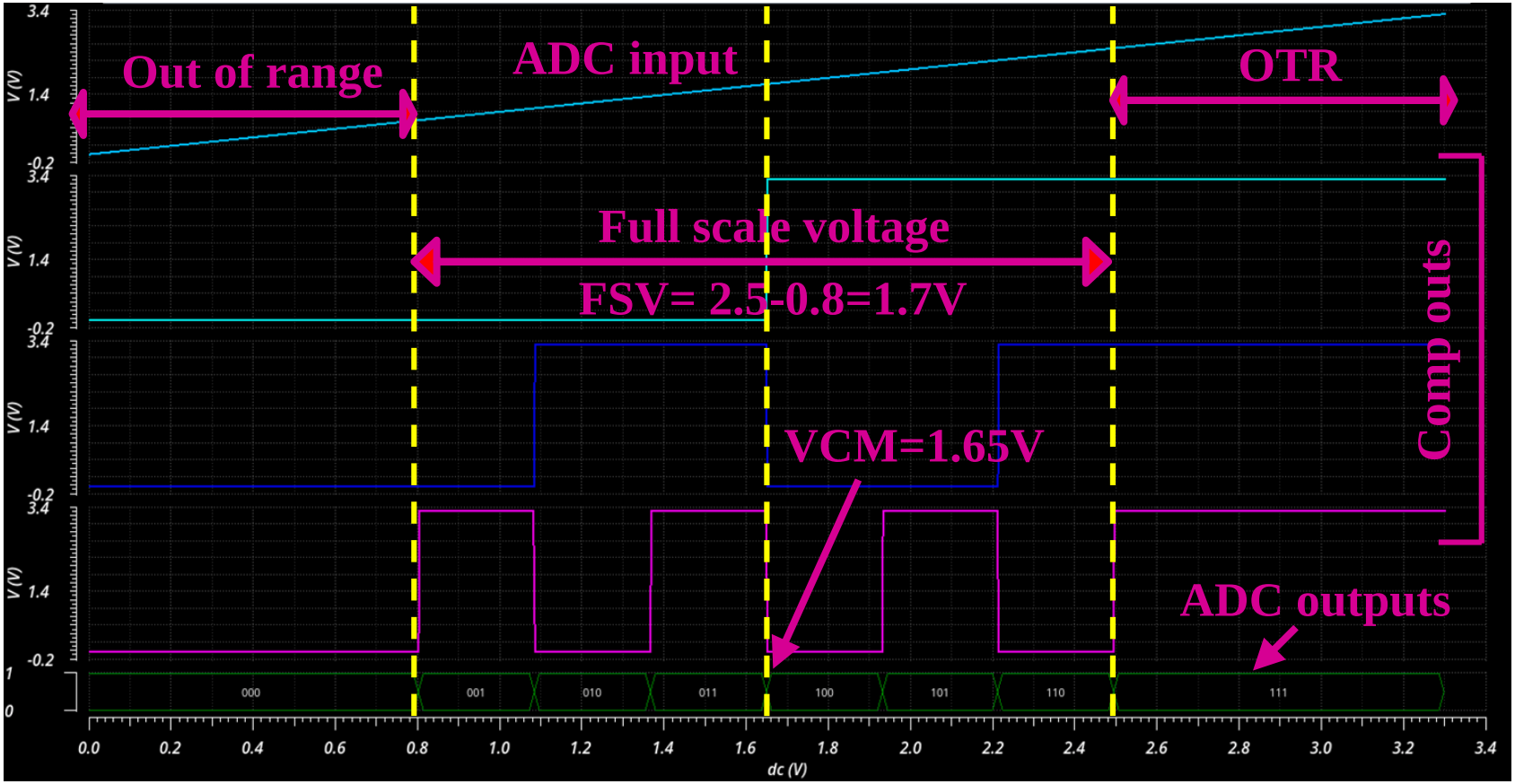
5. ADC

Test bench



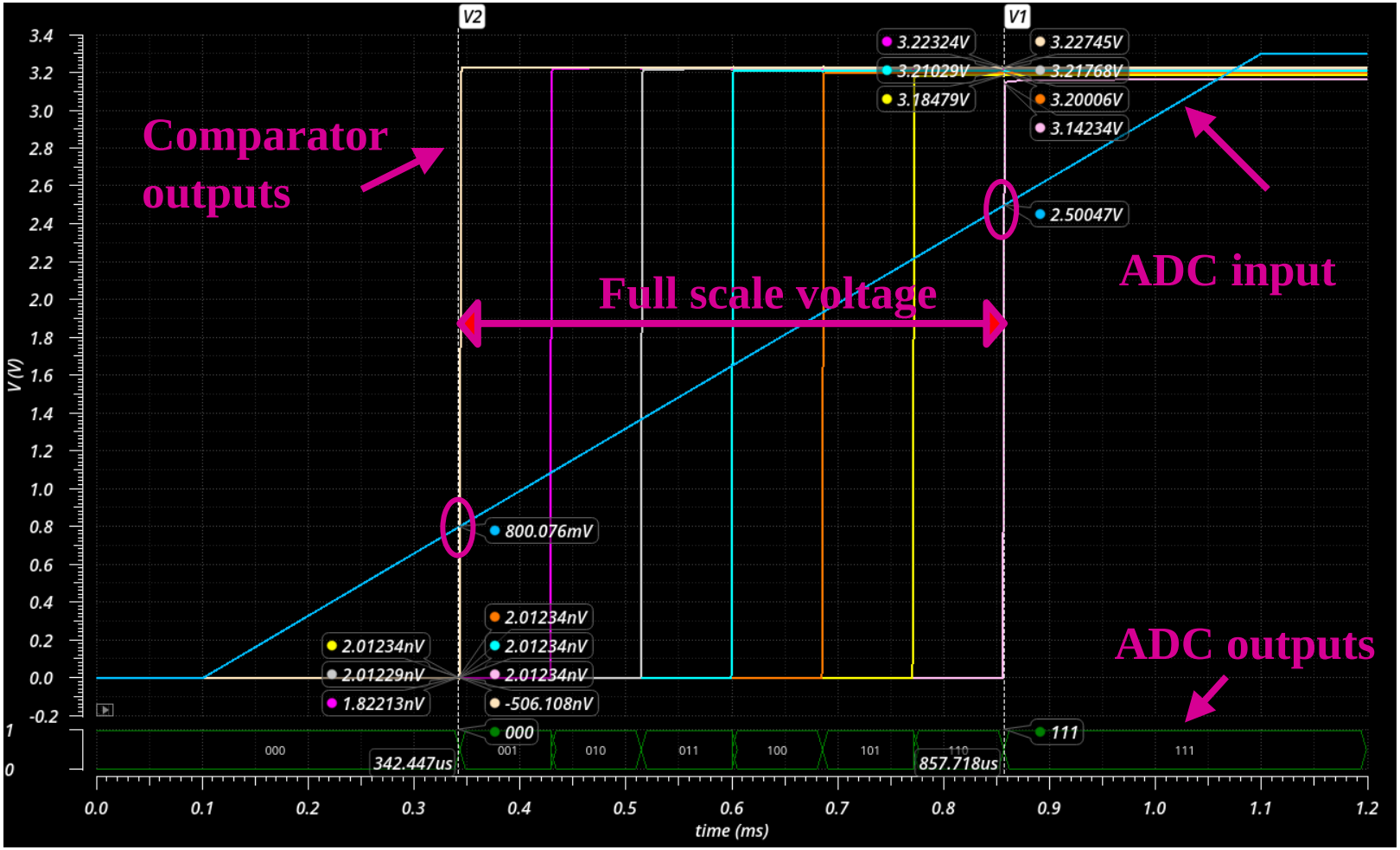
5. ADC

DC characteristic (Analog extracted view)



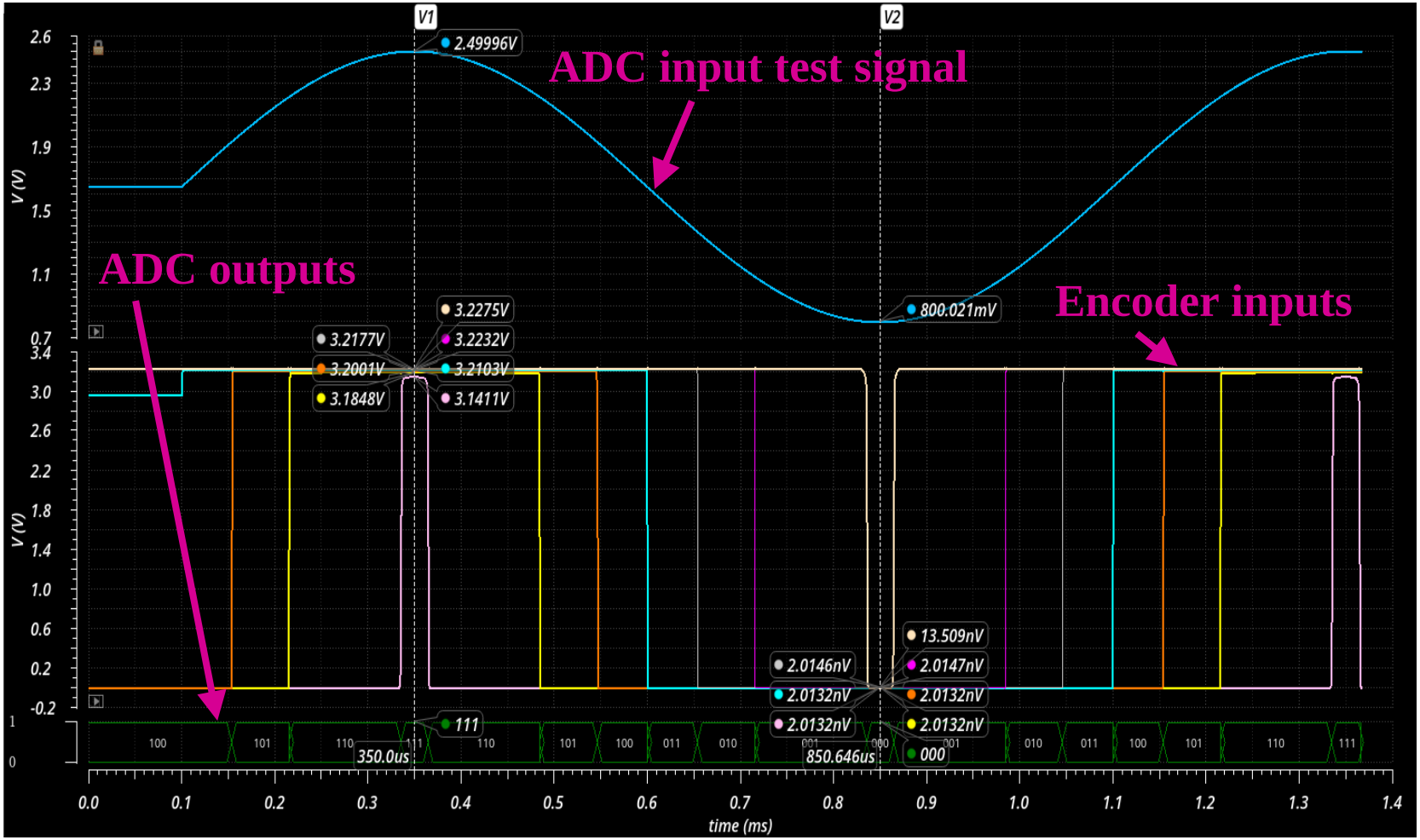
5. ADC

Transient analysis (Analog extracted view)



5. ADC

Transient analysis (analog extracted view)



5. ADC

Transient analysis

- Design properties: Post layout simulation (extracted view)

Properties	Values
Quiescent power	2.4057 mW
Conversion Power @ max. freq.	2.9073 mW
Device statistics for ADC	115 Transistors
Maximum frequency	10 kHz

Conclusion

- Nominal design of 3-Bit Flash ADC done
- Maximum frequency 10 kHz with 2.9073 mW conversion power and 2.4057 mW quiescent power
- Compact layout area of 134.575um x 141.325um
- MC, WC/corner simulations!
- Better matching
- Reference voltage circuit design.

References

✓Lecture and lab material of TESYS subject by Prof. Koenig used to prepare this project and the presentation slides

Thank you for your attention!