InAmp with external R_G and offset compensation based on Miller type OpAmp

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Overview

I. Miller OpAmp

1. **Schematic and minimum specifications**
2. **Schematic simulation and parameter adjustments**
3. **Layout design**
4. **Post layout simulation**

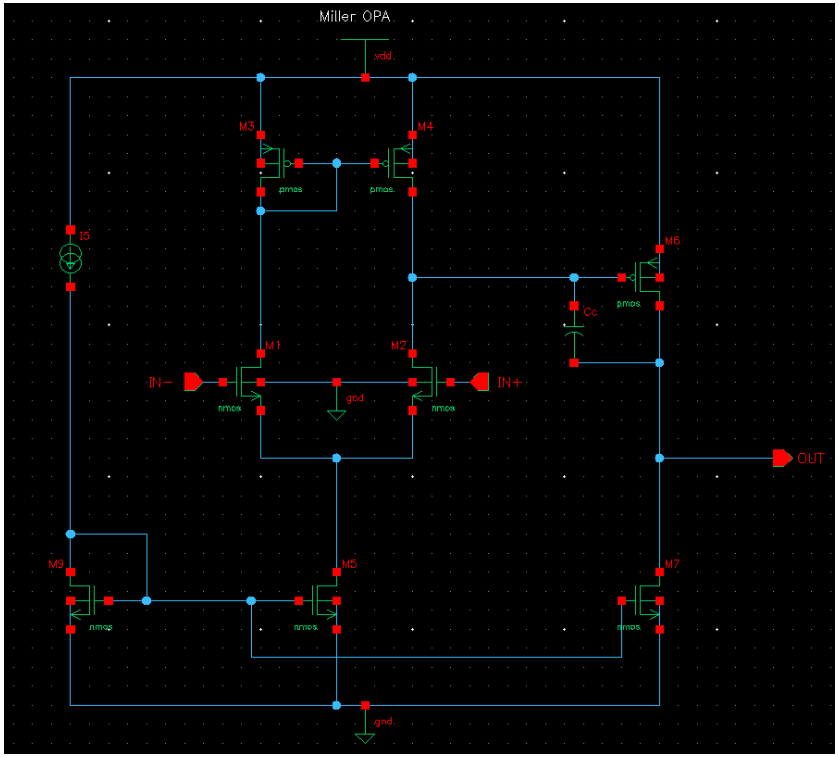
II. InAmp

1. **Layout design**
2. **Post layout simulation**

Miller OpAmp

Schematic and minimum requirements

Schematic



- Stage 1: differential amplifier with pmos current mirror load and single-ended output
- Stage 2: common-source amplifier with a large miller capacitor
- M5 quiescent current set by separate biasing circuit
- Miller compensation capacitor improves stability at the cost of bandwidth

Miller OpAmp

Schematic and minimum requirements

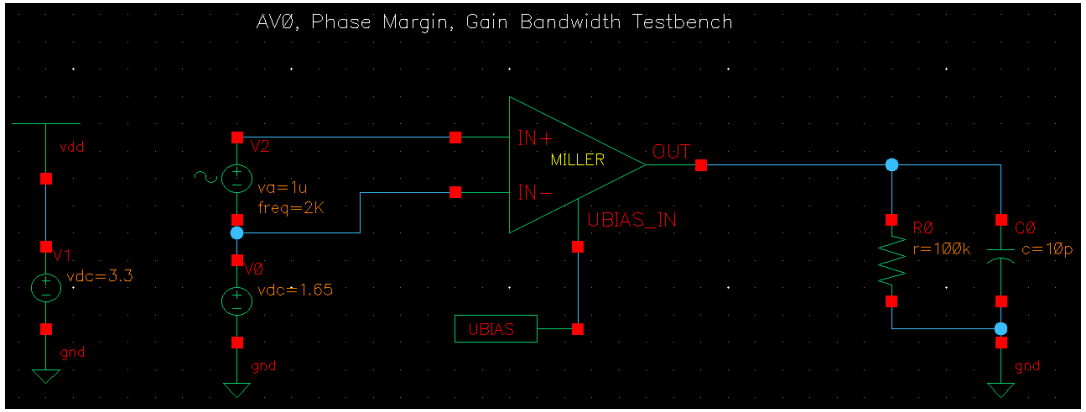
Minimum requirements

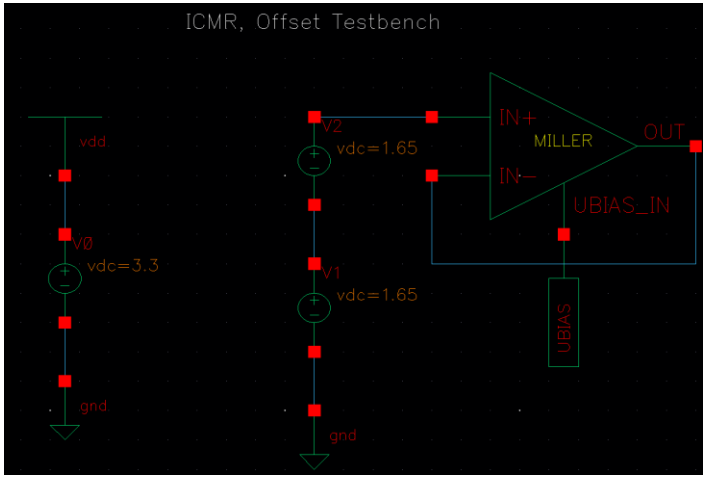
Open Loop Gain	80 dB
Gain Bandwidth	1 MHz
Phase Margin	60°
Common Mode Range +	0.75 V
Common Mode Range -	-0.75 V
Settling Time	< 1 µs
Slew Rate	1 V/µs
Offset	minimum
CMRR	80 dB
Power Dissipation	minimum
Load Capacitance	10 pF

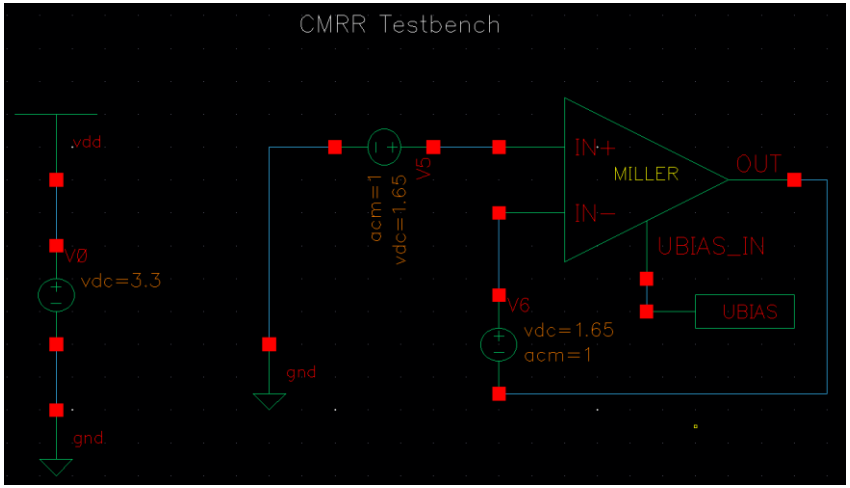
- Minimum requirements for acceptable performance
- Miller OpAmp used to design InAmp in later stage of the project
  - ➢ Higher Open Loop Gain, Slew Rate and Settling time than minimum specification further improve InAmp performance

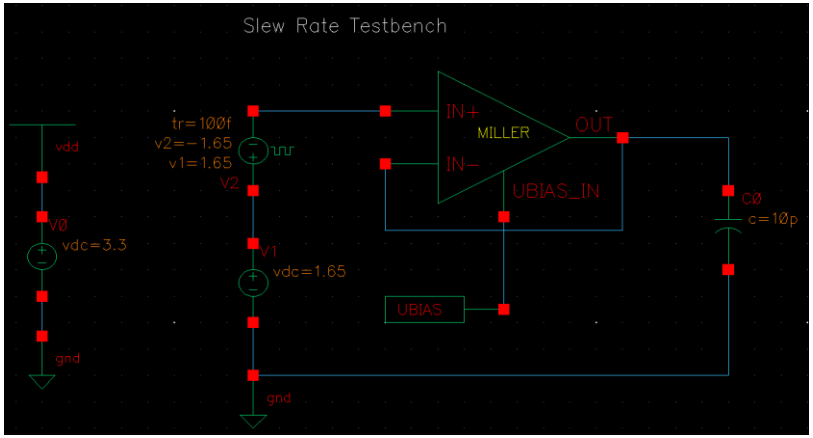
Miller OpAmp

Simulation schematics









Miller OpAmp

Schematic simulation and parameter adjustments

Implementing the before calculated design parameters in the schematic and running all simulations resulted in the following specification:

Open Loop Gain	77 dB
Gain Bandwidth	976 kHz
Phase Margin	73°
Common Mode Range +	1.52 V
Common Mode Range -	-1.30 V
Settling Time	0.77 µs
Slew Rate	1 V/µs
Offset	80 µV
CMRR	86.64 dB

- Open Loop Gain and Gain Bandwidth below minimum spec, high Offset
- Excessive Phase Margin
- Slew Rate and Common Mode Rejection Ratio match minimum spec but improvement for better InAmp performance useful

Miller OpAmp

Schematic simulation and parameter adjustments

Design Approach to improve simulation results

- Hand model transistor equations give hint on the effect of certain design parameters
- Simulator uses much more complex transistor models

  ➢ Impact of certain parameters might differ from expectation

Solution

- Combine hand model transistor equations with iterative circuit simulation and manual refinement based on experience with the circuit

Miller OpAmp

Schematic simulation and parameter adjustments

Design route

Design change	Specification after Allen/Holberg	Cc -> 1.8pF	I5 -> 4	I5 -> 10	S6, S7 -> 30	S1, S2 -> 2	S1, S2 -> 3	S7 -> 35	S6 -> 31	Final simulation		
												Cc -> 1.6
Open Loop Gain in dB	77	*	78	77	79	82	83	-	-	81.6		
Gain Bandwidth in MHz	0.976	1.15	1.65	2.67	2.80	3.8	4.6	-	-	4.6		-
Phasemargin in °	73	71	69	66	72	66	62	-	-	63		5.05
Common Mode Range - in V	1.52	-	-	-1.3	-	-	*	-	-	*		60.7
Common Mode Range + in V	-1.30	-	-	1.3	-	-	*	-	-	1.22		-
Settling Time in µs	0.77	-	-	-	-	-	-	-	-	-		-
Slew Rate in µs	1	1.22	2.19	4.2	5.3	5.4	*	-	-	*		6.07
Common Mode Rejection Ratio in dB	86.64	-	-	82	*	91	100	-	-	99.83		-
Offset in µV	80	-	-	-	-	-	90	35	7.21	*		-
												-
S1, S2	1	*	*	*	*	2	3	*	*	*		
S3, S4	1	*	*	*	*	*	*	*	*	*		*
S6	20	*	*	*	30	*	*	*	31	*		*
S7	20	*	*	*	30	*	*	35	*	*		*
S5	2	*	*	*	*	*	*	*	*	*		*
I5 in µA	2.21	*	4	10	*	*	*	*	*	*		*
Cc in µF	2.21	1.8	*	*	*	*	*	*	*	*		1.6

Miller OpAmp

Schematic simulation and parameter adjustments

	Specification after Allen/Holberg	Design Result	Cc -> 1.6pF ?
Open Loop Gain in dB	77	81.6	81.6
Gain Bandwidth in MHz	0.976	4.59	5.05
Phasemargin in °	73	63°	60.7
Common Mode Range - in V	1.52	1.22	1.22
Common Mode Range + in V	-1.30	-1.3	-1.3
Settling Time in µs	0.77	0.21	0.22
Slew Rate in µs	1	5.42	6.07
Common Mode Rejection Ratio in dB	86.64	99.83	99.83
Offset in µV	80	7.22	7.22
S1, S2	1	3	3
S3, S4	1	1	1
S6	20	31	31
S7	20	35	35
S5	2	2	2
I5 in µA	2.21	10	10
Cc in µF	2.21	1.8	1.6

Further improvement but high chance of Phase Margin requirement not being met after layout and extract, Cc kept at 1.8pF

Miller OpAmp

Layout design

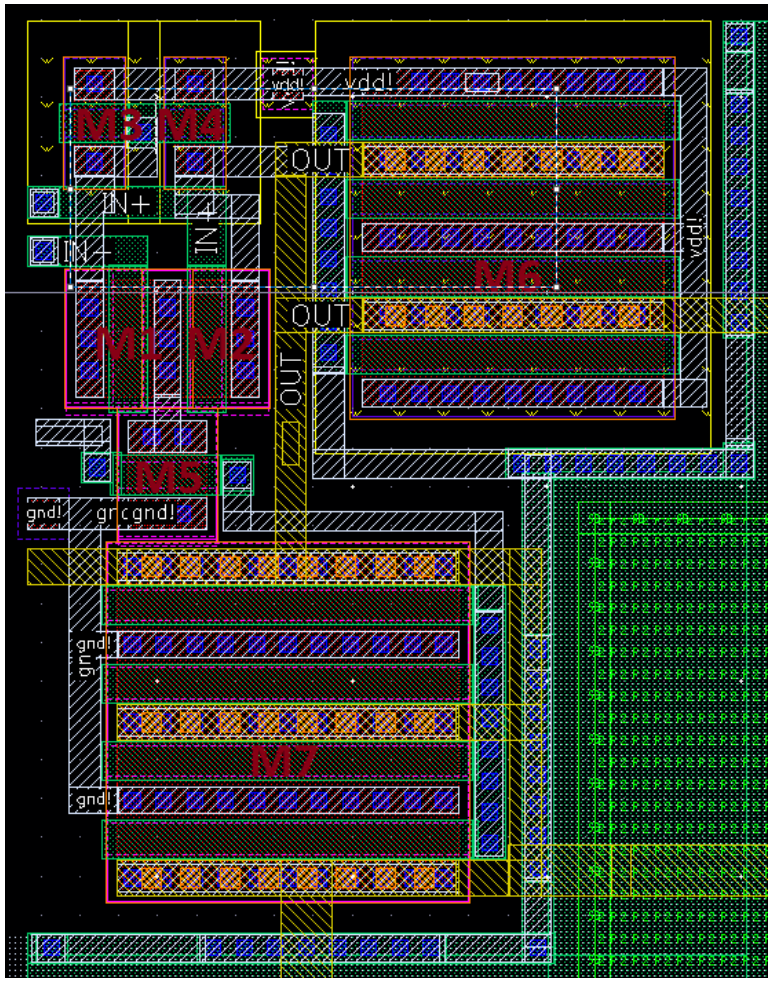
- Transistors must be designed to achieve acceptable W/L ratio in the complete layout
  - Folded layout for M6 and M7
  - Folded layout not necessary for M1 and M2 but would result in better matching, less parasitics

- Arranging the transistors to form a close to perfect square not necessary
  - Fill out space with large Miller capacitor to achieve desired chip level W/L ratio

Miller OpAmp

Layout design

Layout without Cc

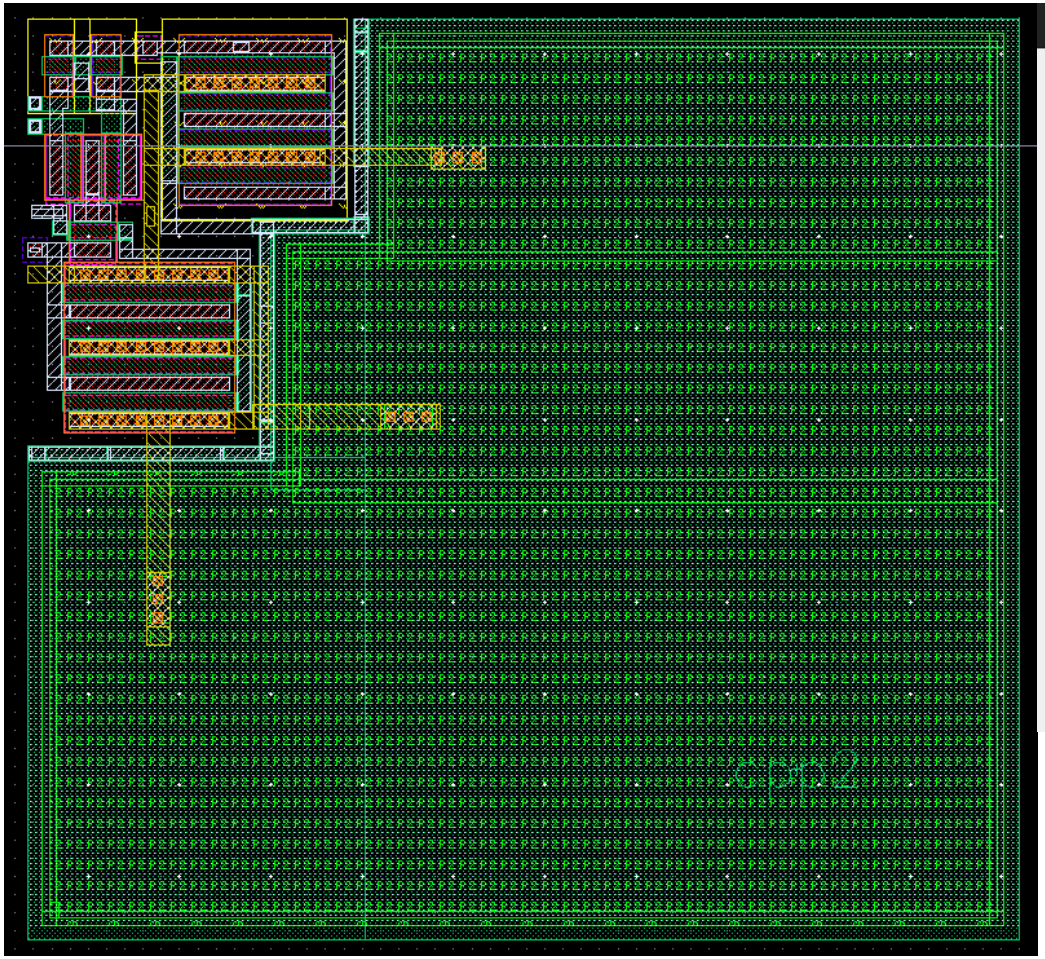


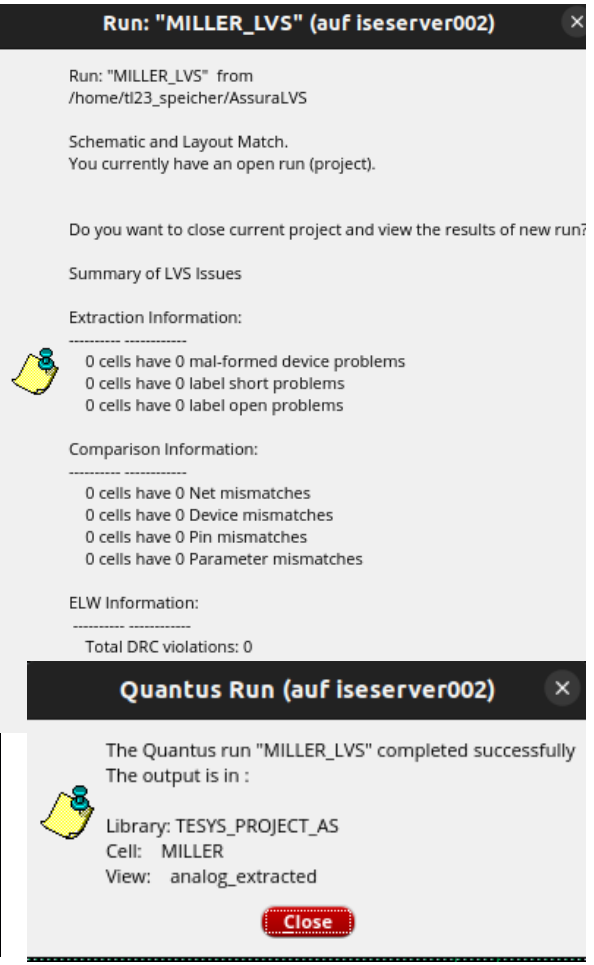
- Arrangement should not have too many corners
- Minimize area by using minimum design rules

Miller OpAmp

Layout design

Layout with Cc





Miller OpAmp

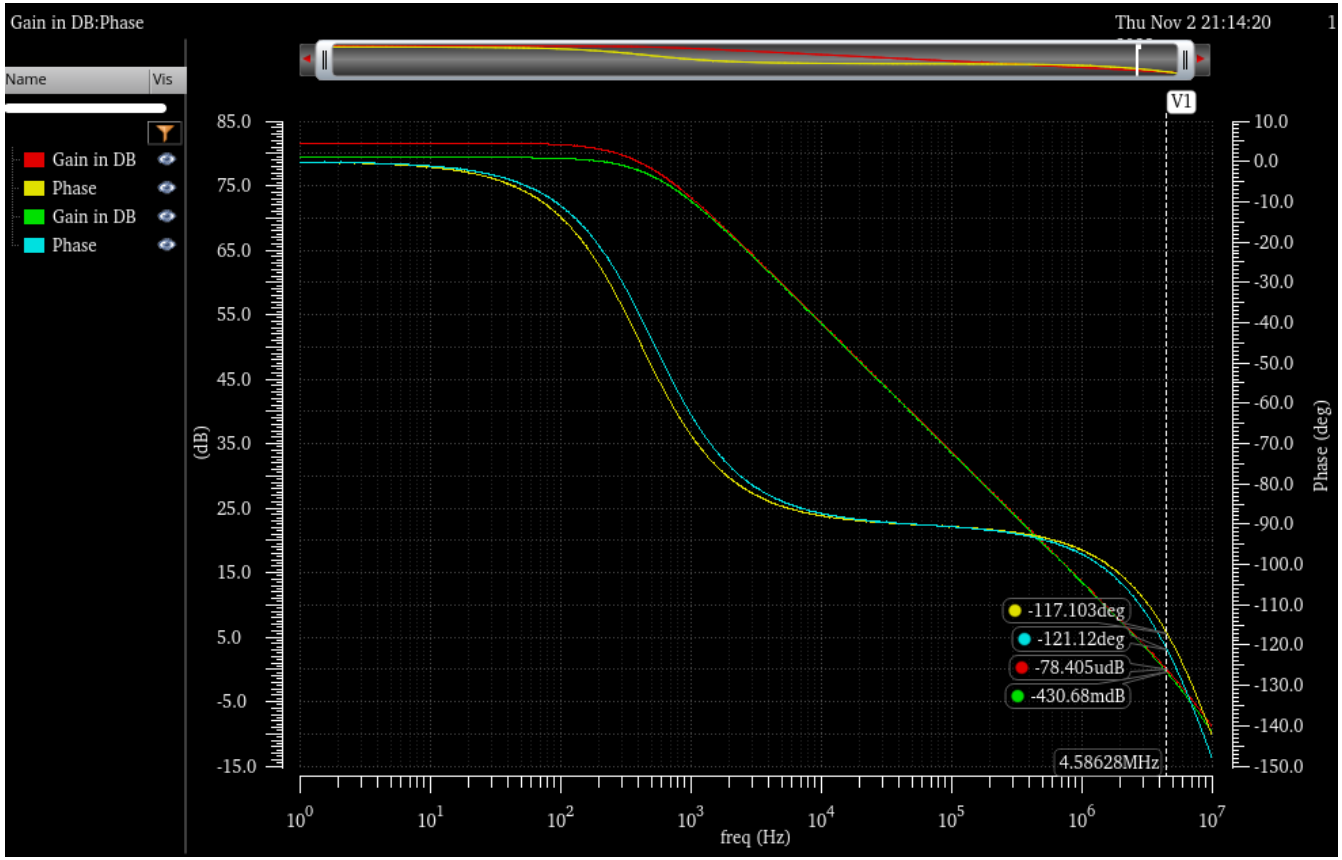
Post layout simulation

	Specification after Allen/Holberg	Design Result	Post Layout
Open Loop Gain in dB	77	81.6	79.4
Gain Bandwidth in MHz	0.976	4.59	4.40
Phasemargin in °	73	63°	60
Common Mode Range - in V	1.52	1.22	1.22
Common Mode Range + in V	-1.30	-1.3	-1.3
Settling Time in µs	0.77	0.21	0.22
Slew Rate in V/µs	1	5.51	5.46
Common Mode Rejection Ratio in dB	86.64	99.83	99.35
Offset in µV	80	7.22	13.83
S1, S2	1	3	3
S3, S4	1	1	1
S6	20	31	31
S7	20	35	35
S5	2	2	2
I5 in µA	2.21	10	10
Cc in µF	2.21	1.6	1.6

Miller OpAmp

Post layout simulation

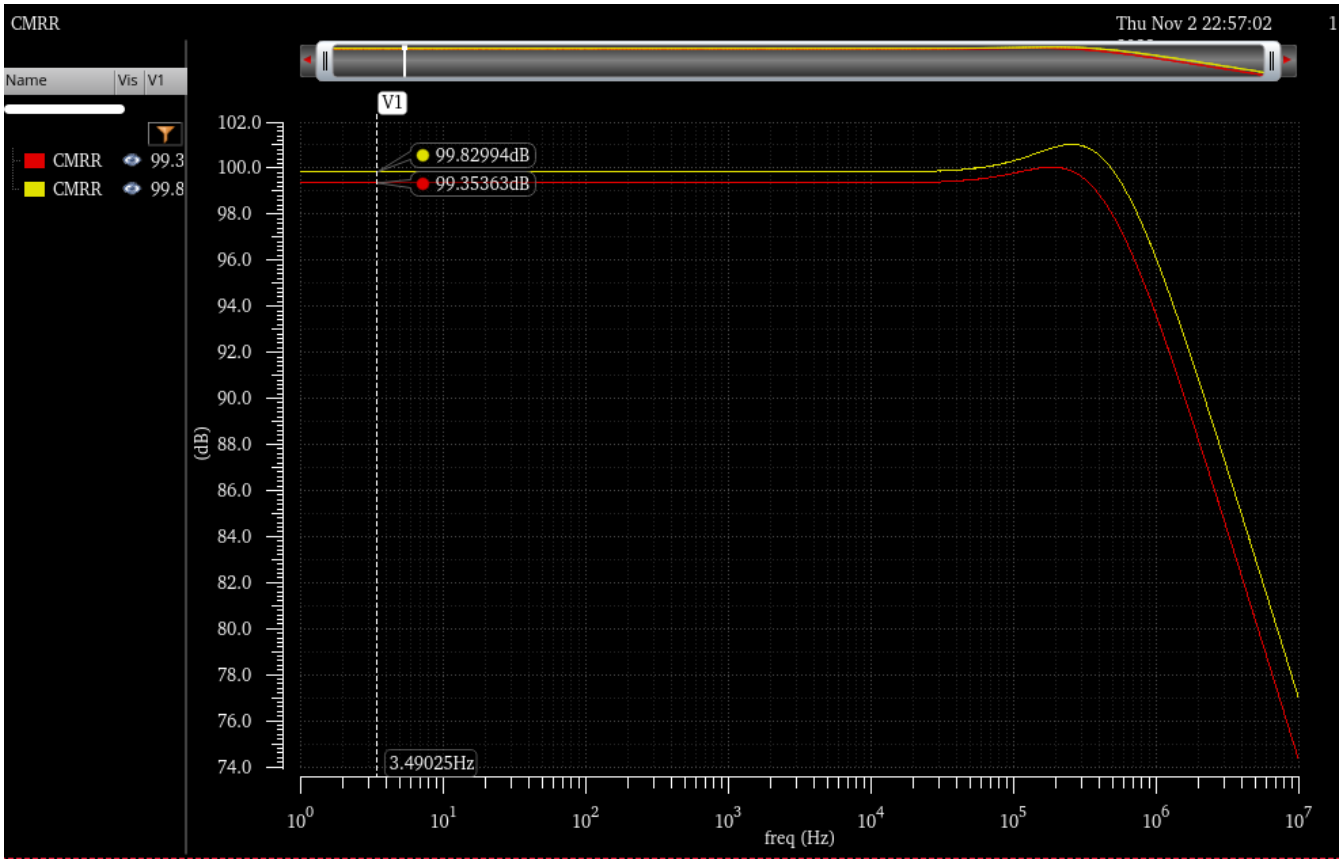
Open Loop Gain, Gain Bandwidth, Phase Margin



Miller OpAmp

Post layout simulation

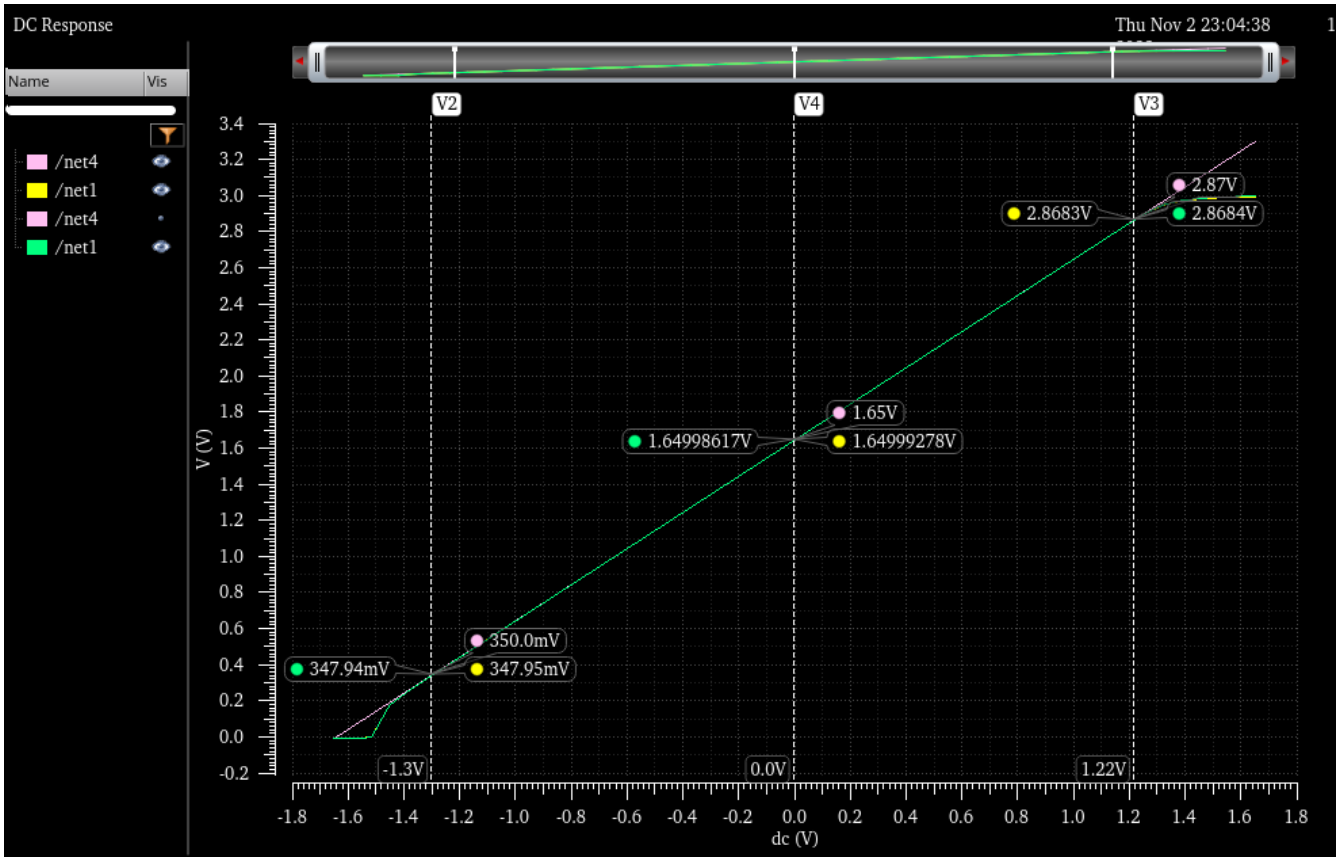
Common Mode Rejection Ratio



Miller OpAmp

Post layout simulation

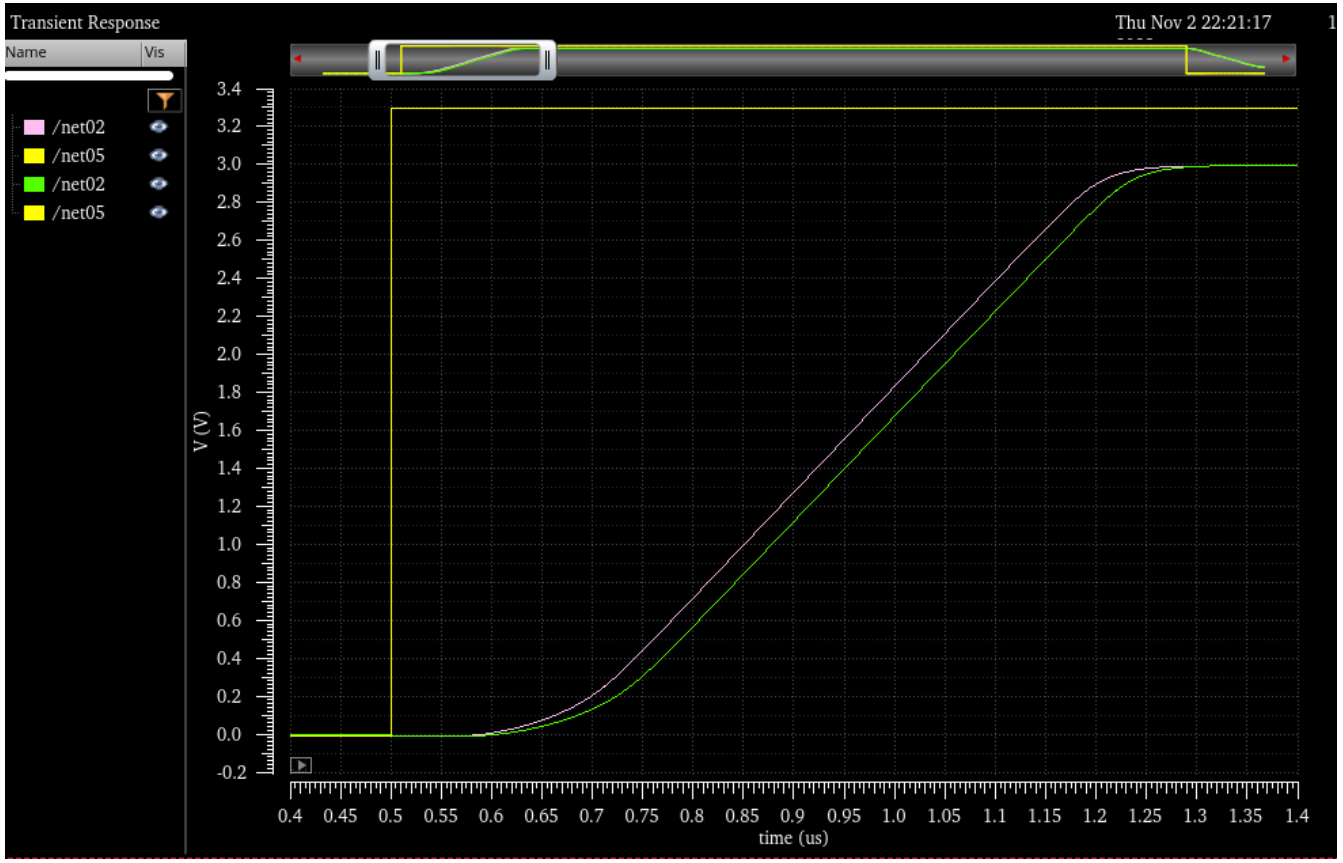
Input Common Mode Range, Offset



Miller OpAmp

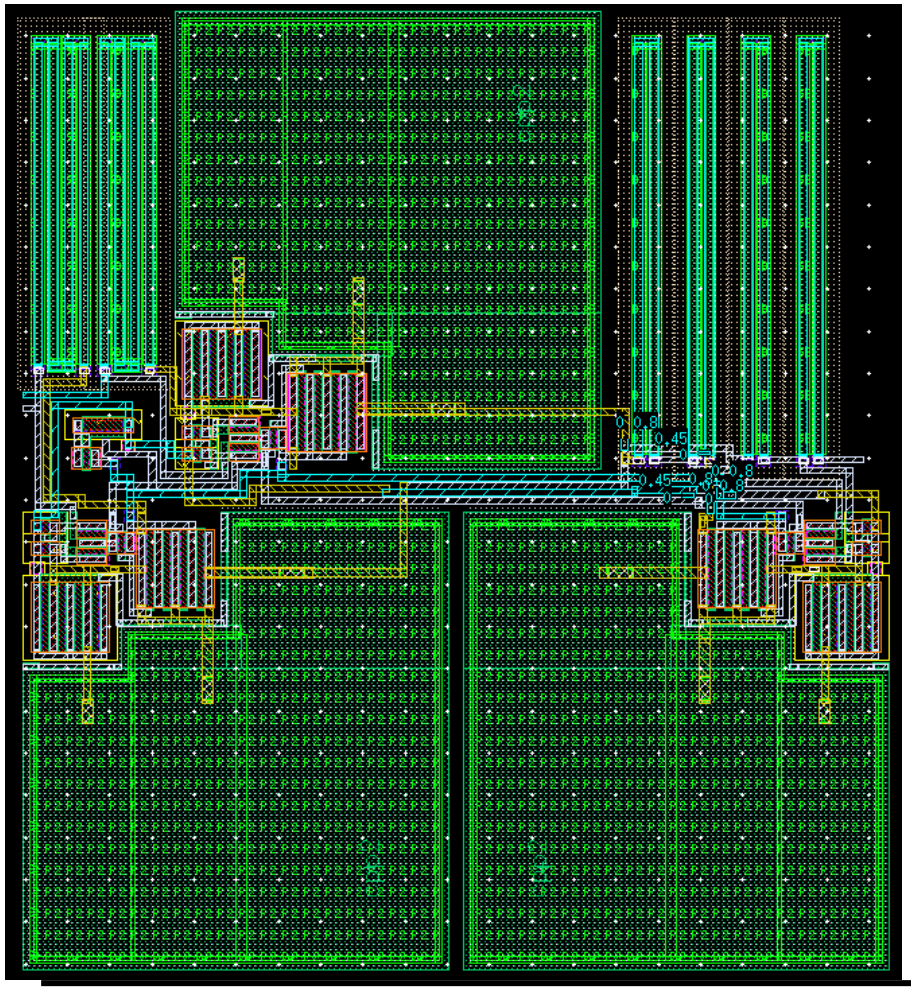
Post layout simulation

Slew Rate

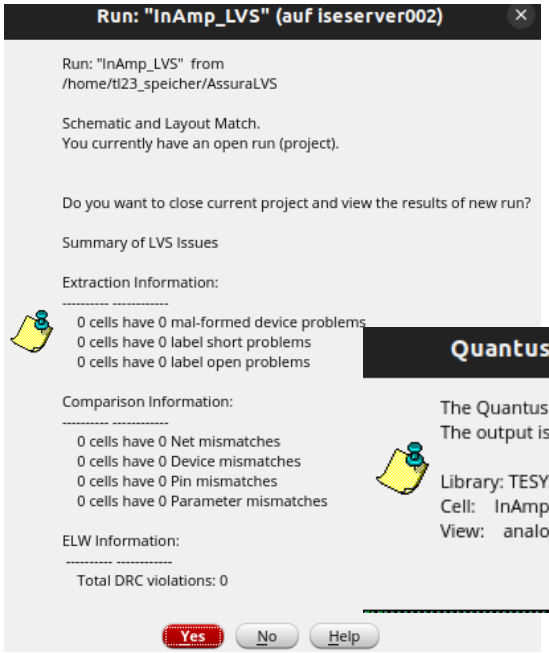


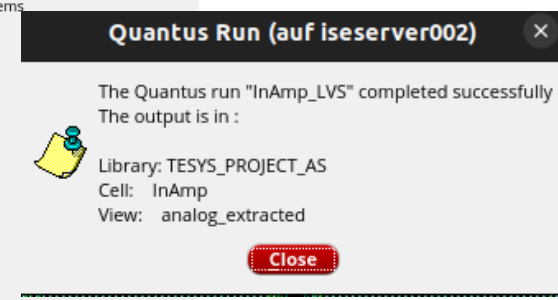
InAmp

Layout design



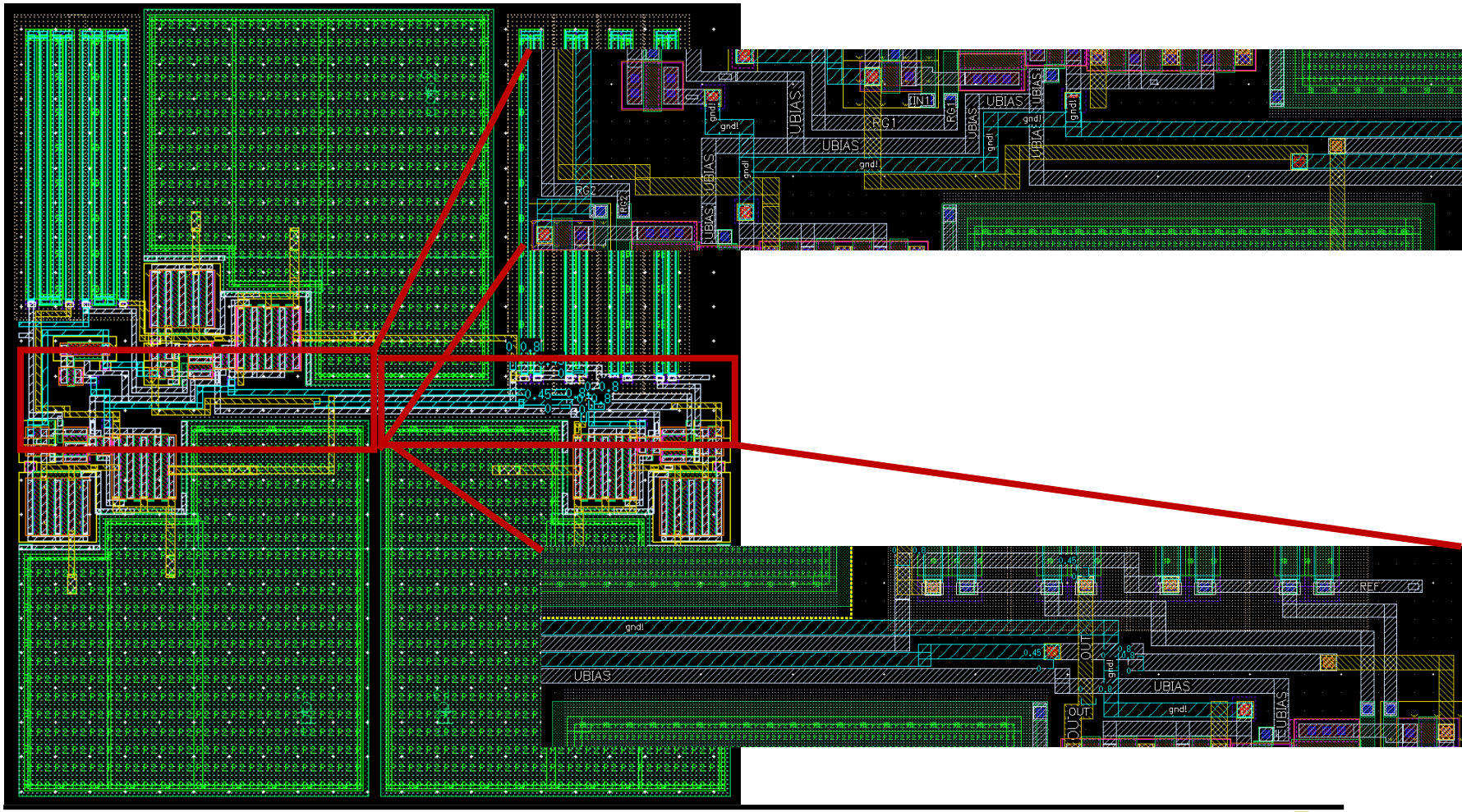
- Find optimal arrangement for short signal paths
- Minimize area by using minimum design rules





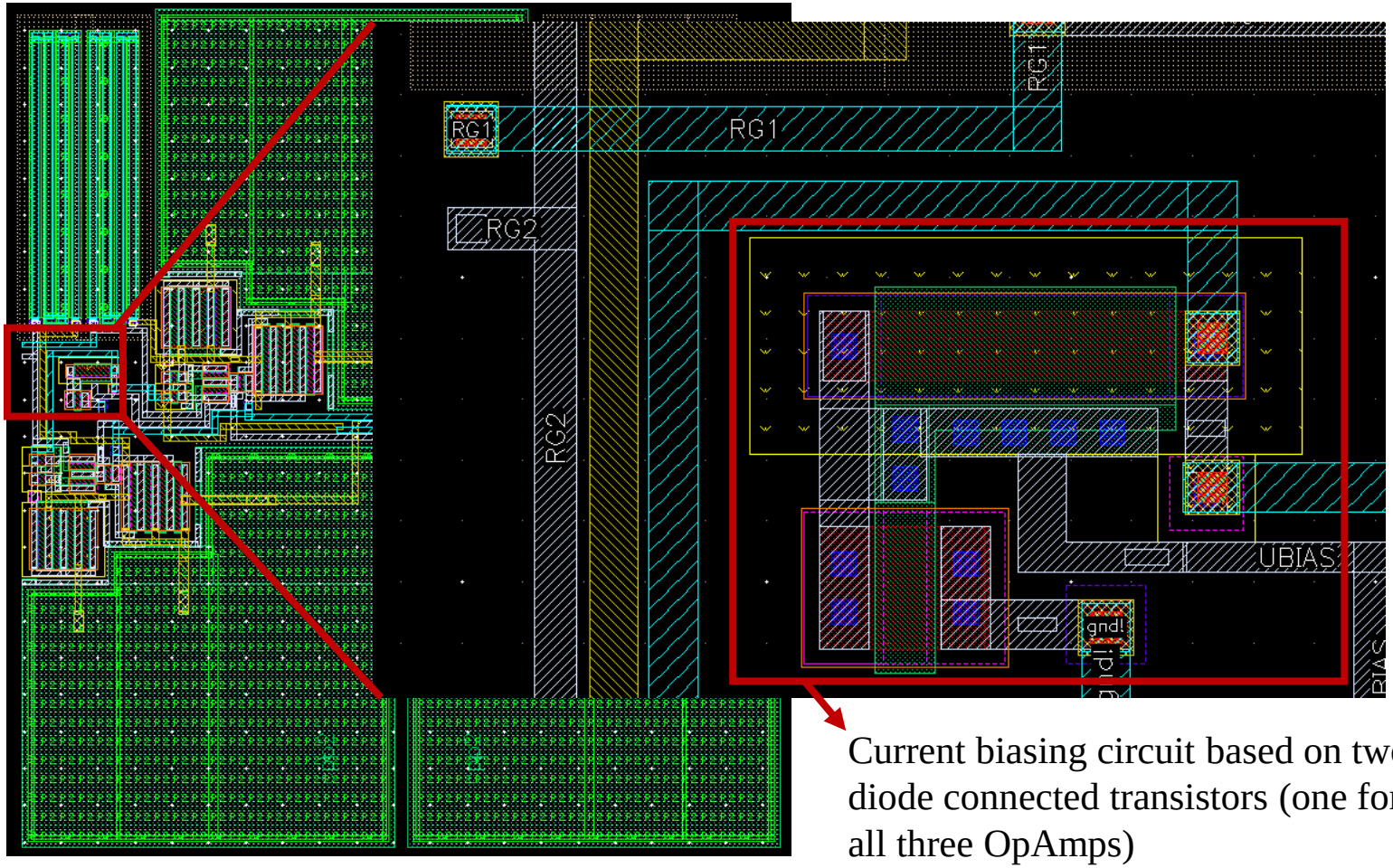
InAmp

Layout design



InAmp

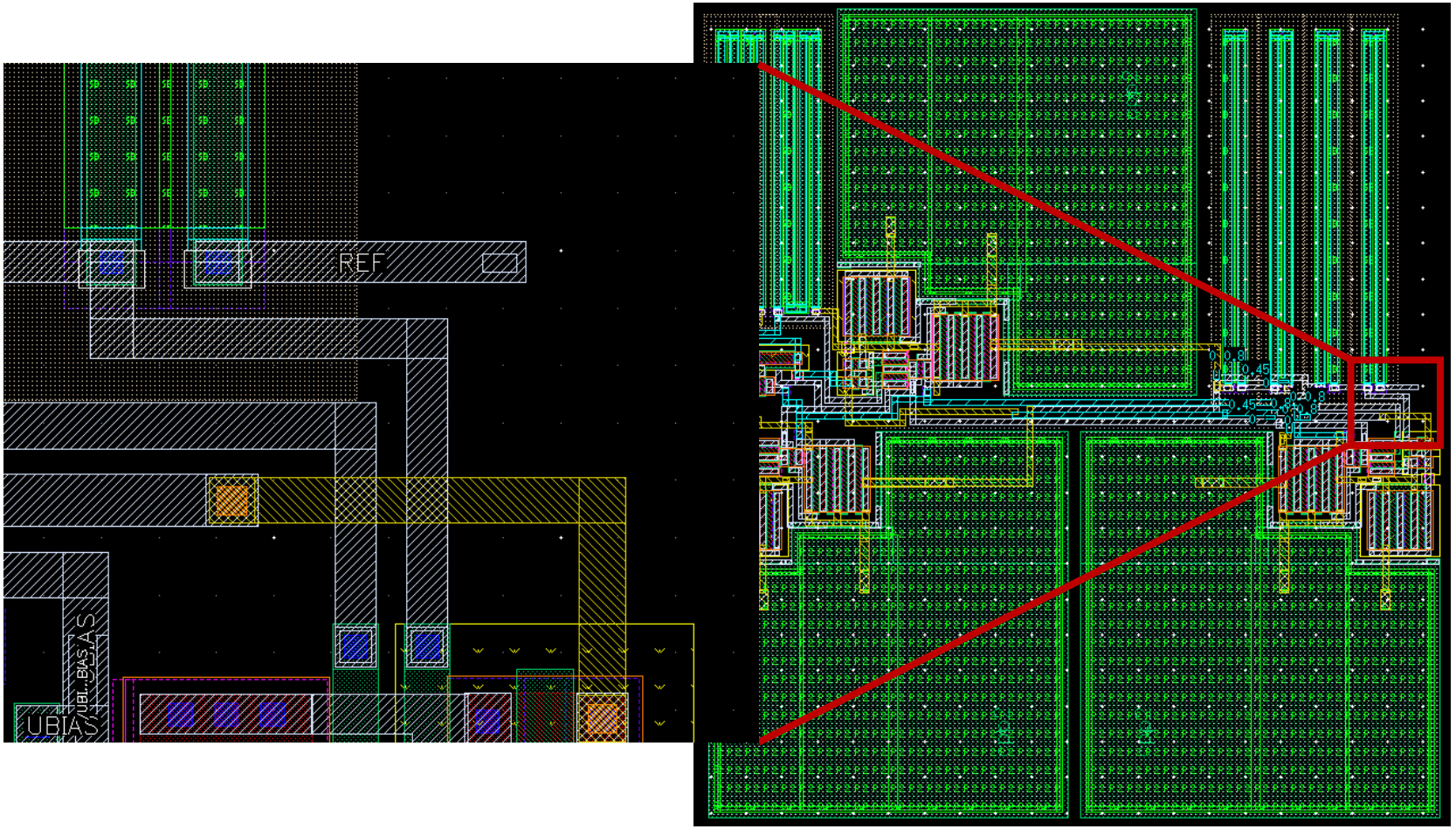
Layout design



Current biasing circuit based on two diode connected transistors (one for all three OpAmps)

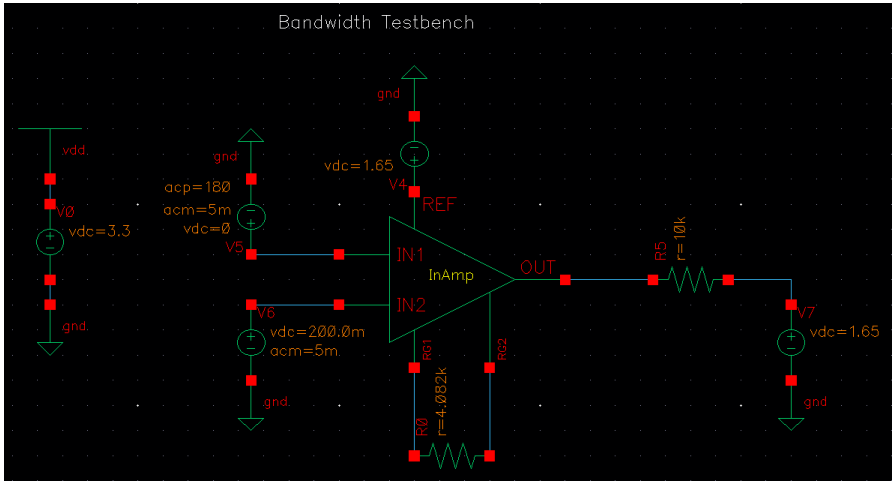
InAmp

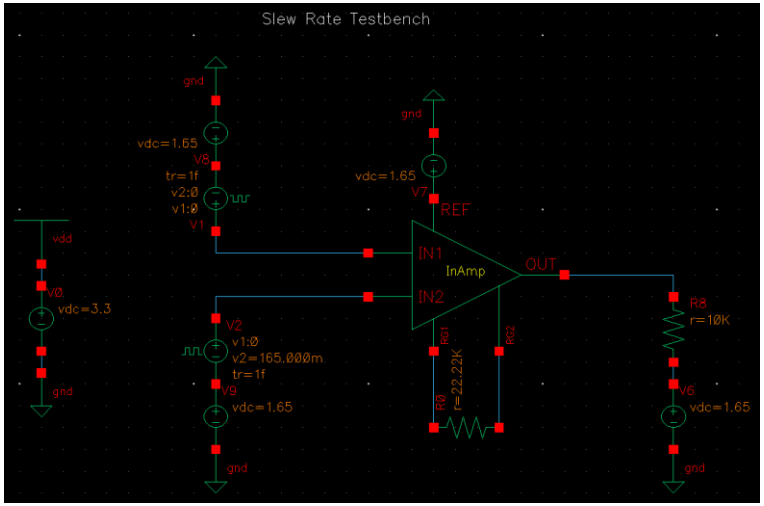
Layout design

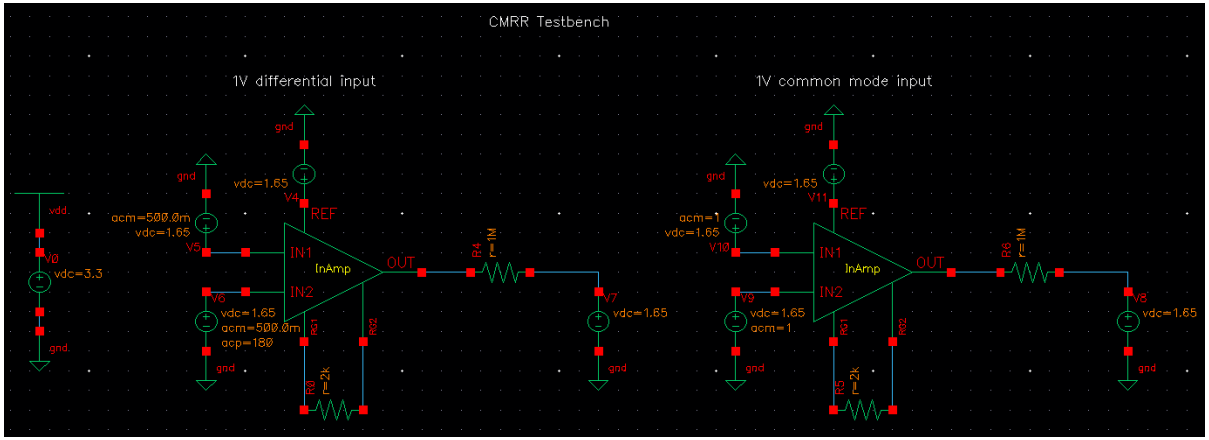


InAmp

Simulation schematics







InAmp

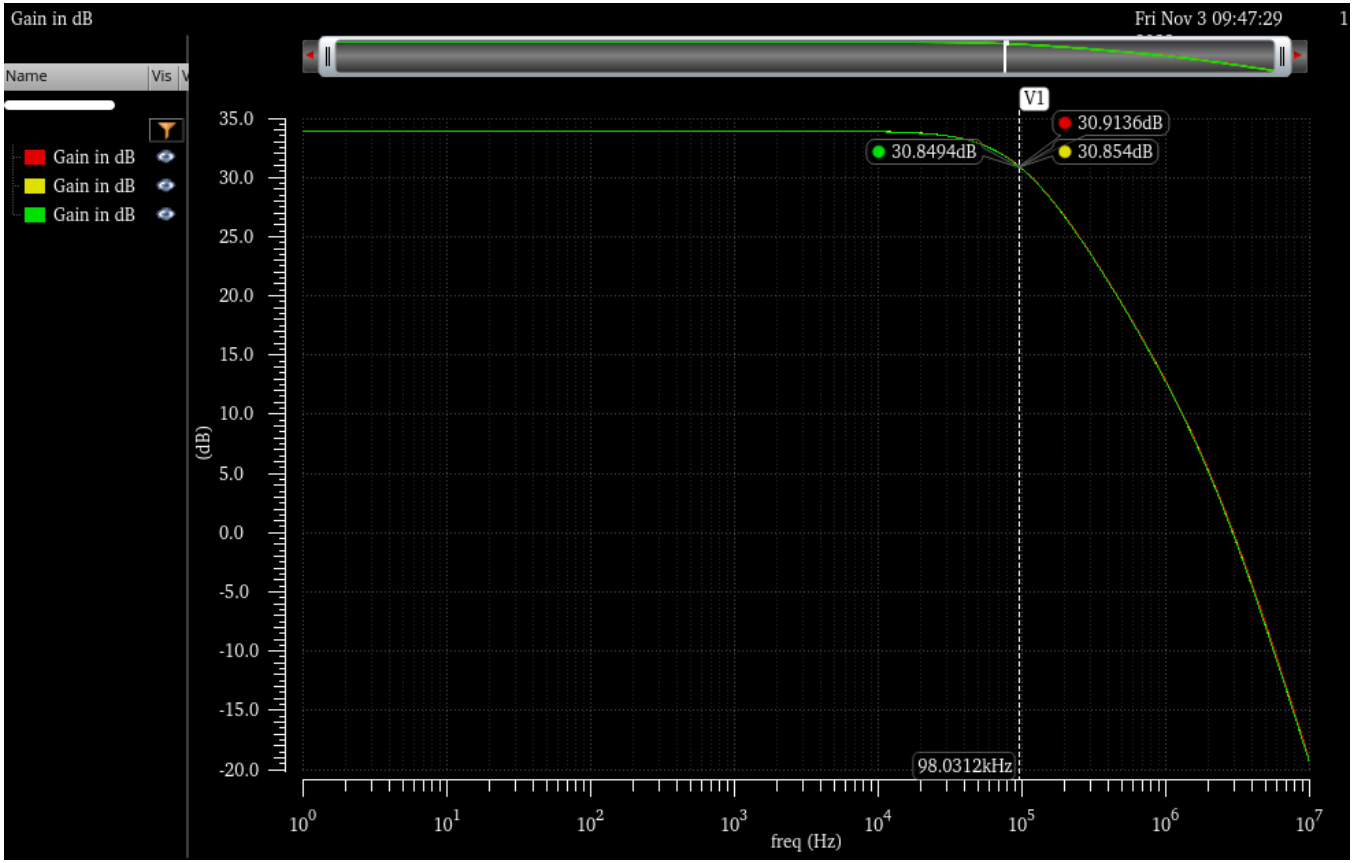
Post layout simulation and comparison to commercial InAmp

	Design Result	Post Layout (ideal connections)	Post Layout	INA350
Output Resistance	7.88	8.12	6.78	-
Slew Rate in V/µs	1.97	1.93	1.92	0.24
Common Mode Rejection Ratio in dB	122	121.8	126.5	95
Bandwidth in kHz, G=10	473	467	467	100
Bandwidth in kHz, G=50	98.03	96.67	96.57	25
Gain Error in % G=10	0.095	0.095	0.105	0.05
Gain Error in % G=50	0.19	0.2	0.22	0.082

InAmp

Post layout simulation

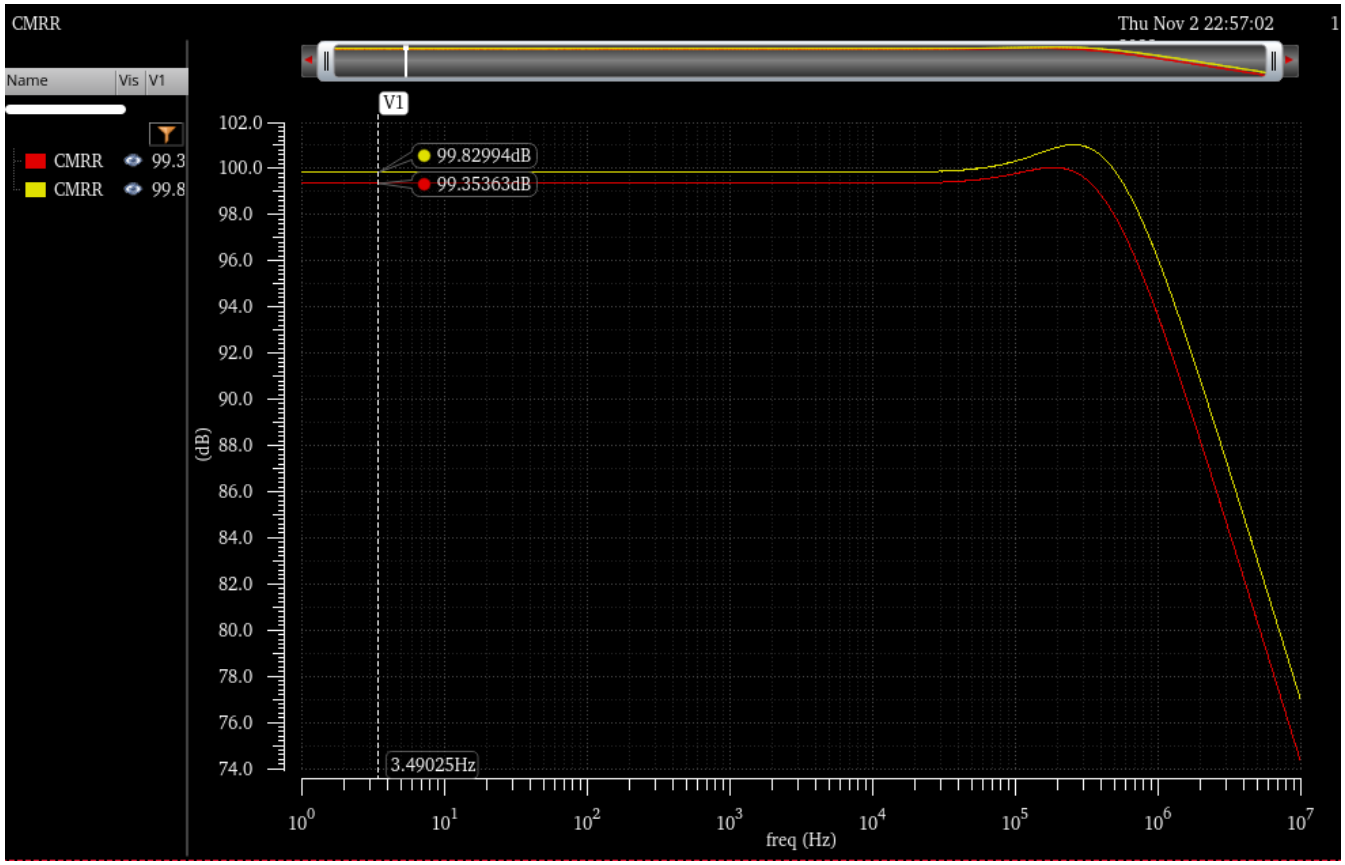
Bandwidth G=50



InAmp

Post layout simulation

Common Mode Rejection Ratio



Conclusion

- Miller type OpAmp reaches minimum specification, especially Phase Margin (after layout and extract)
- Successful design of current biasing circuit
- Final InAmp design outperforms commercially available INA350 (after layout and extract)
- Square footprint of final InAmp layout
- Possible improvements:
  - Matched resistors in InAmp layout

Thank You for your attention!

References

- Lecture and lab material of Elektronik II subject by Prof. Koenig
- Lecture and lab material of TESYS subject by Prof. Koenig