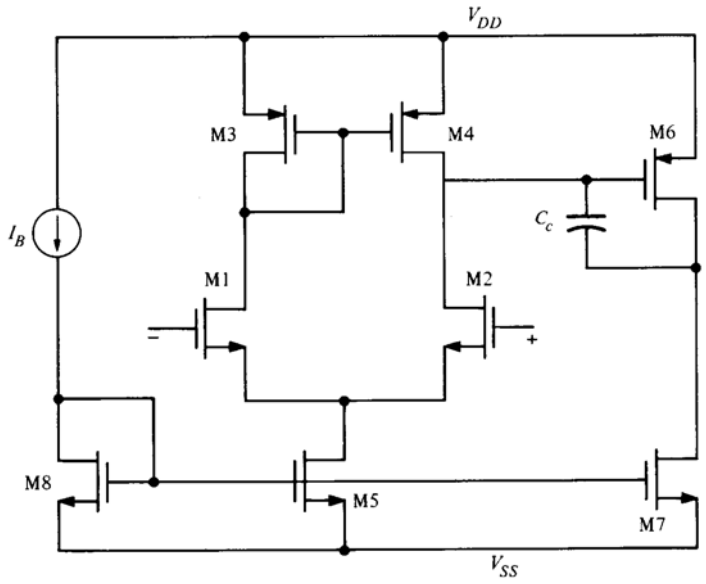
# Designing an Operational Amplifier

CAD-Laboratory
in Sensor Electronics

by Robert Freier

# Goal

- **Design of a differential amplifier: sizing and layout**
  - **for given specifications**
  - **0.351μm Austria Microsystems technology**
  - **precisely adjustable for use of high-speed operation**



# Overview

- Parameter calculation according to Allen/Holberg design plan
- Simulation
  - adjust values if necessary
  - optimize for high-speed operation / slew rate
- Inclusion of scalable transistors
  - precise adjustment / optimization
- Simulation
- Layout drawing
- Simulation / verification

# Parameter Calculation

**compensation capacitance:**

$$C_C > 0.29 C_L$$

**tail current:**

$$I_5 = SR \cdot C_C$$

**Transistor M3:**

$$S_3 = \frac{W_3}{L_3} = \frac{2 I_3}{K'_3 \left[ V_{DD} - V_{in}(\max) - \left| V_{T03} \right| (\max) + V_{T1}(\min) \right]^2} \geq 1$$

**Transistors M1 + M2:**

$$g_{m1} = GB \cdot C_C \Rightarrow S_1 = S_2 = \frac{g_{m2}^{\ 2}}{K_2' I_5}$$

# Parameter Calculation

**Transistor M5:**

$$V_{DS5}(sat) = V_{in}(\min) - V_{SS} - \sqrt{\frac{I_5}{\beta_1}} - V_{T1}(\max) \geq 100mV$$

$$S_5 = \frac{2I_5}{K_5'\left[V_{DS5}(sat)\right]^2}$$

**Transistor M6:**

$$g_{m6} = 2.9 g_{m2} \frac{C_L}{C_C}$$

$$S_6 = \frac{g_{m6}}{K_6' V_{DS6}(sat)}$$

# Parameter Calculation

**Transistor M7:**

$$I_6 = \frac{g_{m6}^{\ 2}}{2K_6' V_{DS6}(sat)}$$

$$S_7 = \frac{I_6}{I_5} S_5$$

**Check gain and power dissipation:**

$$A_V = \frac{2g_{m2}g_{m6}}{I_5(\lambda_2 + \lambda_4) I_6(\lambda_6 + \lambda_7)}$$

$$P_{diss} = (I_5 + I_6)(V_{DD} + |V_{SS}|)$$

# Simulation

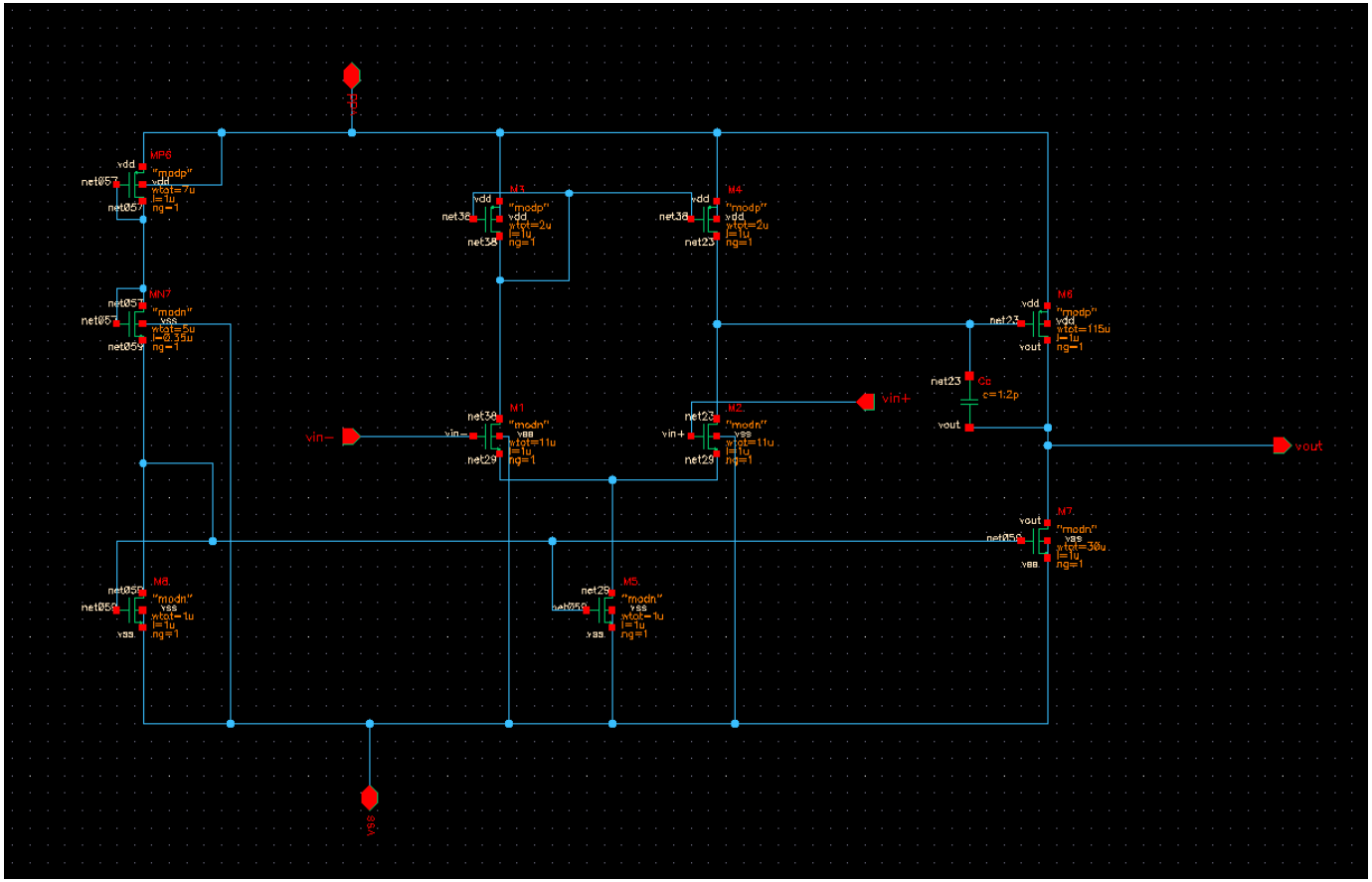
***Simulation delivers results far from desired specifications!***

⇒ ***adjust values manually***
***(with respect to above mentioned relations)***

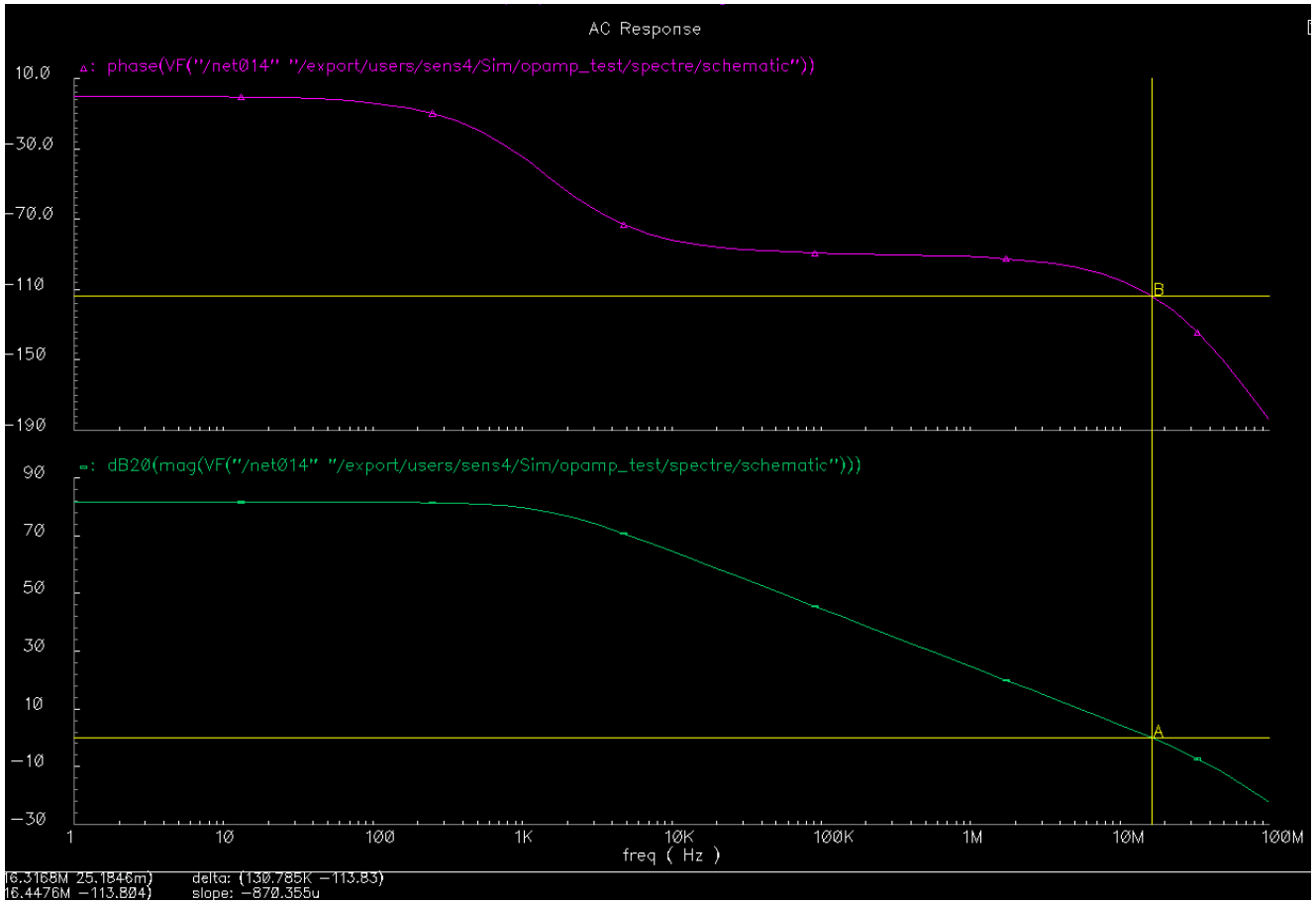
⇒ ***optimize slew rate***

| | S1 | S2 | S3 | S4 | S5 | S6 | S7 | $C_C$ |
|---|---|---|---|---|---|---|---|---|
| **calculated** | 1 | 1 | 1 | 1 | 1 | 2 | 63 | 1,43pF |
| **adjusted** | 11 | 11 | 2 | 2 | 1 | 115 | 30 | 1,2pF |

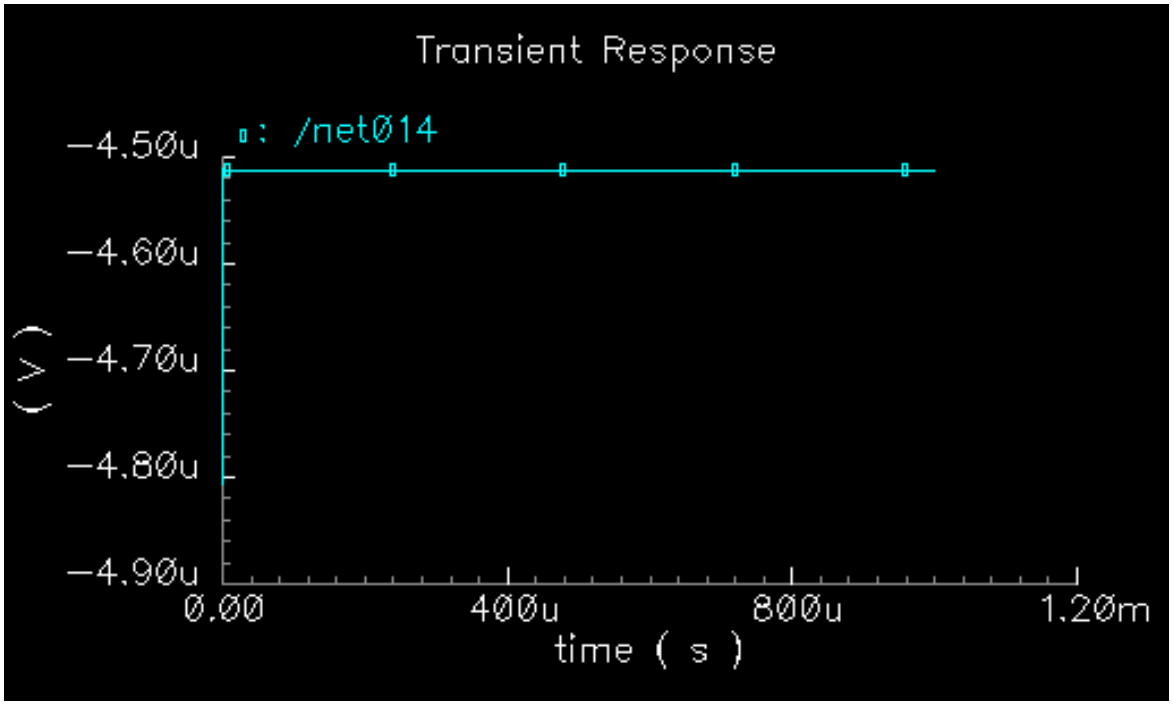
# Circuit


vdd
MP6
"mpdp"
net057
M3
net38
M4
net23
MN7
"mndn"
vss
M6
vout
Cc
c=1.2p
vin+
vin−
M1
M2
net29
M7
net050
M8
M5
vss

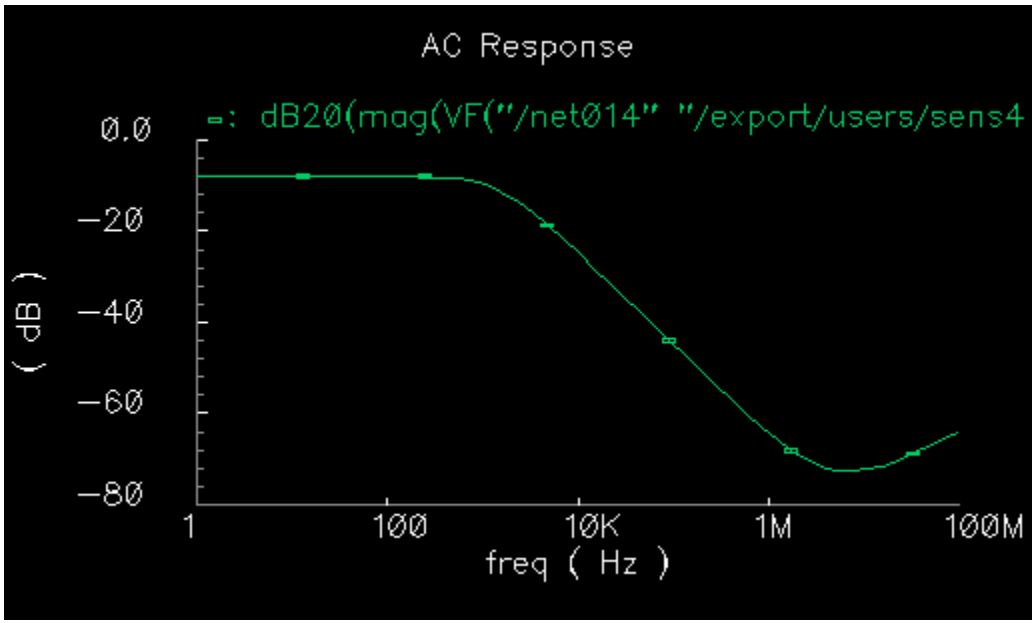
# Bode plot


AC Response
phase(VF("/net014" "/export/users/sens4/Sim/opamp_test/spectre/schematic"))
10.0
-30.0
-70.0
-110
-150
-190
B
dB20(mag(VF("/net014" "/export/users/sens4/Sim/opamp_test/spectre/schematic")))
90
70
50
30
10
-10
-30
A
1
10
100
1K
10K
100K
1M
10M
100M
freq ( Hz )
16.3168M 25.1846m)
16.4476M -113.804)
delta: (130.785K -113.83)
slope: -870.355u

# Offset


Transient Response
: /net014
−4.50u
−4.60u
−4.70u
−4.80u
−4.90u
( V )
0.00
400u
800u
1.20m
time ( s )

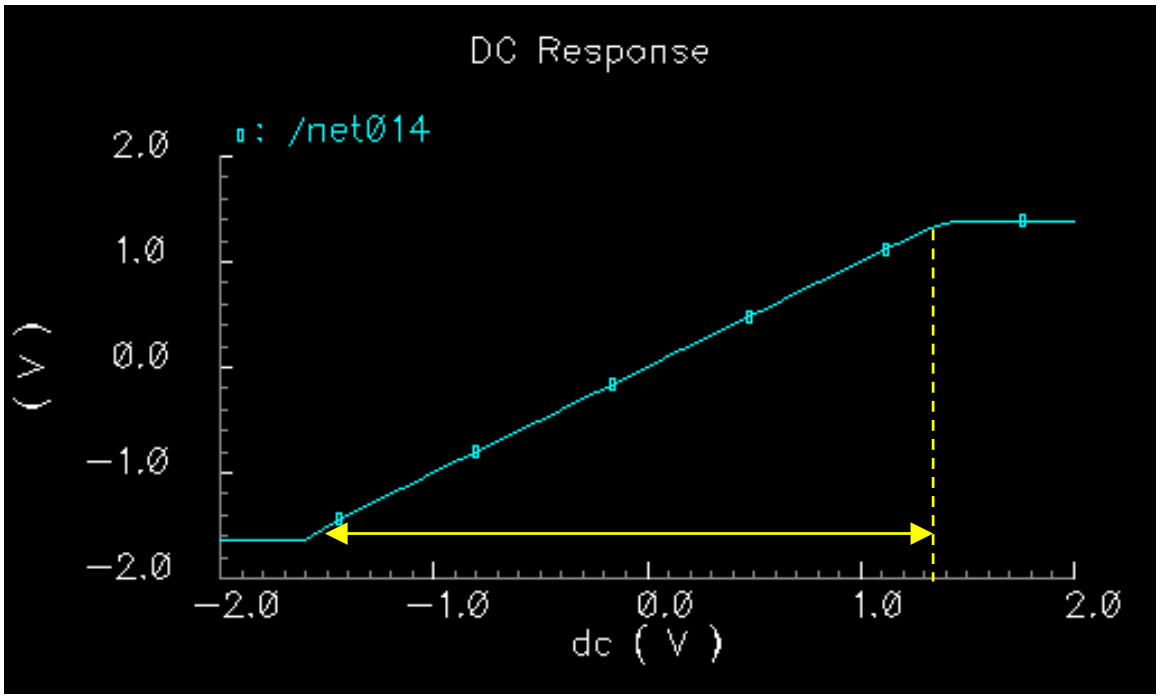
# CMRR



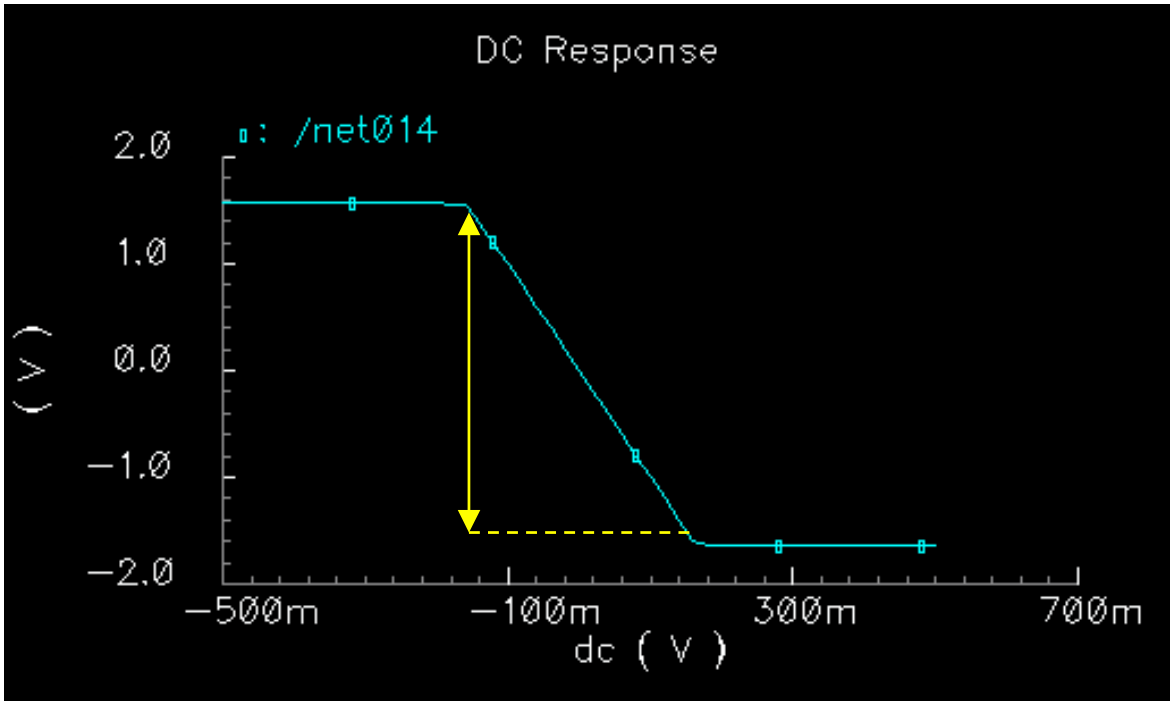

***common mode gain***

**CMRR = (differential-mode gain) – (common-mode gain)**

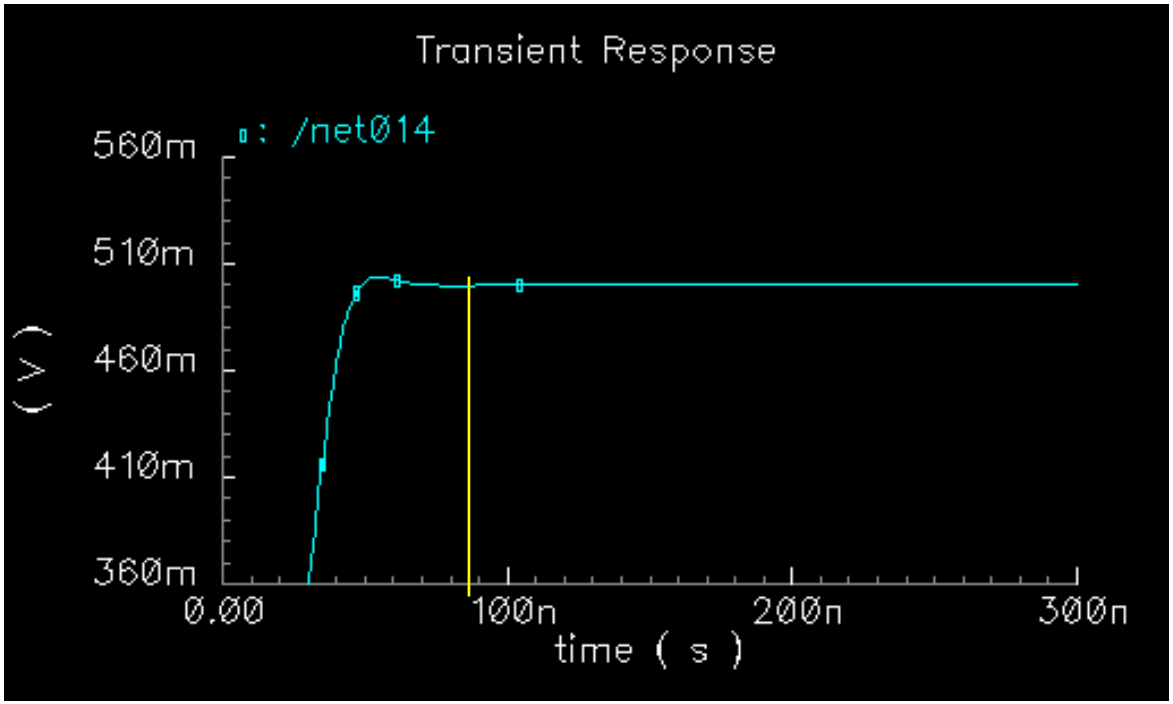
# Input CMR



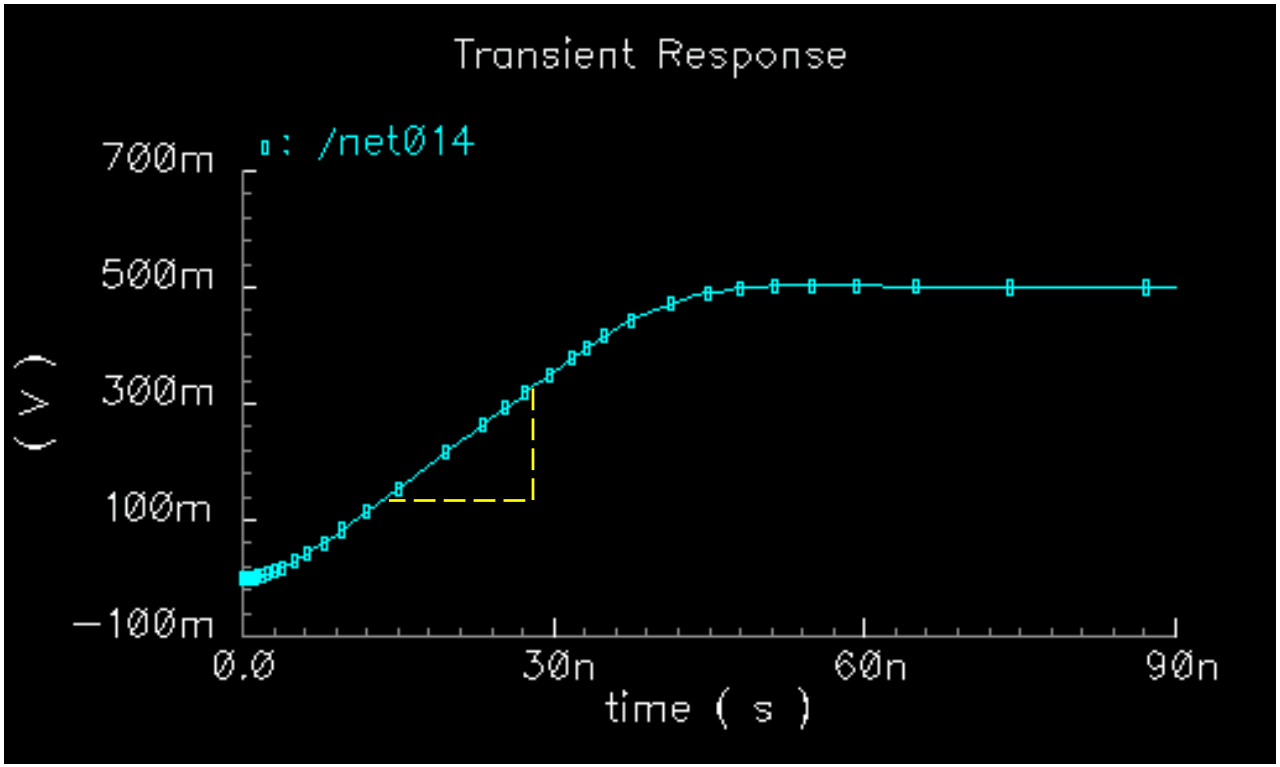
# Output Swing



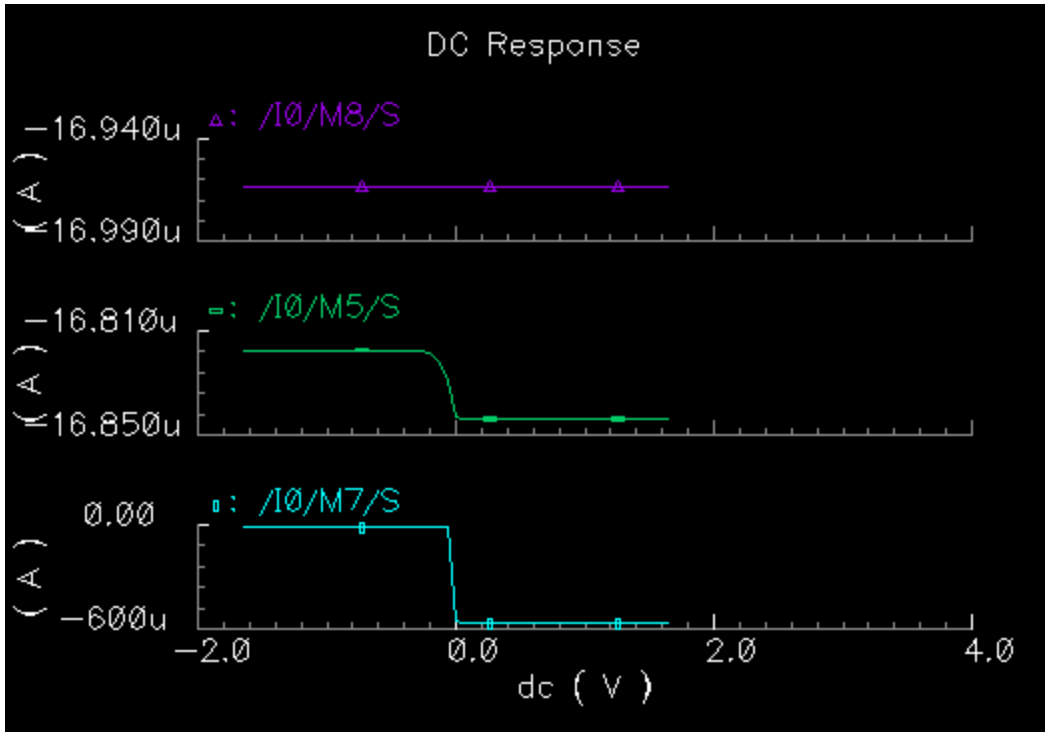
# Settling Time



# Slew Rate


Transient Response
: /net014
700m
500m
300m
100m
−100m
( V )
0.0
30n
60n
90n
time ( s )

# Power dissipation



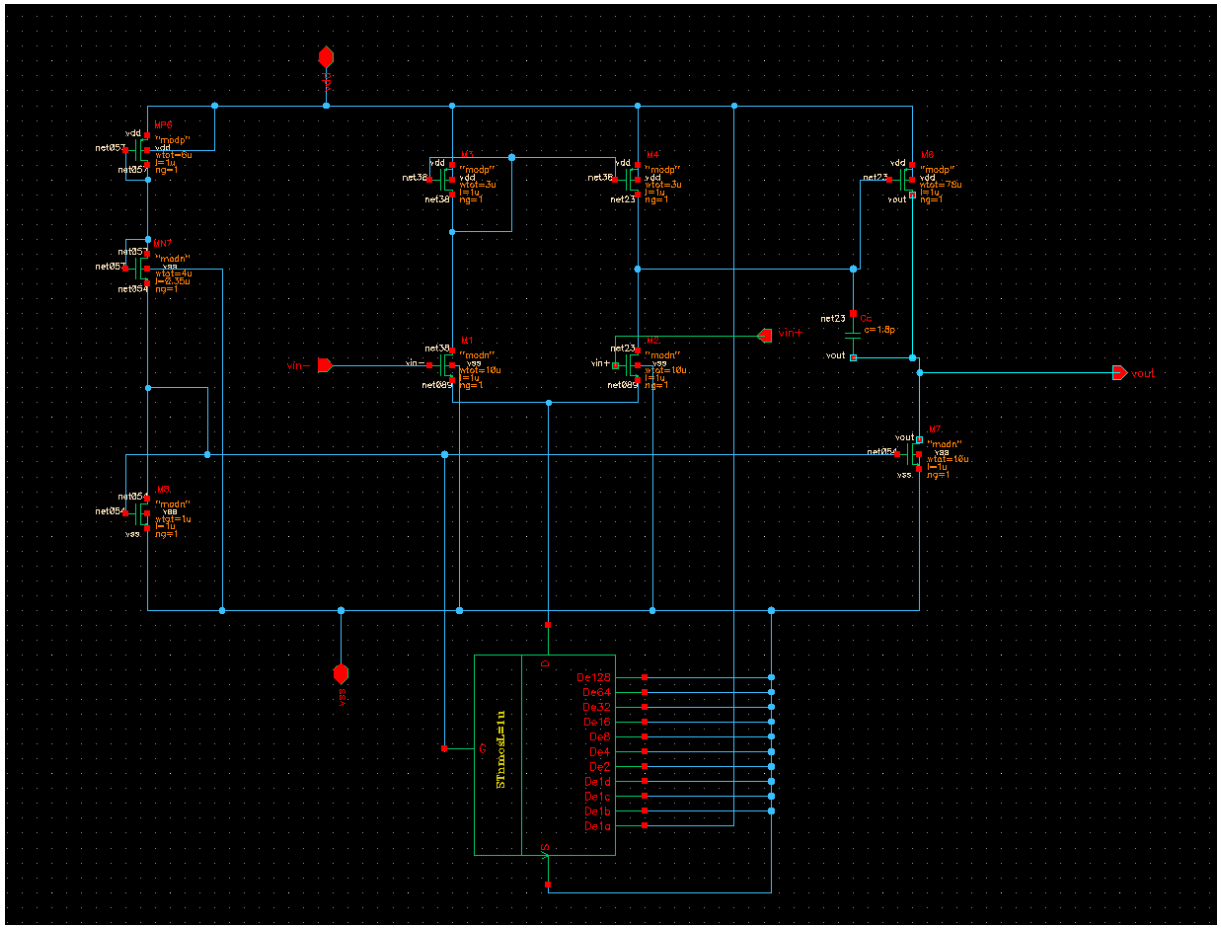

$$P_{diss} = 3.3V \cdot I_{diss}$$

# Integration of scalable transistors

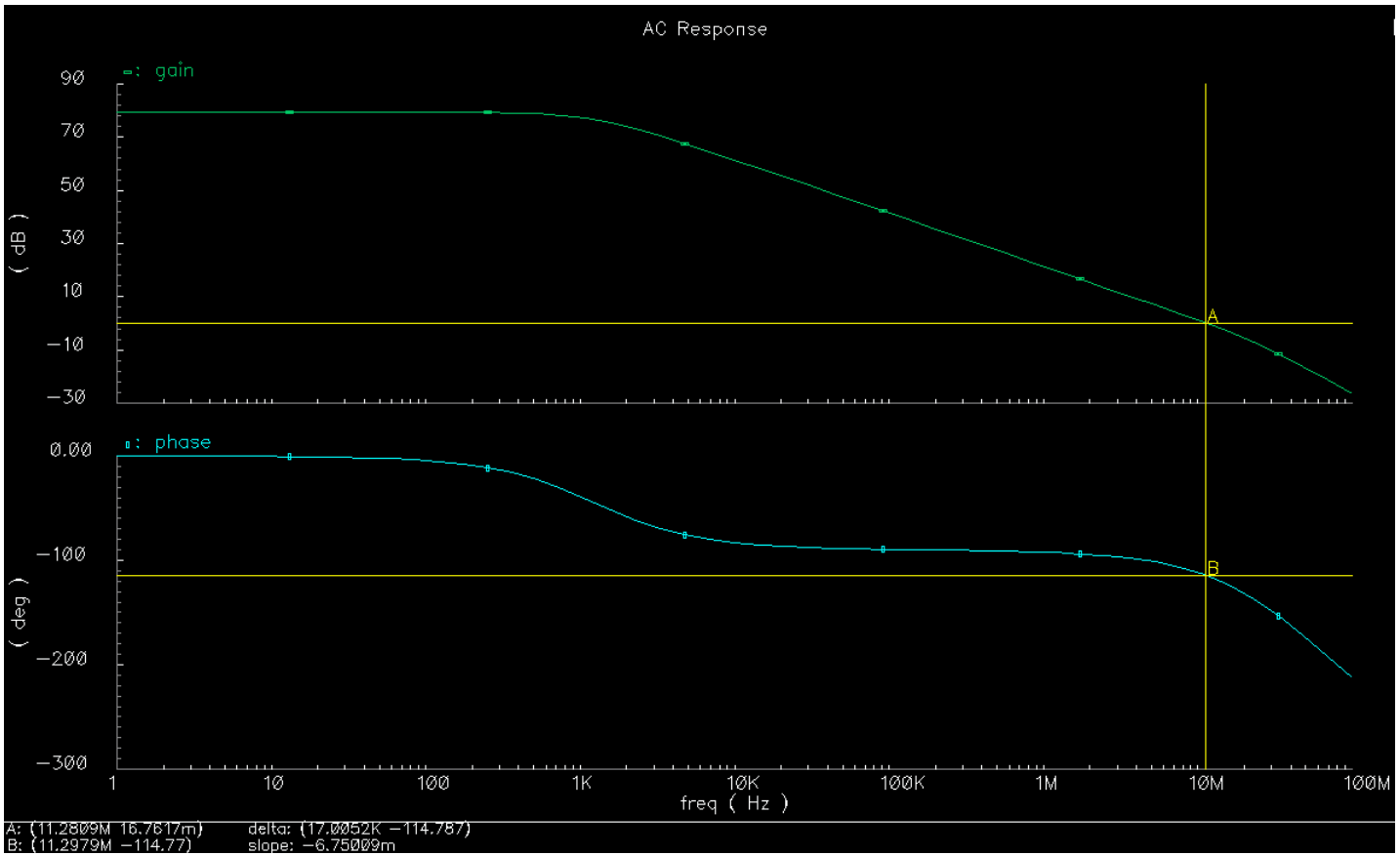
- **Integration of two scalable transistors**
  - ⇒ ***leads to poor simulation results***
  - ⇒ ***unable to achieve requirements***

- **Integration of only one scalable transistor**
  - ⇒ ***readjust values***

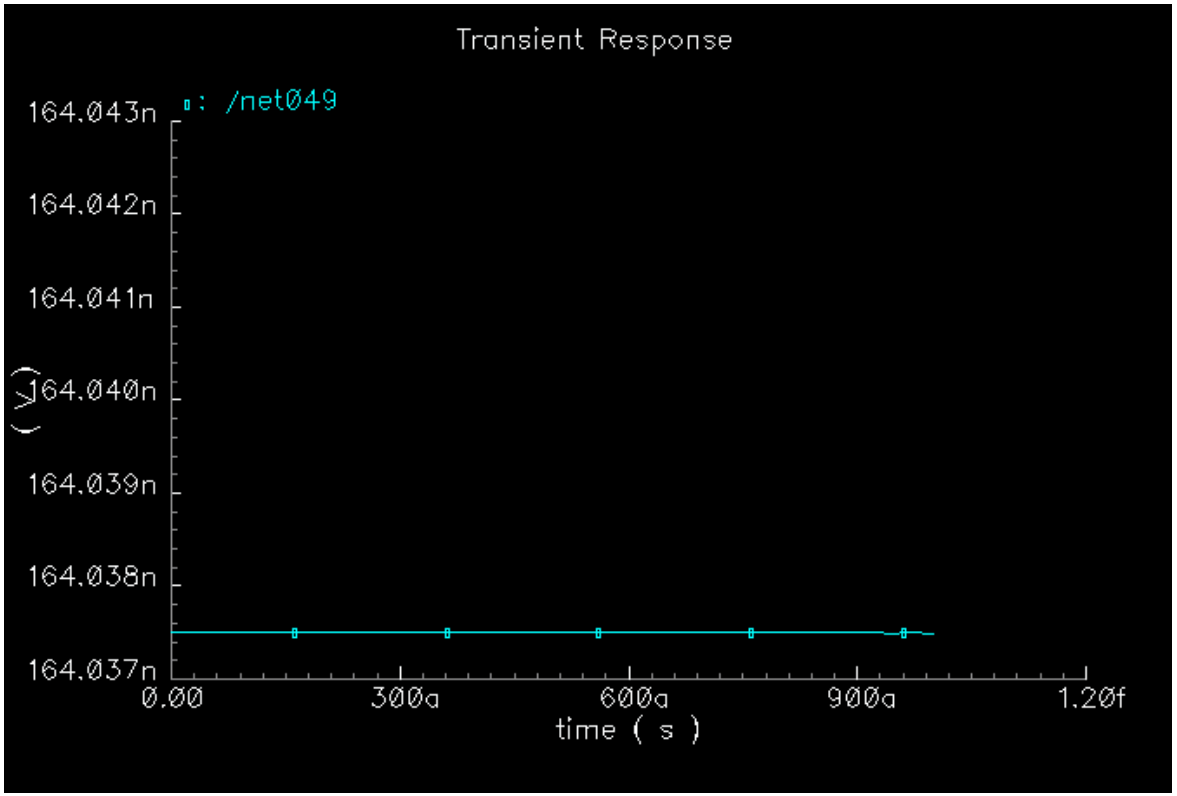
# Circuit with scalable device



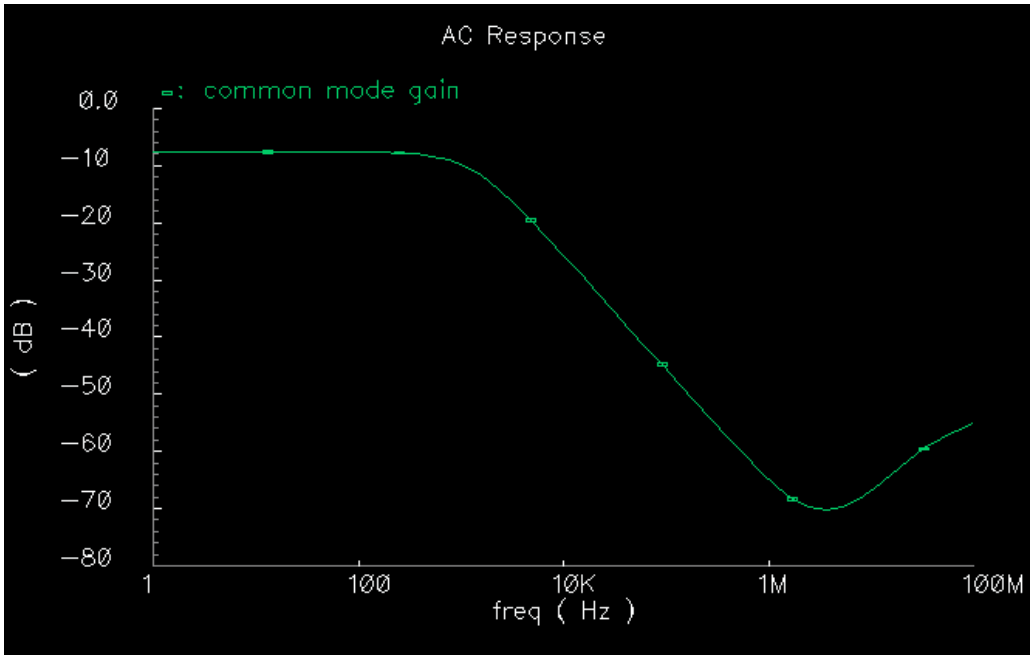
# Bode plot


AC Response
gain
90
70
50
30
10
−10
−30
( dB )
A
phase
0.00
−100
−200
−300
( deg )
B
1
10
100
1K
10K
100K
1M
10M
100M
freq ( Hz )
A: (11.2809M 16.7617m)
B: (11.2979M −114.77)
delta: (17.0052K −114.787)
slope: −6.75009m

# Offset


Transient Response
: /net049
164.043n
164.042n
164.041n
164.040n
164.039n
164.038n
164.037n
0.00
300a
600a
900a
1.20f
time ( s )

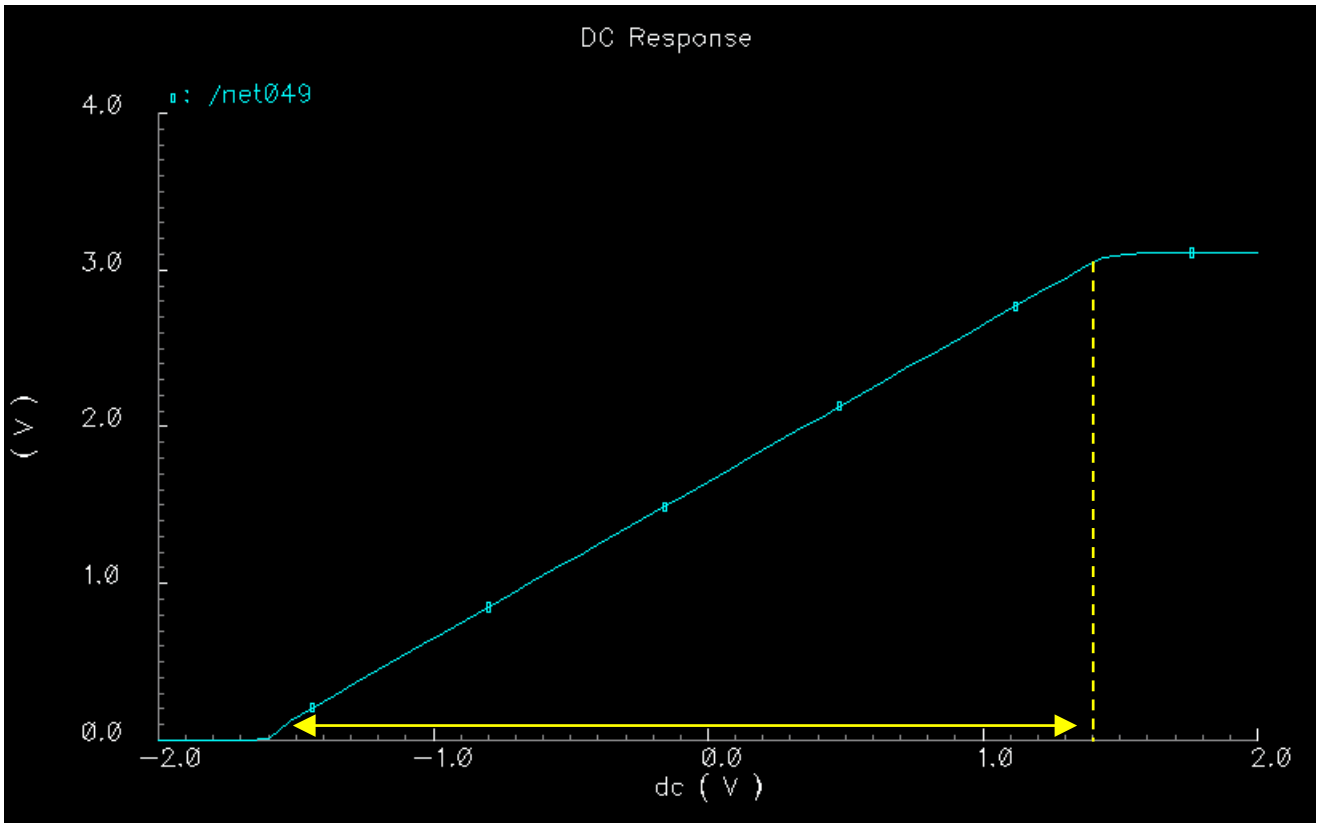
# CMRR



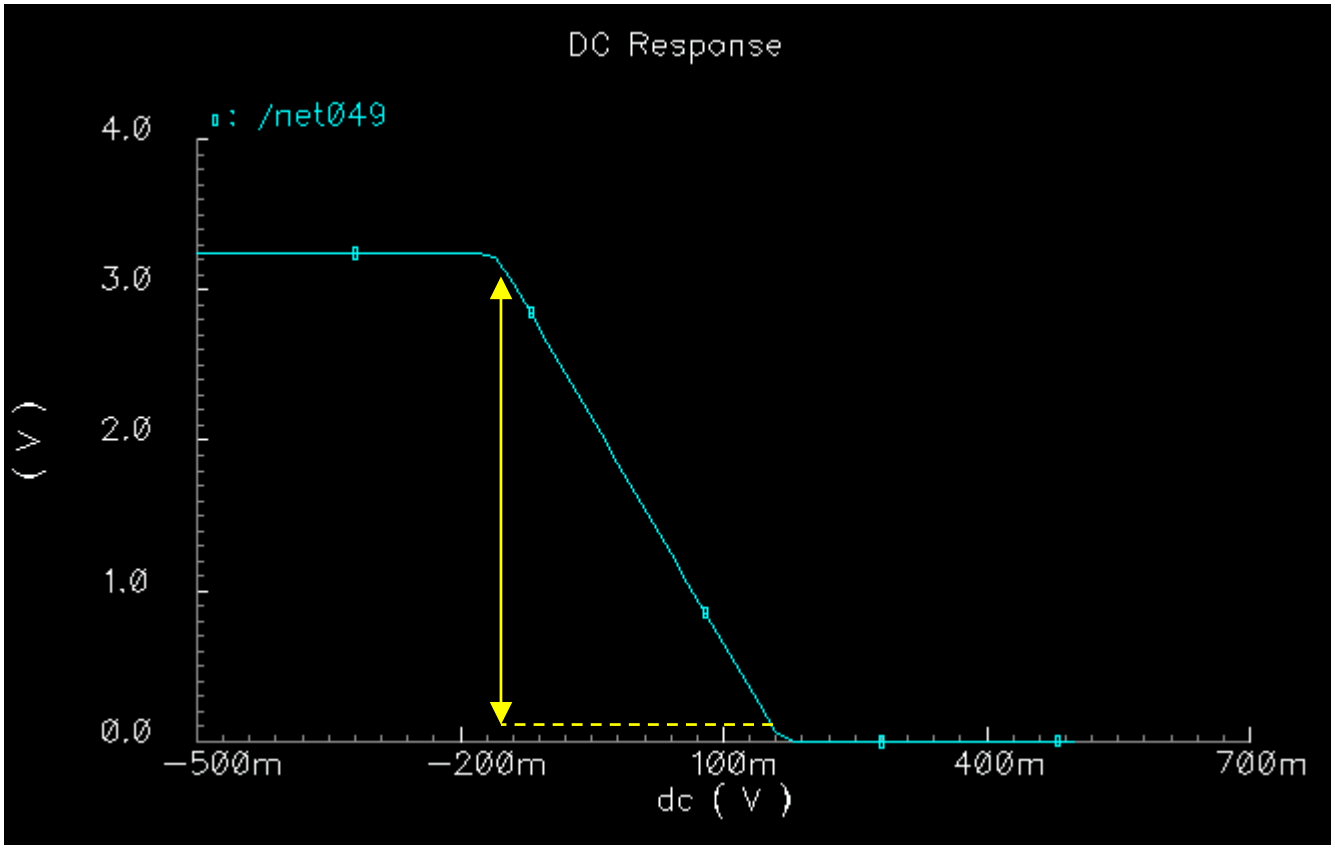

***common mode gain***

**CMRR = (differential-mode gain) – (common-mode gain)**

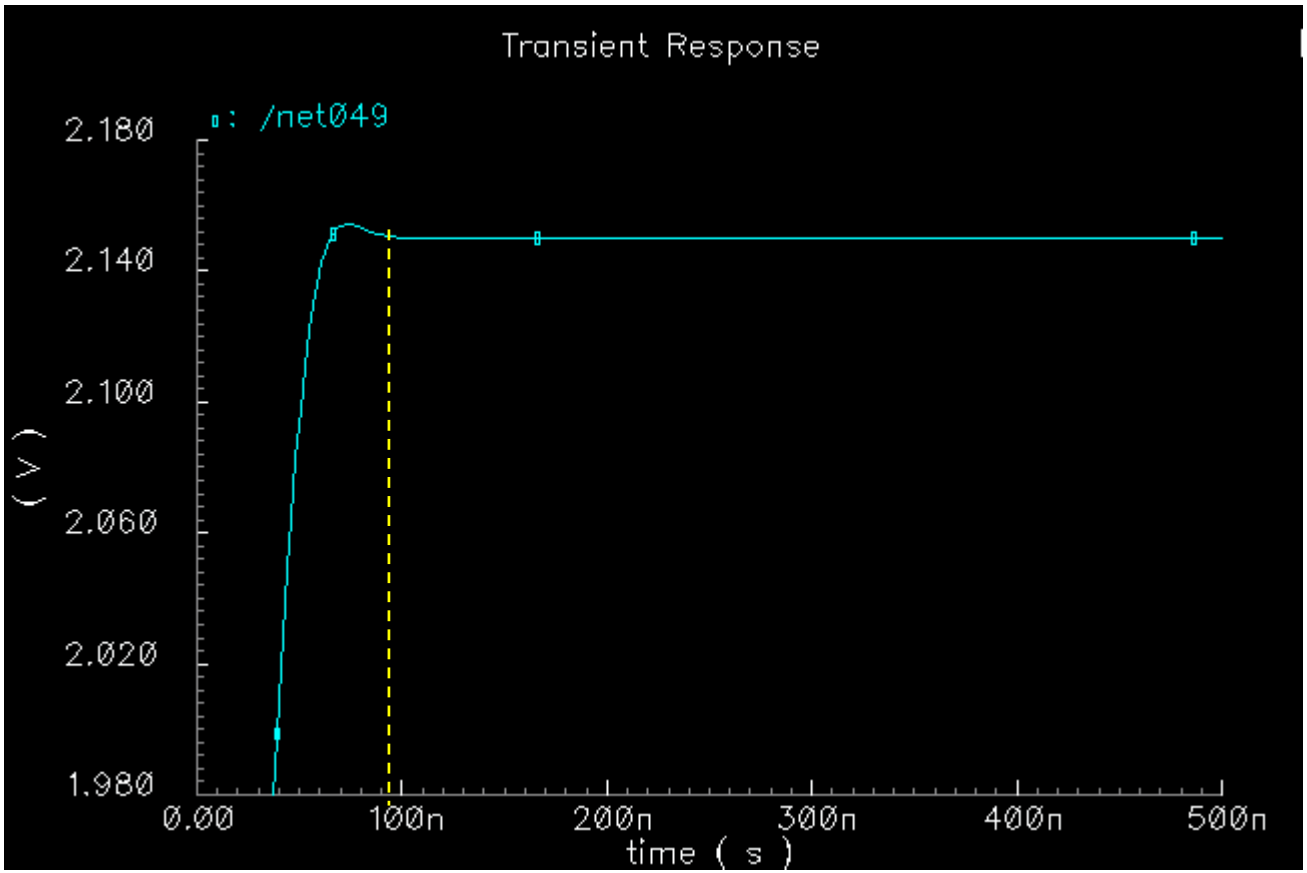
# Input CMR



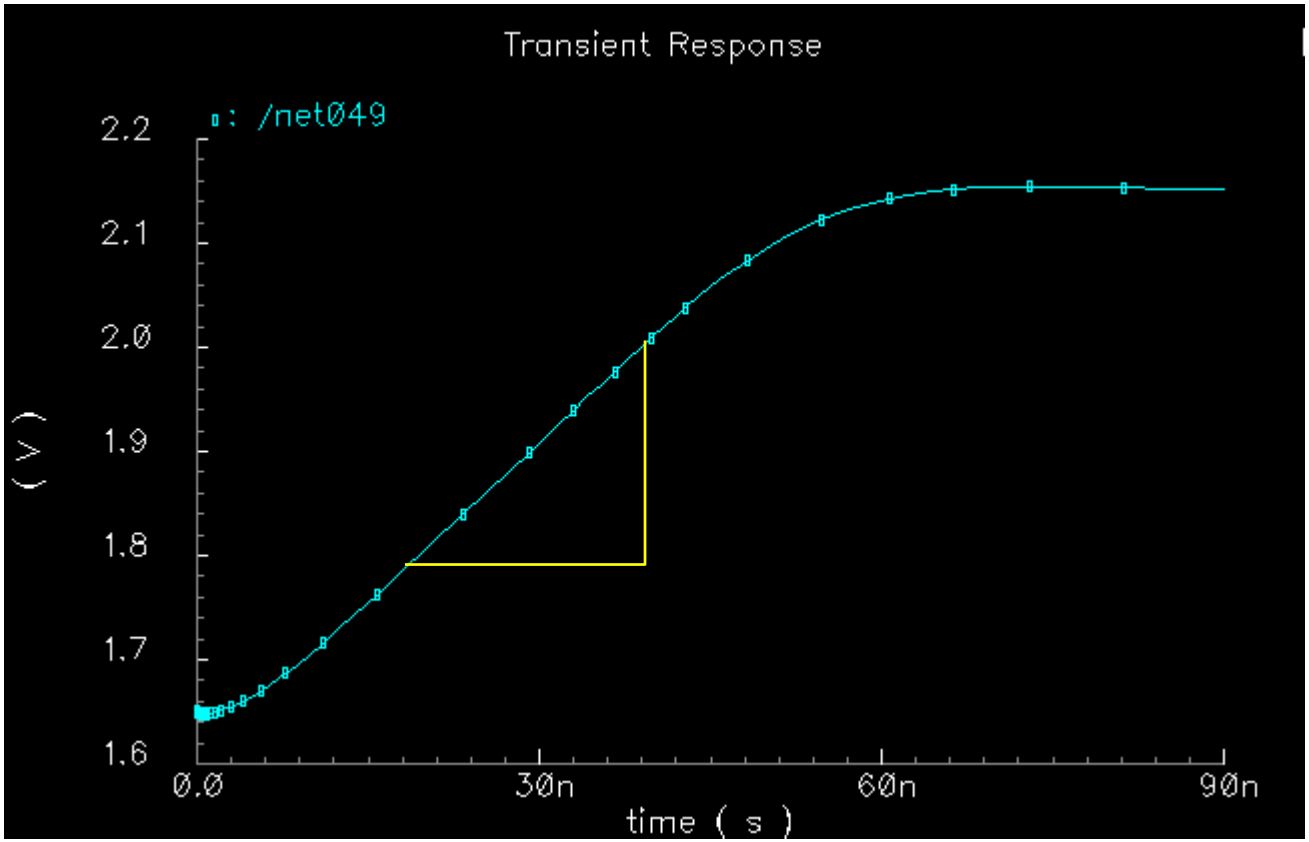
# Output Swing



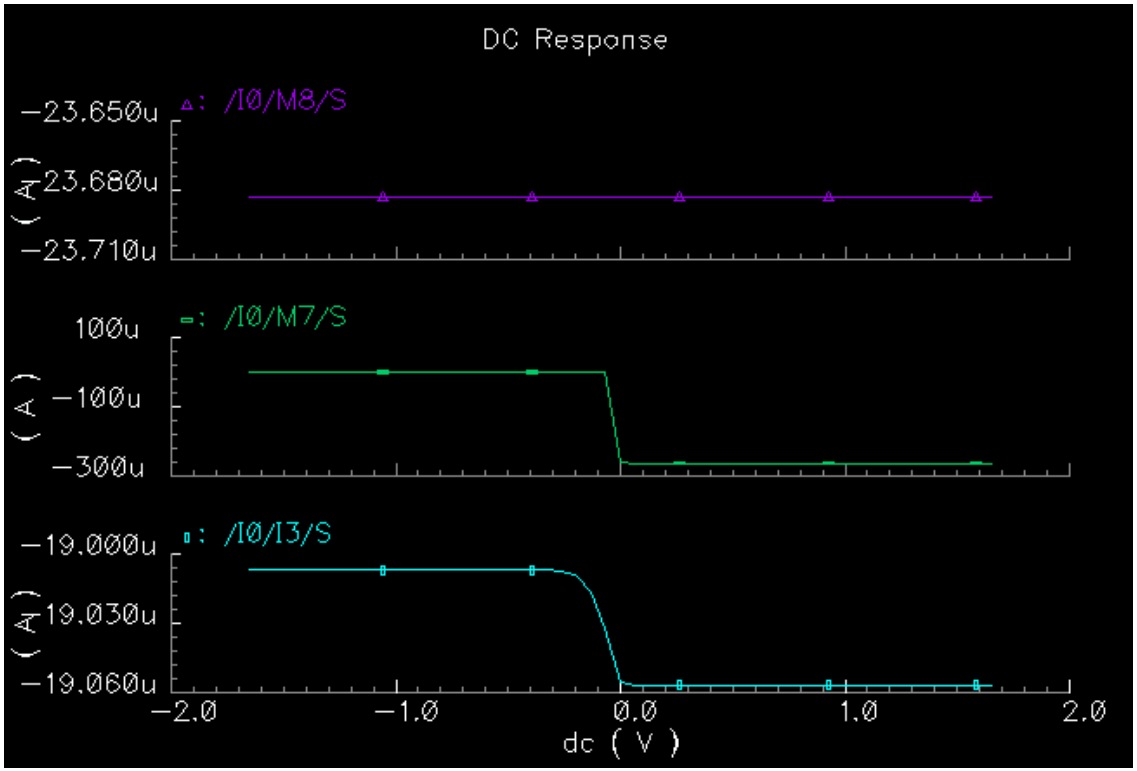
# Settling Time



# Slew Rate

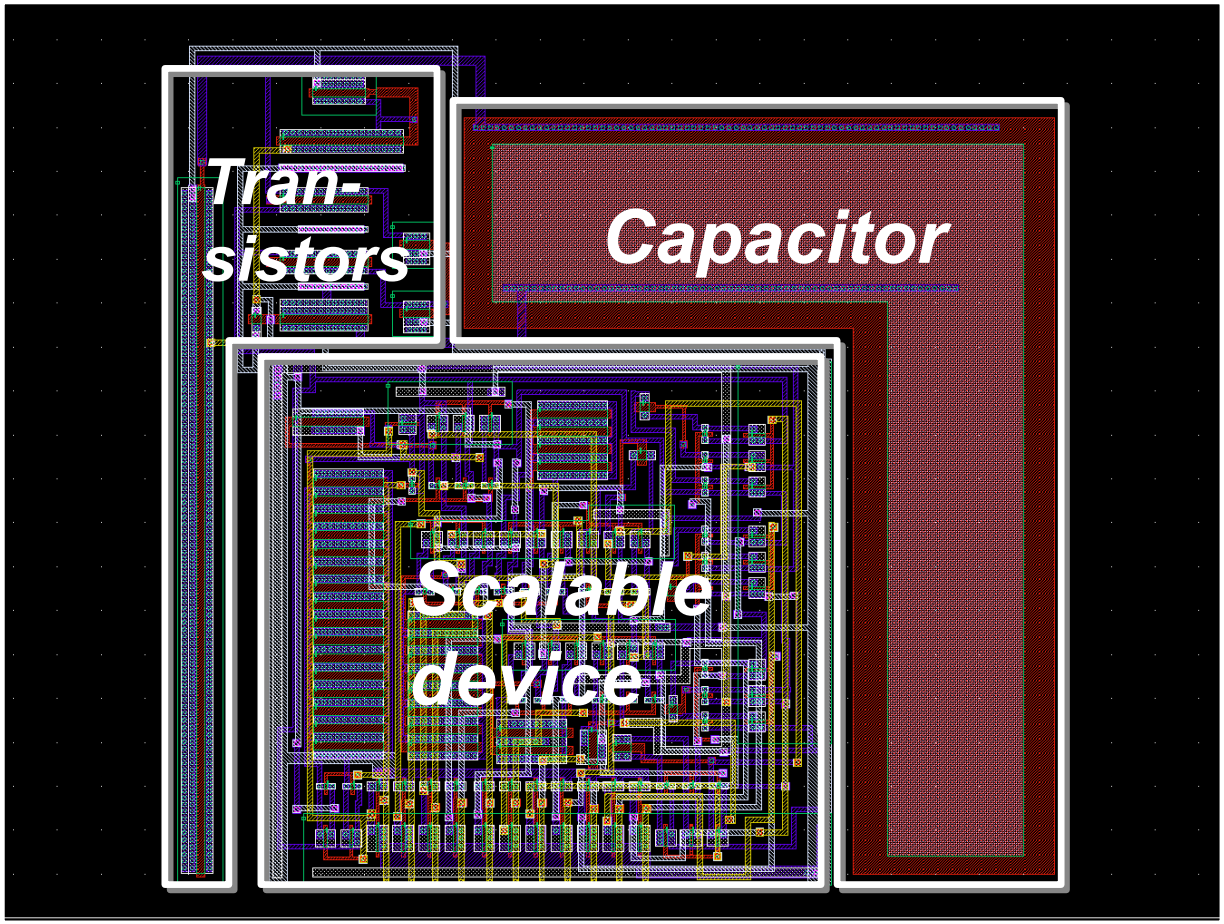

Transient Response
: /net049
2.2
2.1
2.0
1.9
1.8
1.7
1.6
( V )
0.0
30n
60n
90n
time ( s )

# Power dissipation

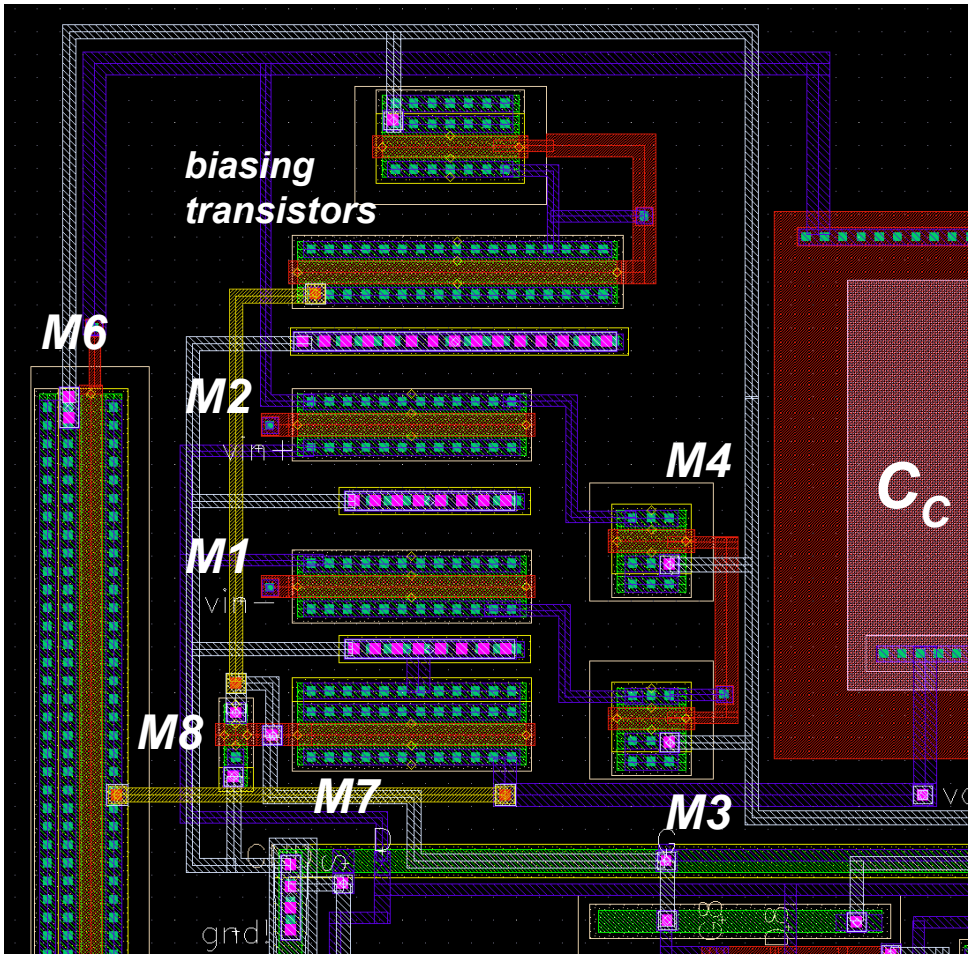



$$P_{diss} = 3.3V \cdot I_{diss}$$

# Layout



# Layout detail



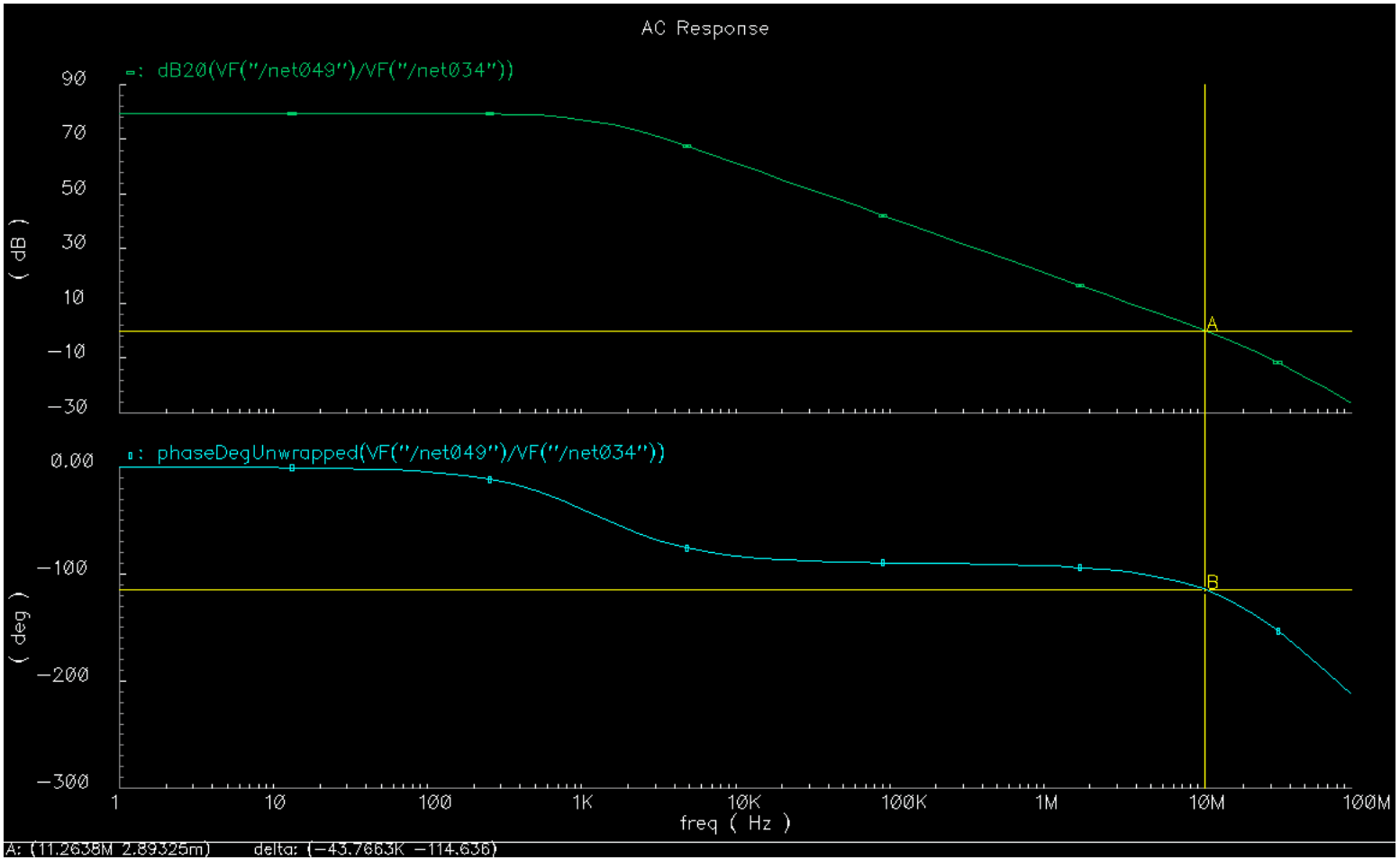
# LVS check

```
Running simulation in directory: "/export/users/sens4/LVS".

Loading all available p-cell functions
ROD pcell code loaded

Begin netlist:    Nov  7 12:06:14 2007
    view name list  = ("auLvs" "extracted" "schematic" "symbol")
    stop name list  = ("auLvs")
    library name    = "Course_rf"
    cell name       = "opamp"
    view name       = "extracted"
    globals lib     = "basic"
Running Artist Flat Netlisting ...
End netlist:    Nov  7 12:06:14 2007

Moving original netlist to extNetlist
Removing parasitic components from netlist
    presistors removed:  0
    pcapacitors removed: 0
    pinductors removed:  0
    pdiodes removed:     9
    trans lines removed: 0
    55 nodes merged into 55 nodes

Begin netlist:    Nov  7 12:06:15 2007
    view name list  = ("auLvs" "schematic" "cmos_sch" "netlist" "symbol")
    stop name list  = ("auLvs")
    library name    = "Course_rf"
    cell name       = "opamp"
    view name       = "schematic"
    globals lib     = "basic"
Running Artist Flat Netlisting ...
End netlist:    Nov  7 12:06:15 2007

Moving original netlist to extNetlist
Removing parasitic components from netlist
    presistors removed:  0
    pcapacitors removed: 0
    pinductors removed:  0
    pdiodes removed:     9
    trans lines removed: 0
    55 nodes merged into 55 nodes
```

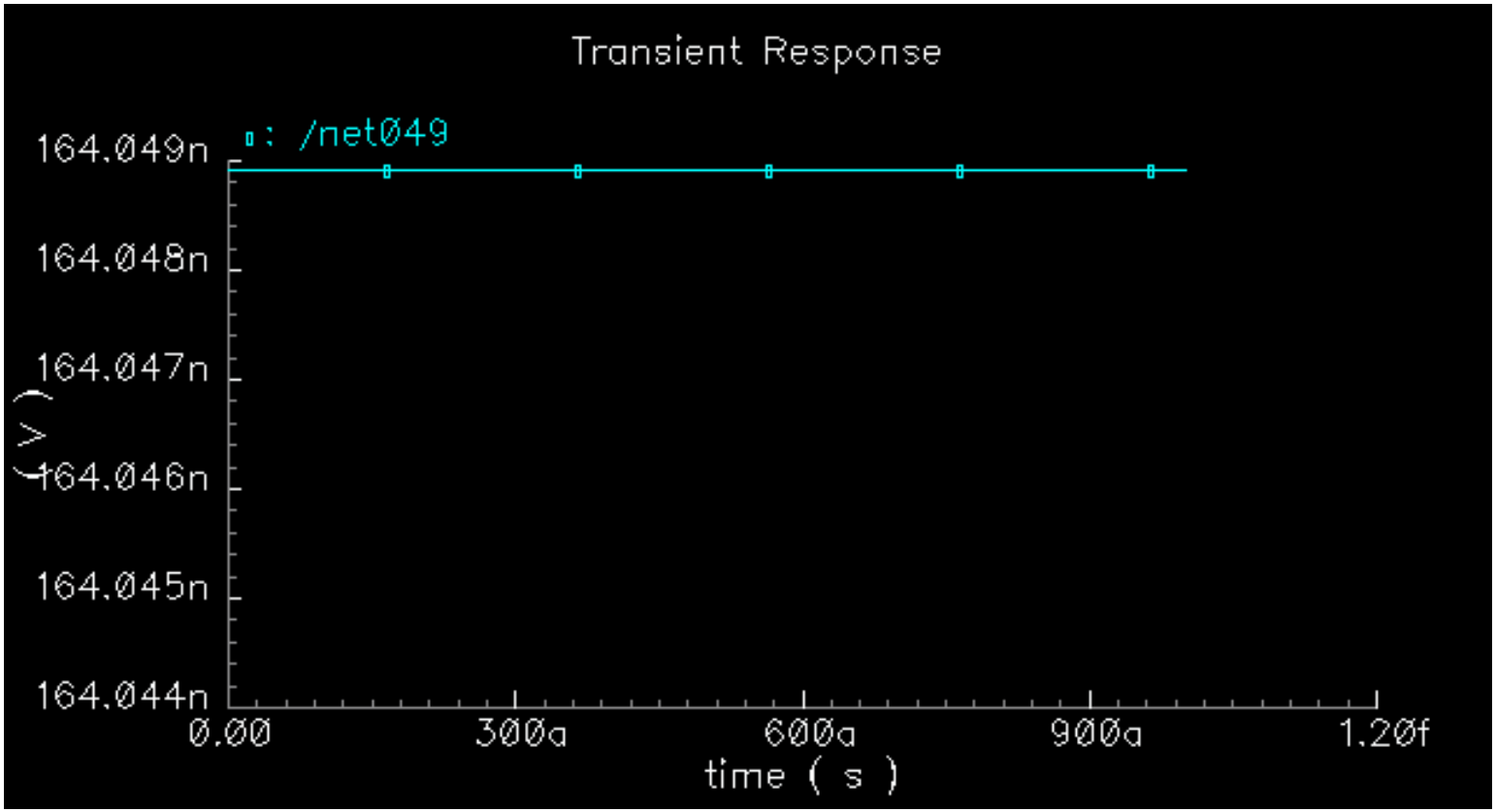
# LVS check

```
Running netlist comparison program:  LVS
Begin comparison:    Nov  7 12:06:15 2007
@(#)$CDS: LVS version 5.0.0 05/30/2003 19:44 (cds11939) $
Warning: Unknown device "zd2sm24" on a compareDeviceProperty command.
[...]
Warning: Unknown device "nd" on a permuteDevice command.

The net-lists match.

                          layout  schematic
                               instances
    un-matched                 0          0
    rewired                    0          0
    size errors                0          0
    pruned           0         0
    active           135       109
    total                      135        109

                                 nets
    un-matched                 0          0
    merged           0         0
    pruned           0         0
    active           55        55
    total                      55         55

                               terminals
    un-matched                 0          0
    matched but
    different type   0         0
    total                      16         16
End comparison:      Nov  7 12:06:15 2007

Comparison program completed successfully.
```

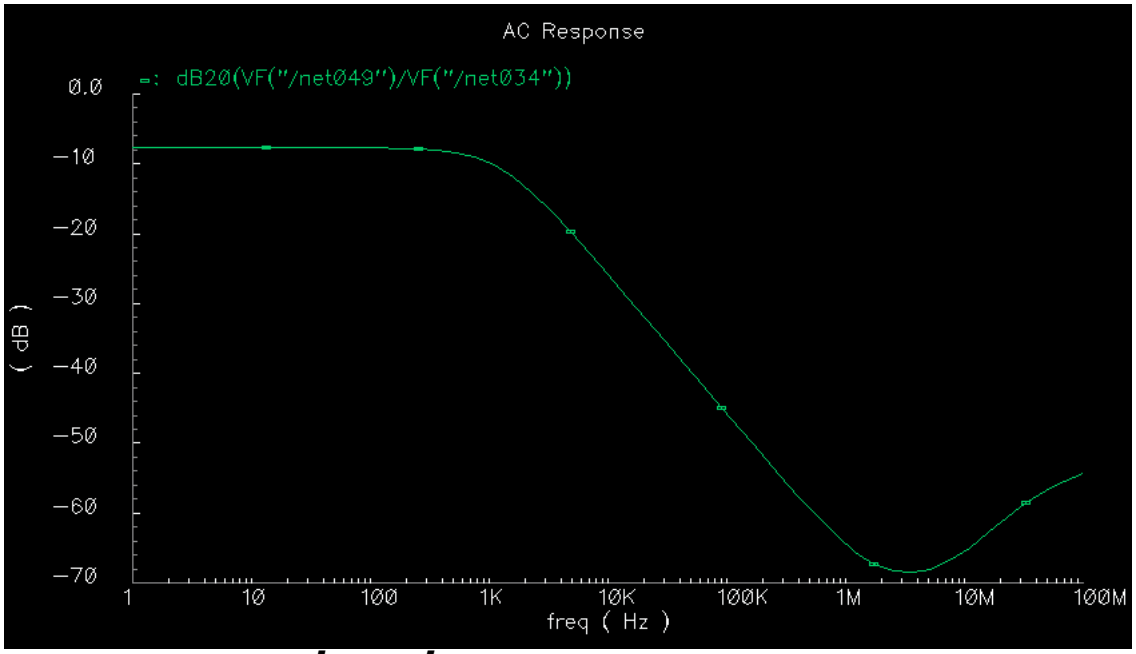
# Bode plot


AC Response
dB20(VF("/net049")/VF("/net034"))
90
70
50
30
10
−10
−30
( dB )
A
phaseDegUnwrapped(VF("/net049")/VF("/net034"))
0.00
−100
−200
−300
( deg )
B
1
10
100
1K
10K
100K
1M
10M
100M
freq ( Hz )
A: (11.2638M 2.89325m)
delta: (−43.7663K −114.636)

# Offset


Transient Response
: /net049
164.049n
164.048n
164.047n
164.046n
164.045n
164.044n
0.00
300a
600a
900a
1.20f
time ( s )

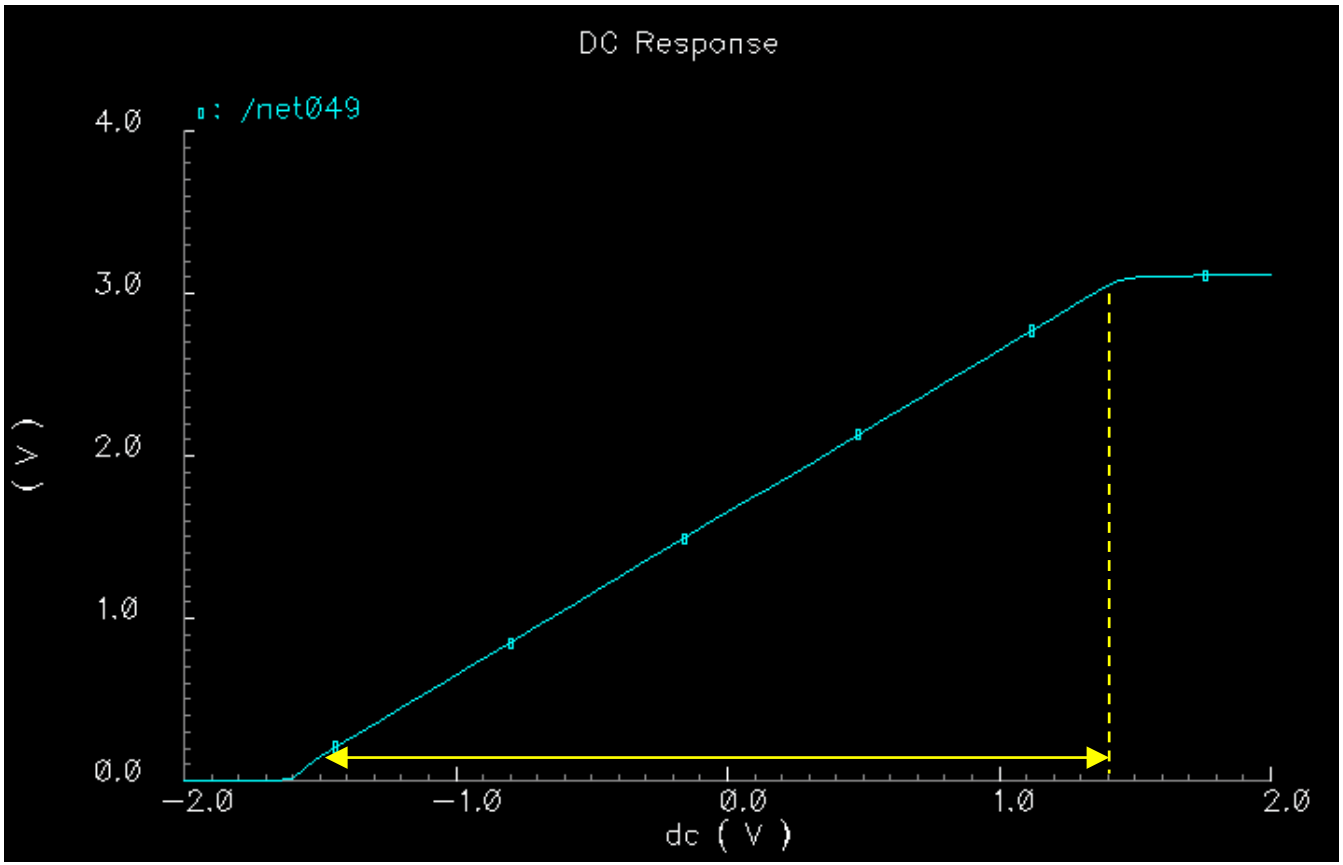
# CMRR



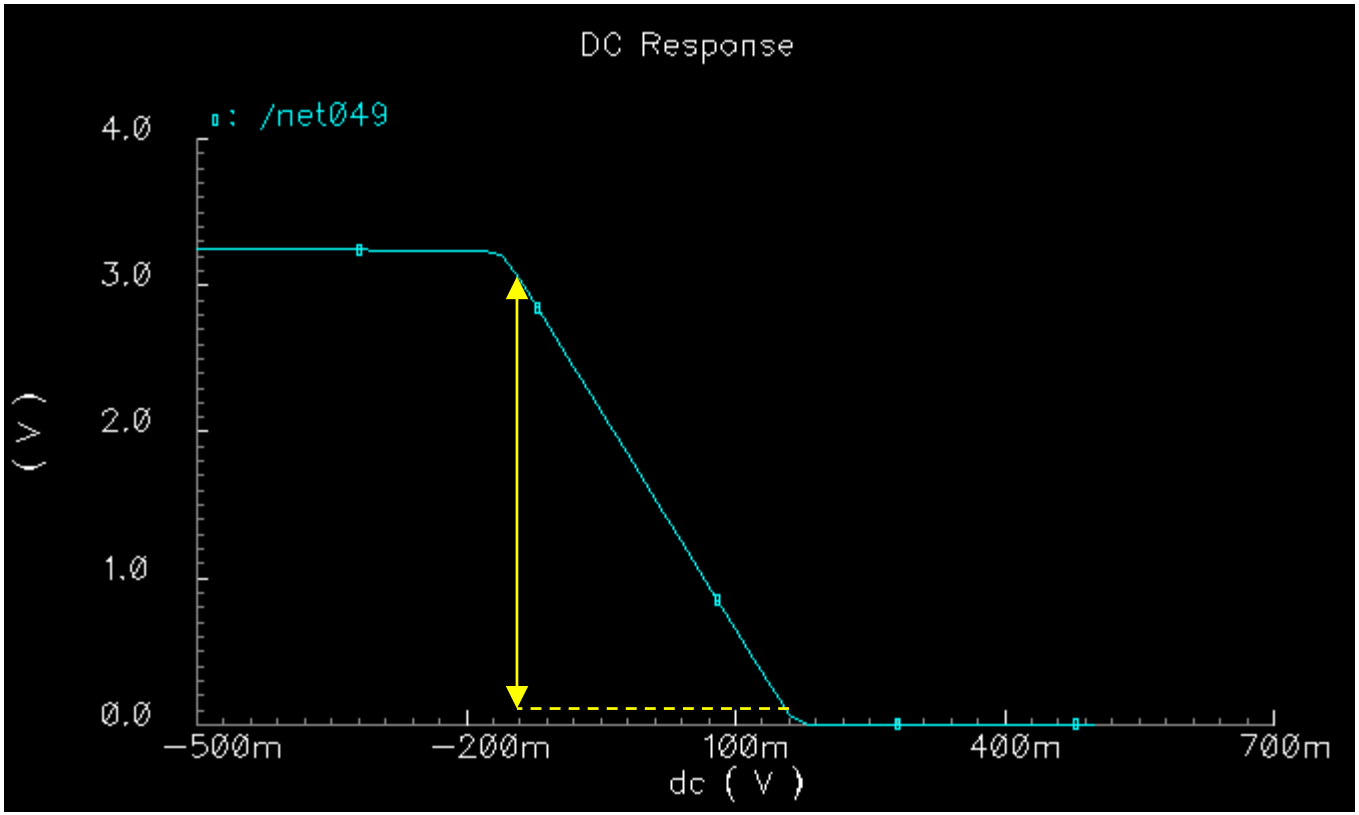

***common mode gain***

**CMRR = (differential-mode gain) – (common-mode gain)**

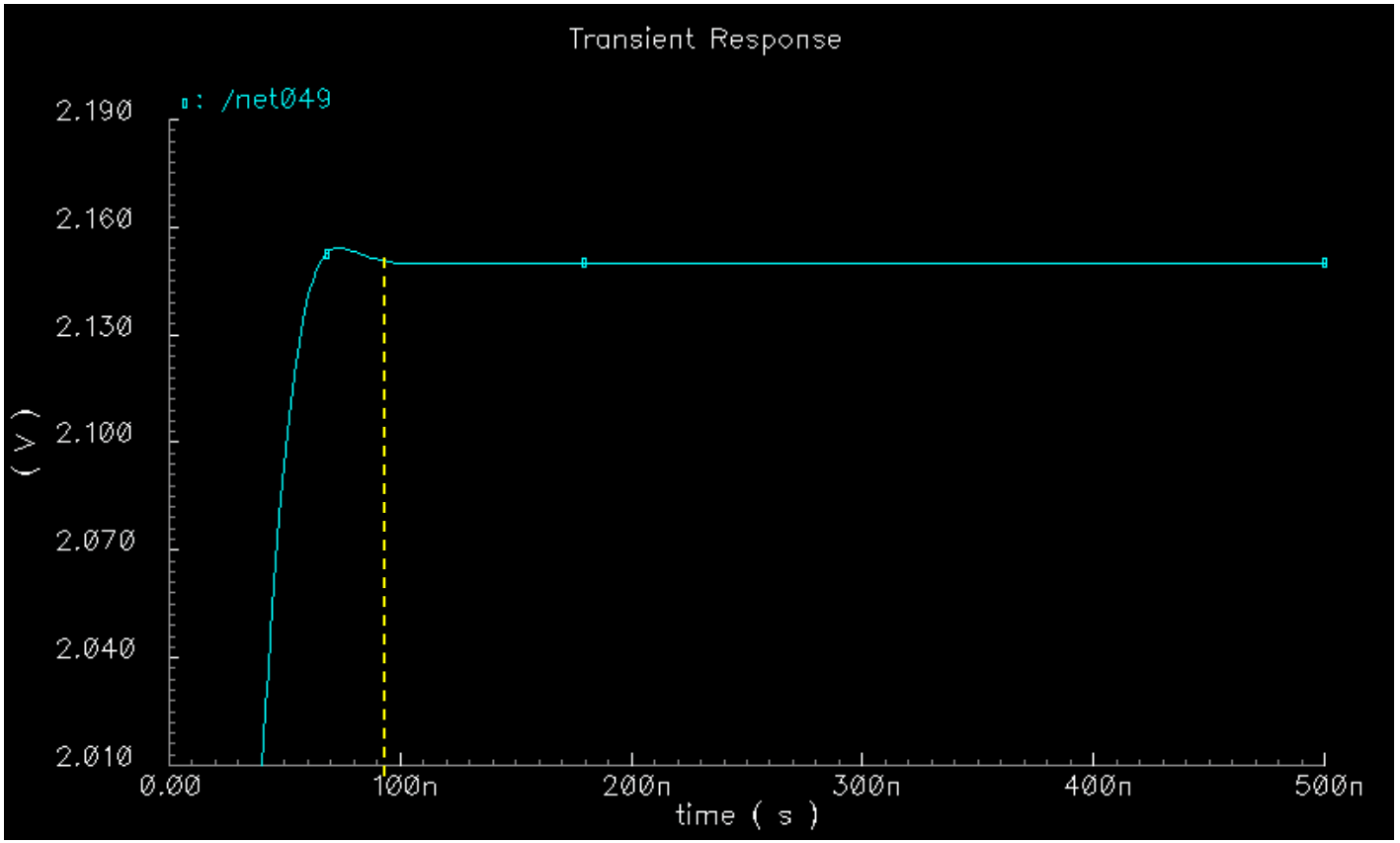
# Input CMR



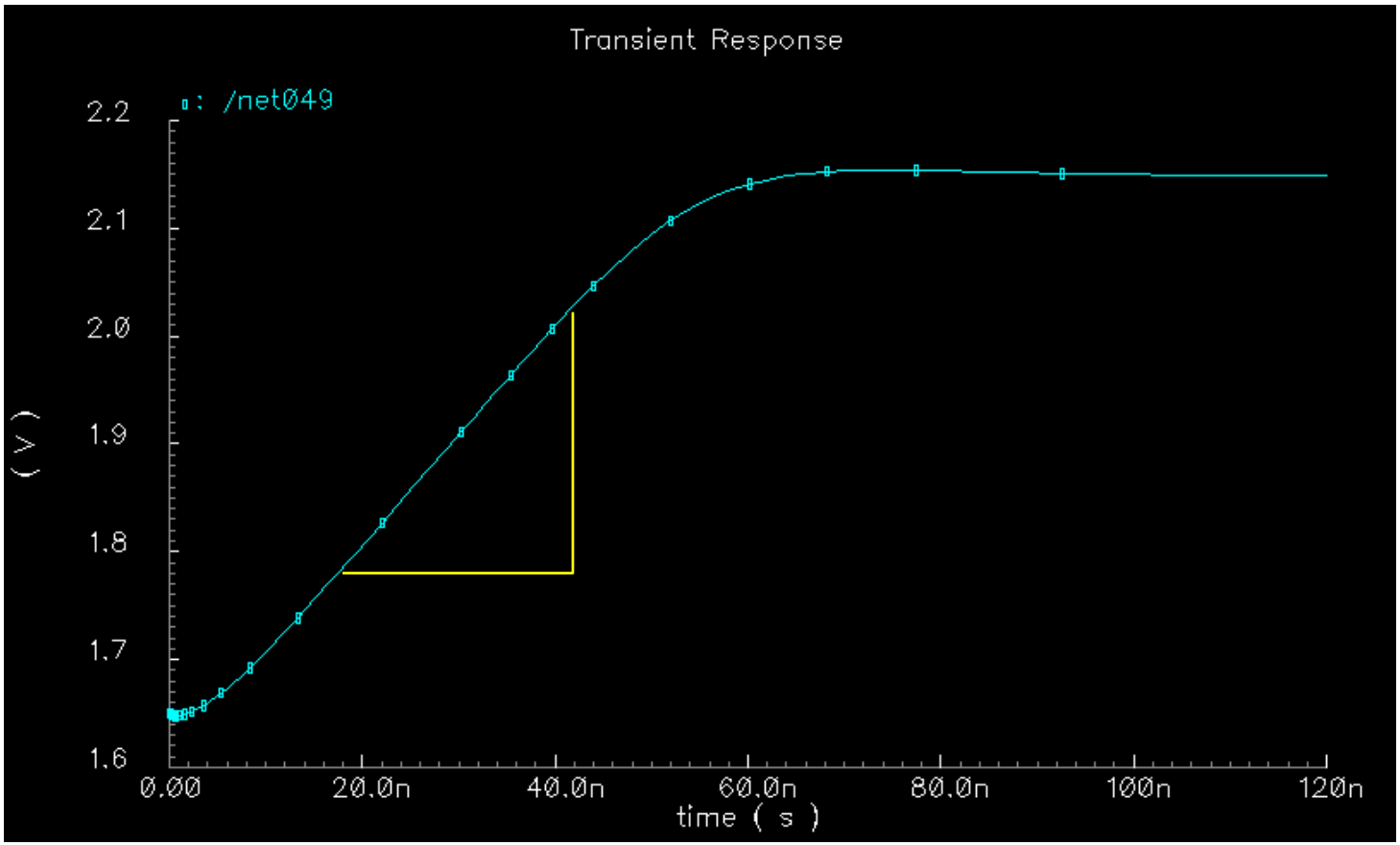
# Output Swing



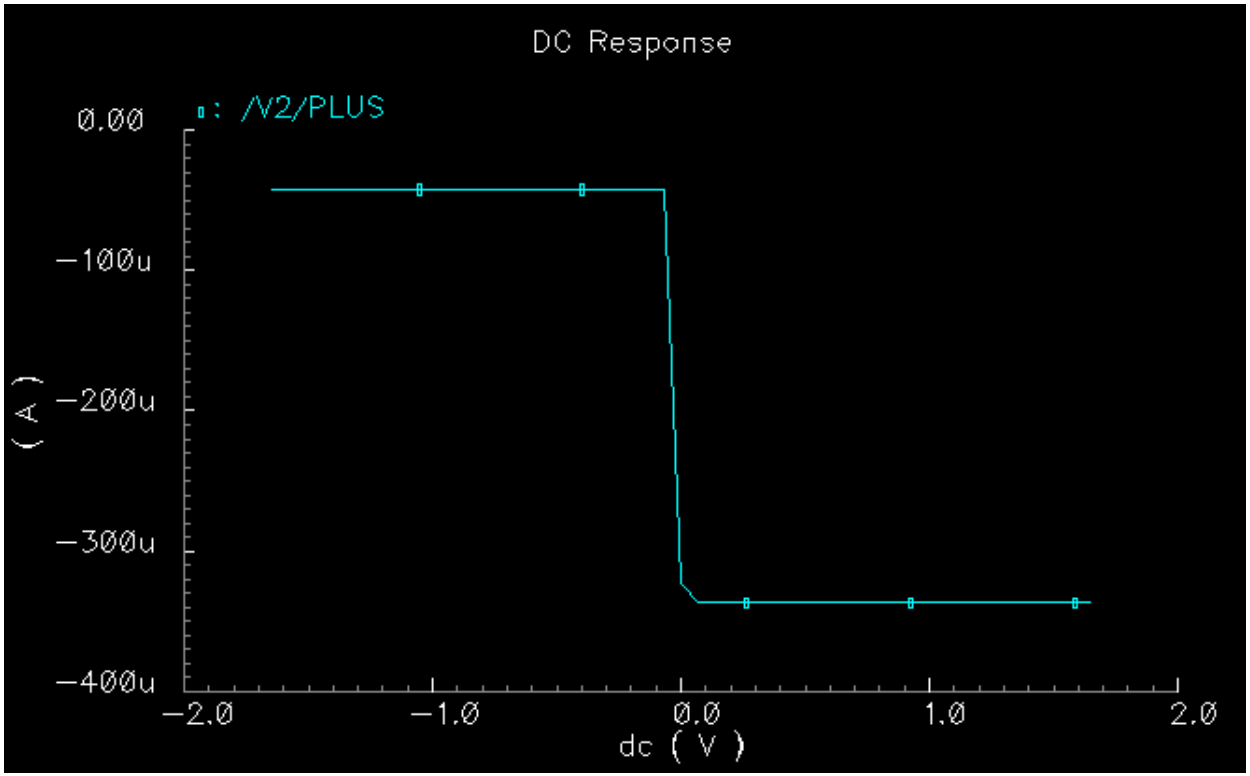
# Settling Time



# Slew Rate

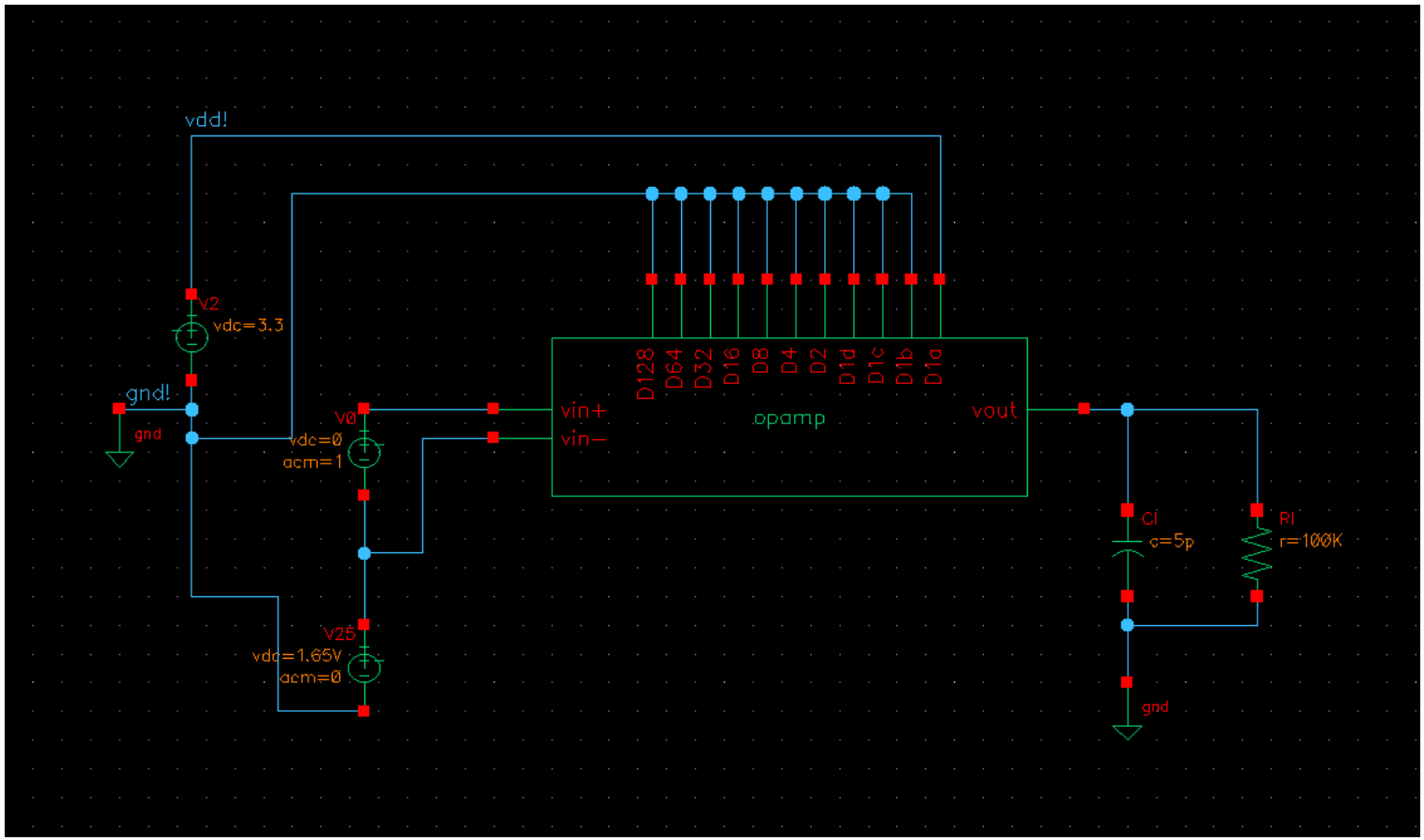

Transient Response
: /net049
2.2
2.1
2.0
1.9
1.8
1.7
1.6
( V )
0.00
20.0n
40.0n
60.0n
80.0n
100n
120n
time ( s )

# Power dissipation

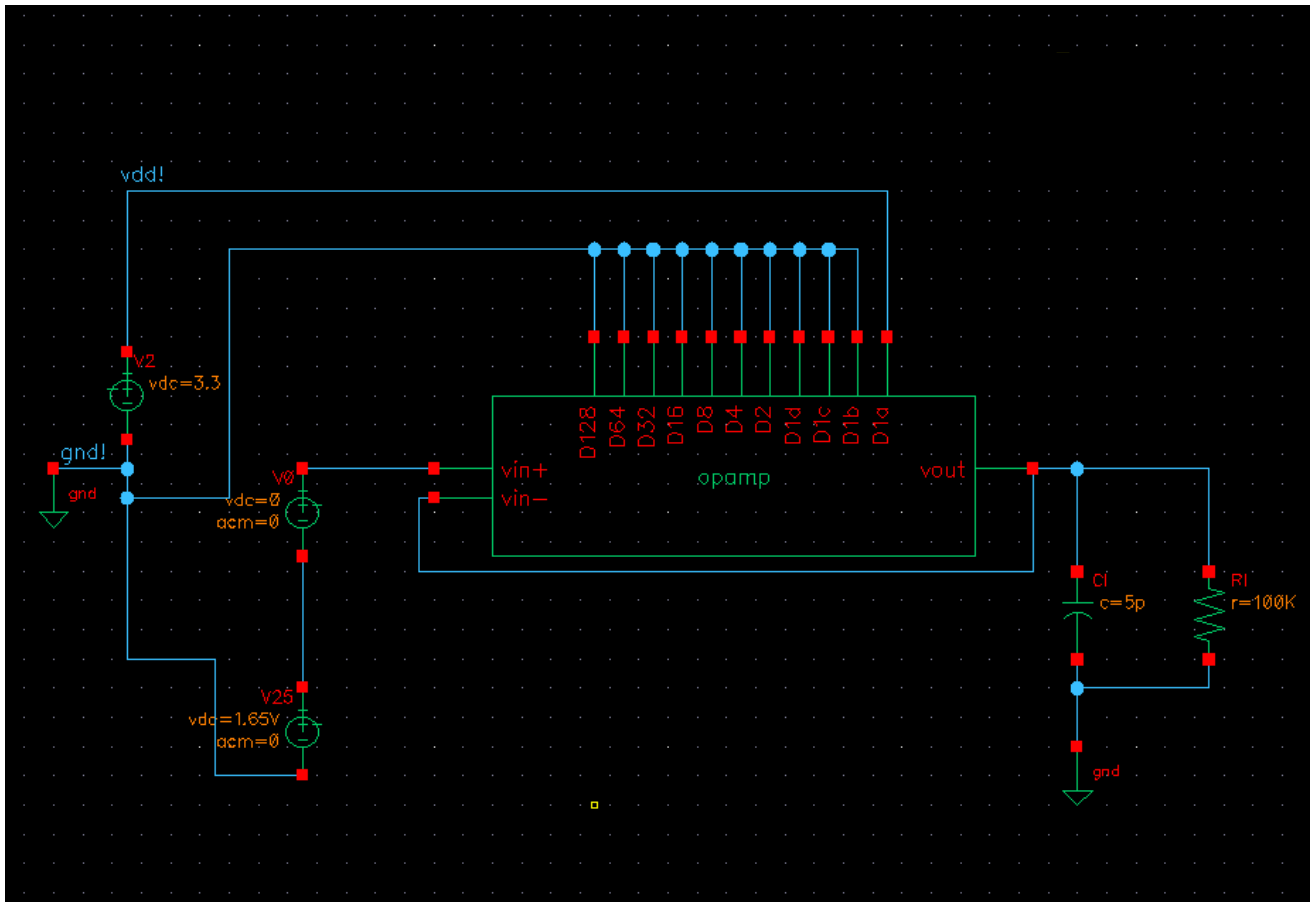



$$P_{diss} = 3.3V \cdot I_{diss}$$

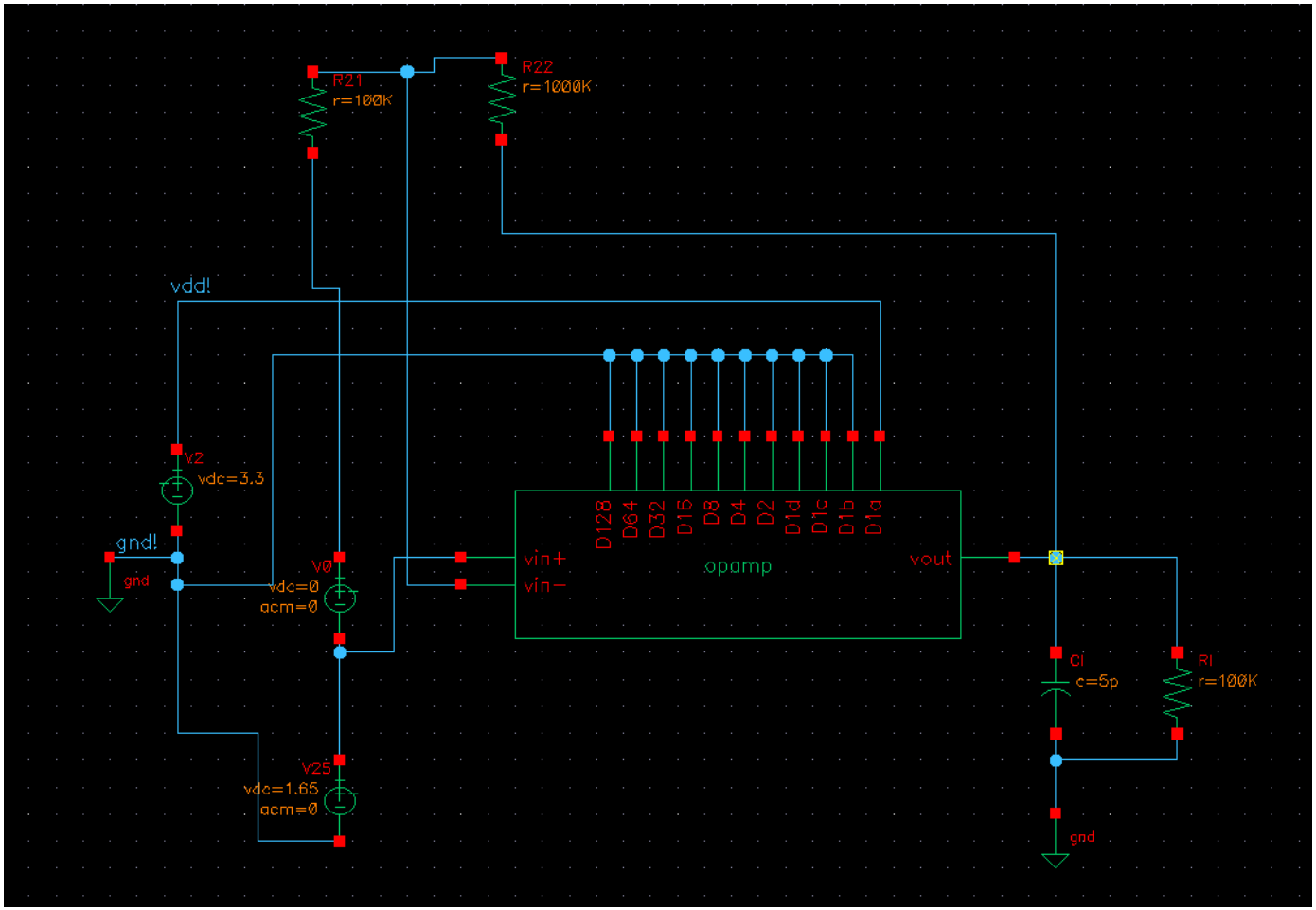
# Testing circuit for bode plot



# Testing circuit for offset, CMRR



# Testing circuit for output swing



# Results

| | required | w/o scalable device | with scalable device | analog extracted |
|---|---|---|---|---|
| **Open loop gain** | > 75 dB | 79.4 dB | 79.5 dB | 79.4 dB |
| **Gain bandwidth** | 10 MHz | 20.5 MHz | 11.3 MHz | 11.25 MHz |
| **Phase margin** | > 65° | 65.6° | 65.2° | 65.4° |
| **Settling time** | < 1 μs | < 0.1 μs | < 0.1 μs | < 0.1 μs |
| **Slew rate** | 1 V/μs | 19.5 V/μs | 10.3 V/μs | 10.4 V/μs |
| **Offset** | 1 μV | 4.5 μV | 0.16 μV | 0.16 μV |
| **Input CMR** | +/- 0.5 V | -1.5 V / +1.2 V | -1.5 V / +1.4 V | -1.5 V / +1.4 V |
| **Output Swing** | +/- 0.35 V | -1.4 V / +1.6 V | -1.6 V / +1.5 V | -1.5 V / +1.5 V |
| **CMRR** | > 80 dB | 87.6 dB | 87 dB | 87 dB |
| **Power dissipation** | < 1mW | 3 mW | 1.01 mW | 1.1 mW |