

Komparatorentwurf und Verifizierung



Komparator-Design

- Theoretisches Design nach Allan-Holberg
 - Schematic
 - Verifizierung
 - Scalable Devices einbinden
 - Verifizierung
 - Layout
 - Verifizierung
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Vorgabe:

Open Loop Gain	75	Output swing -	-0,35
Gain Bandwidth	1,00E+07	Output swing +	0,35
Phase margin	-	Cmrr	80
Settling Time	1,00E-06	Power dissipation	0,0010
Slew Rate	10	Voltage Supply -	-1,65
Offset	1,00E-06	Voltage Supply +	1,65
CMR -	-0,5	Load Capacitance	5,00E-12
CMR +	1	Load Resistance	100000

Designplan nach Allen-Holberg

$$I_7 = I_6 = C_{II} \frac{dv_{out}}{dt} = C_{II} \frac{(V_{OH} - V_{OL})}{t_p} = 3,5 \cdot 10^{-6} A$$

$$\frac{W_6}{L_6} = \frac{2 \cdot I_6}{K'_p (V_{SD6}(sat))^2} = 0,07$$

$$\frac{W_7}{L_7} = \frac{2 \cdot I_7}{K'_n (V_{DS7}(sat))^2} = 0,02$$

$$I_5 = C_I \frac{dv_{out}}{dt} = C_I \frac{(V_{OH} - V_{OL})}{t_p} = 1,65 \cdot 10^{-6} A \quad \text{mit } C_I \approx 0,5 \text{ pF}$$

Designplan nach Allen-Holberg II

$$\frac{W_3}{L_3} = \frac{W_4}{L_4} = \frac{I_5}{K'_p (V_{SG3} - |V_{TP}|)^2} = 0,04$$

$$g_{m1} = \frac{A_v(0)(g_{ds2} + g_{ds4})(g_{ds6} + g_{ds7})}{g_{m6}} = \frac{A_v(0) \left(\frac{I_5}{2}(\lambda_n + \lambda_p)\right) \left(\frac{I_6}{2}(\lambda_n + \lambda_p)\right)}{\sqrt{2K'_p \cdot I_6 \cdot \frac{W_6}{L_6}}} = 3,79 \cdot 10^{-6} S$$

$$\frac{W_1}{L_1} = \frac{W_2}{L_2} = \frac{g_{m1}^2}{K'_n \cdot I_5} = 0,05 \quad V_{gs1} = V_{tn} + \sqrt{\frac{2 \cdot I_5}{2k'_n \cdot \frac{W_1}{L_1}}} = 0,94 V$$

$$V_{DS5}(sat) = V_{icm} - V_{GS1} - V_{SS} = 0,21 V \Rightarrow \frac{W_5}{L_5} = \frac{2 \cdot I_5}{K'_N (V_{ds5}(sat))^2} = 0,42$$

Realisiert in einer ExcelTabelle

Open Loop Gain	75	95	I6	3,50E-006	2,76E-004
Gain Bandwidth	1,00E+07	1,00E+07	I7	3,50E-006	2,76E-004
Phase margin	-	-			
Settling Time	1,00E-06	3,98E-08	M6 W/L	0,07	31,5
Slew Rate	10000000	10000000	M7 W/L	0,02	10,75
Offset	1,00E-06	1,00E-06			
Input CMR -	-0,5	-0,5	I5	1,65E-006	4,14E-005
Input CMR +	1	1			
Output swing -	-0,35	-1,1	M ³ W/L	0,04	0,98
Output swing +	0,35	1,1	M4 W/L	0,04	0,98
Cmrr	80	80			
Power dissipation	0	0	Gm1	3,79E-006	4,03E-004
Voltage Supply -	-1,65	-1,65			
Voltage Supply +	1,65	1,65	M1 W/L	0,05	23,05
Load Capacitance	5,00E-12	5,00E-12	M ² W/L	0,05	23,05
Load Resistance	100000	100000			
K' n	1,70E-04	1,70E-04	Cgs6	3,24E-016	1,43E-013
K' p	5,80E-05	5,80E-05	Cgd2	2,33E-016	1,05E-013
Lambda n	0,01	0,01	Cgd4	1,78E-016	4,46E-015
Lambda p	0,03	0,03			
Vt n	0,5	0,5	C1_2	7,34E-016	2,52E-013
Vt p	-0,65	-0,65	C1_1 > C1_2	WAHR	WAHR
C1_1	5,00E-013	5,00E-013			
Cox	4,54E-015	4,54E-015	Vgs1	0,94	0,6
			Vds5	0,21	0,55
I6	3,50E-006	2,76E-004	M5 W/L	0,42	1,63
I7	3,50E-006	2,76E-004			10,86
			Power dissipation	0,00002	0,00105

Werte nach Allan-Holberg

M 1	0,05
M 2	0,05
M 3	0,04
M 4	0,04
M 5	0,42
M 6	0,07
M 7	0,02

⇒ Werte erhöhen

M 1	23
M 2	23
M 3	1
M 4	1
M 5	2
M 6	32
M 7	11

Werte nach Messungen

M 1	25
M 2	25
M 3	5
M 4	5
M 5	3
M 6	57
M 7	18

Werte ermittelt durch
mehrmaliges messen und
anpassen der Werte nach
folgenden
Gesichtspunkten:

Änderungskriterien:

Wichtige Eigenschaften:

1. Gain

$$A_V(0) = \frac{\sqrt{2K'_p \cdot I_6 \frac{W_6}{L_6}} \cdot \sqrt{2K'_n \cdot I_2 \frac{W_2}{L_2}}}{\left(\frac{I_5}{2}(\lambda_n + \lambda_p)\right) \left(\frac{I_6}{2}(\lambda_n + \lambda_p)\right)}$$

2. Slewrate

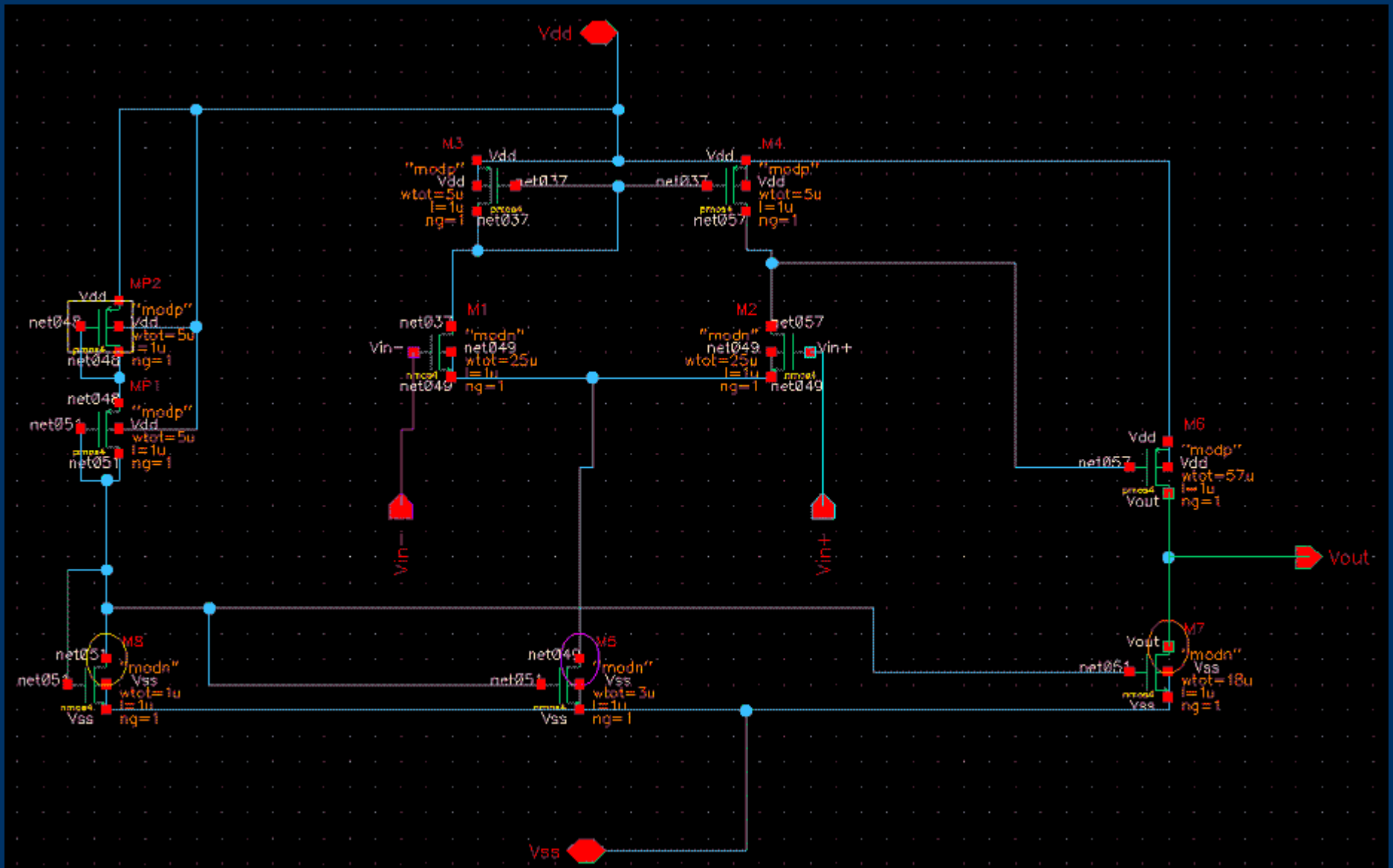
proportional zu :

$$I_6 = \frac{1}{2} \cdot \frac{W_6}{L_6} \cdot K'_p (V_{SD6}(sat))^2$$

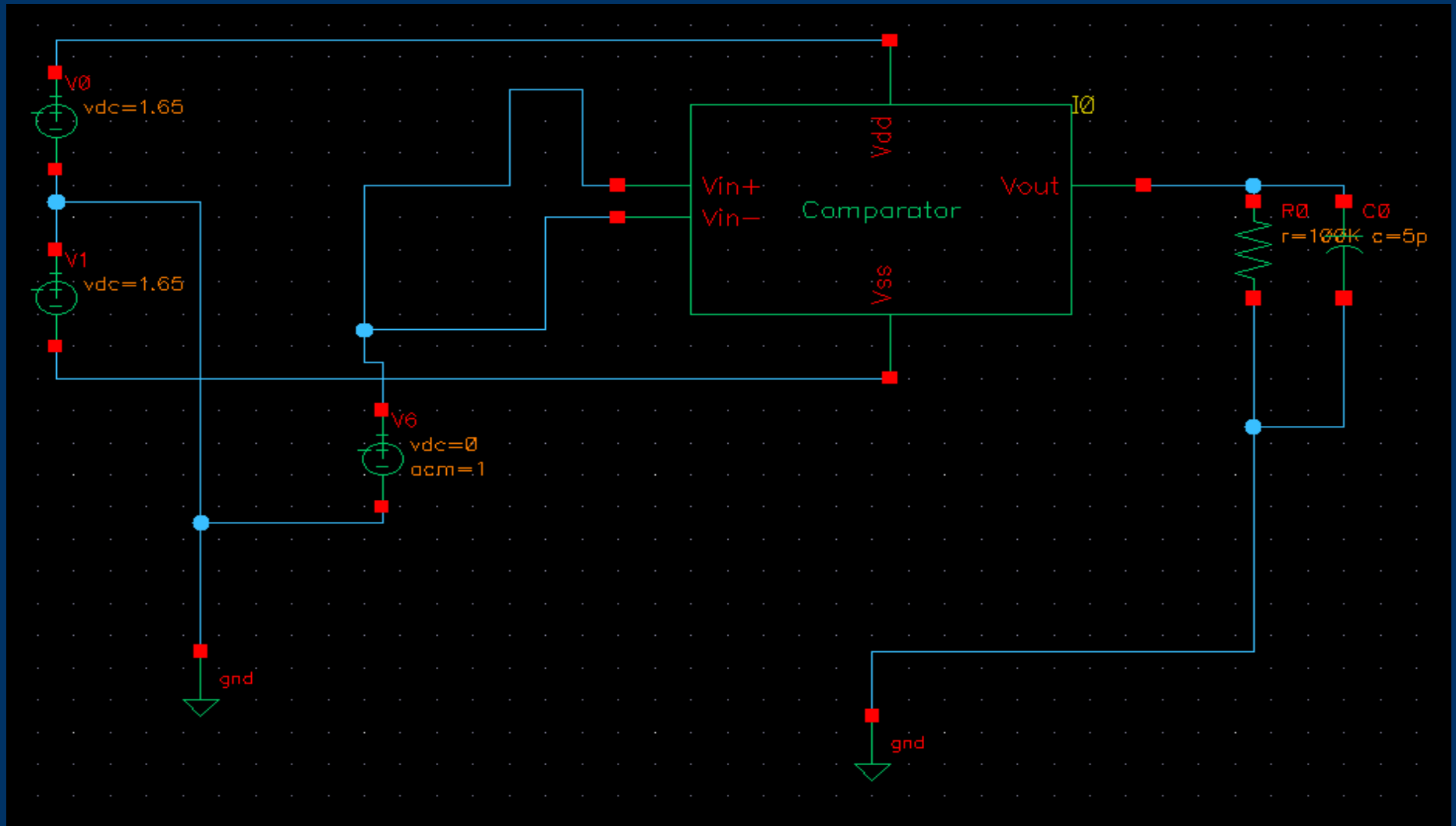
3. Powerconsumption

$$I_6 + I_5 = I_6 + \frac{1}{2} \cdot \frac{W_5}{L_5} \cdot K'_n (V_{SD5}(sat))^2$$

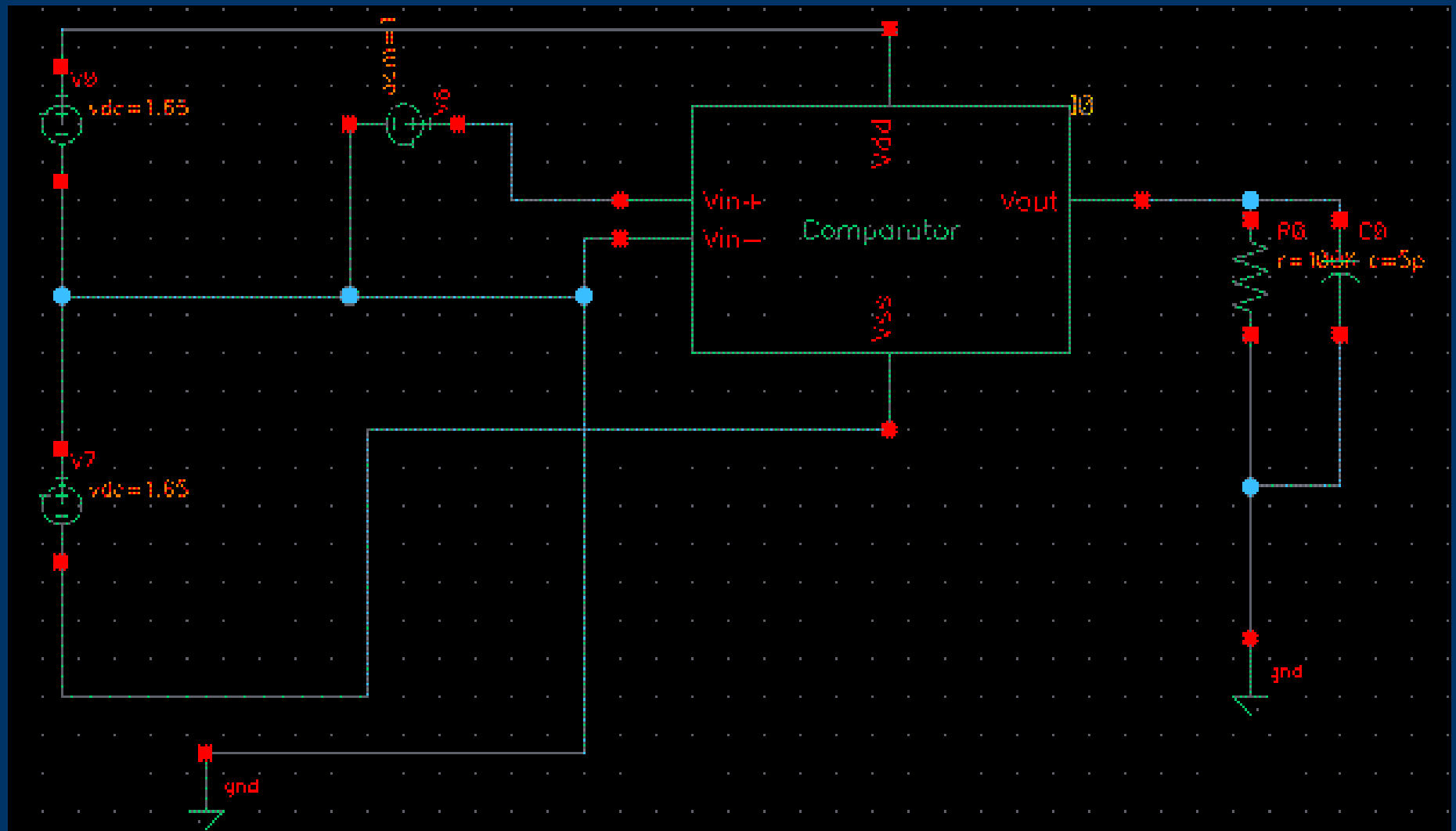
Schematic



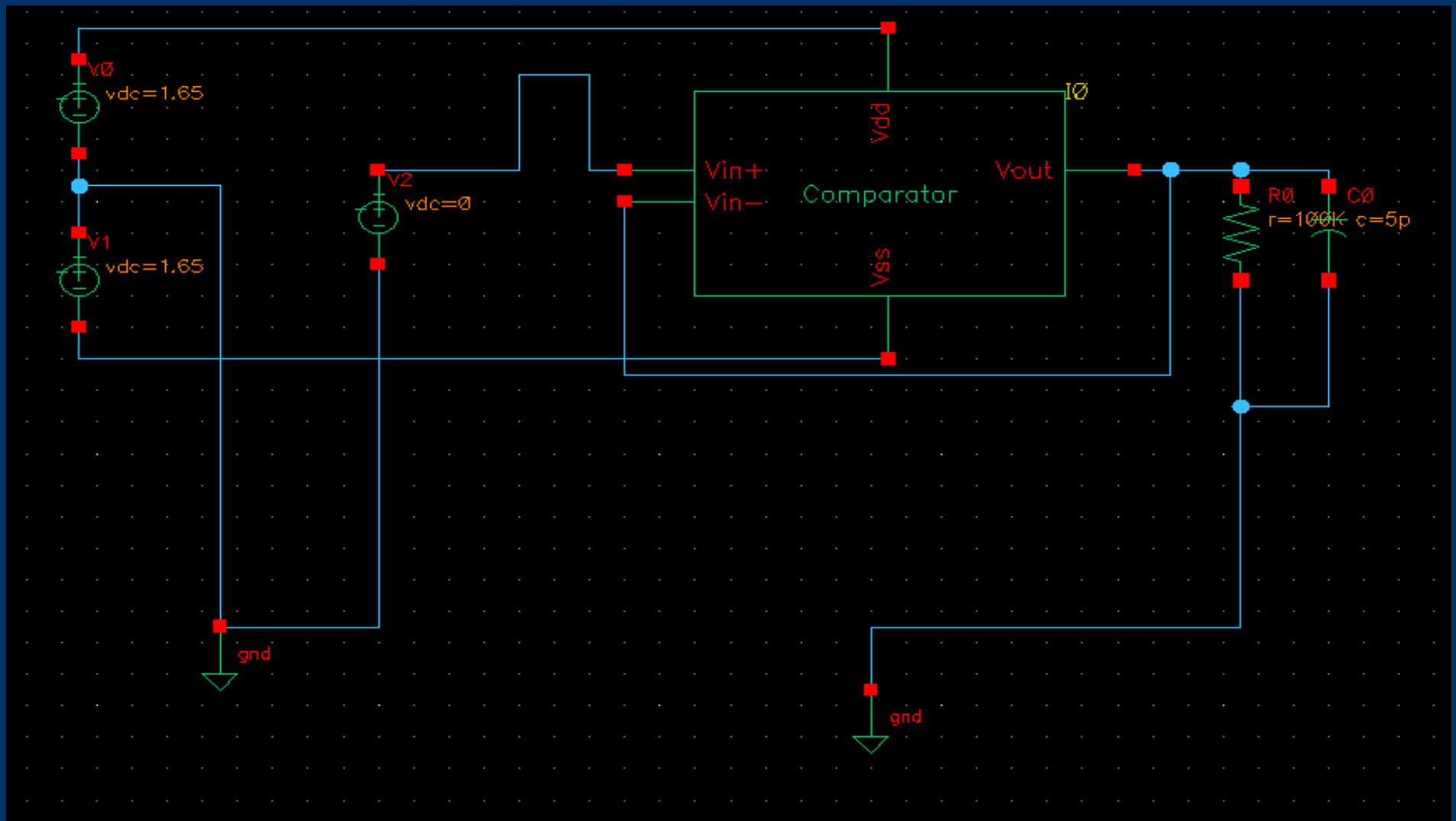
Testschaltung CMRR



Testschaltung Bodeplot

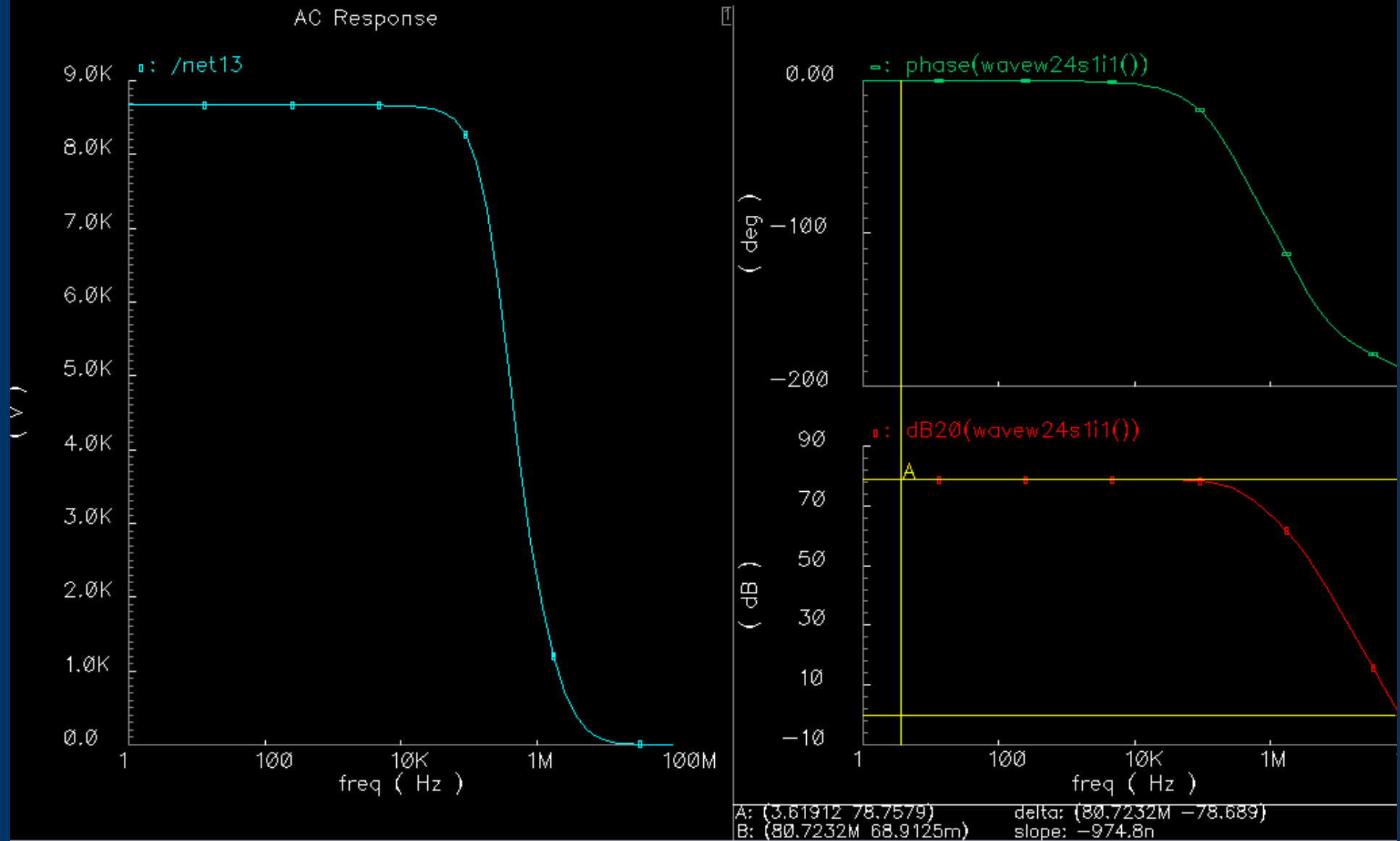


Testschaltung CMR

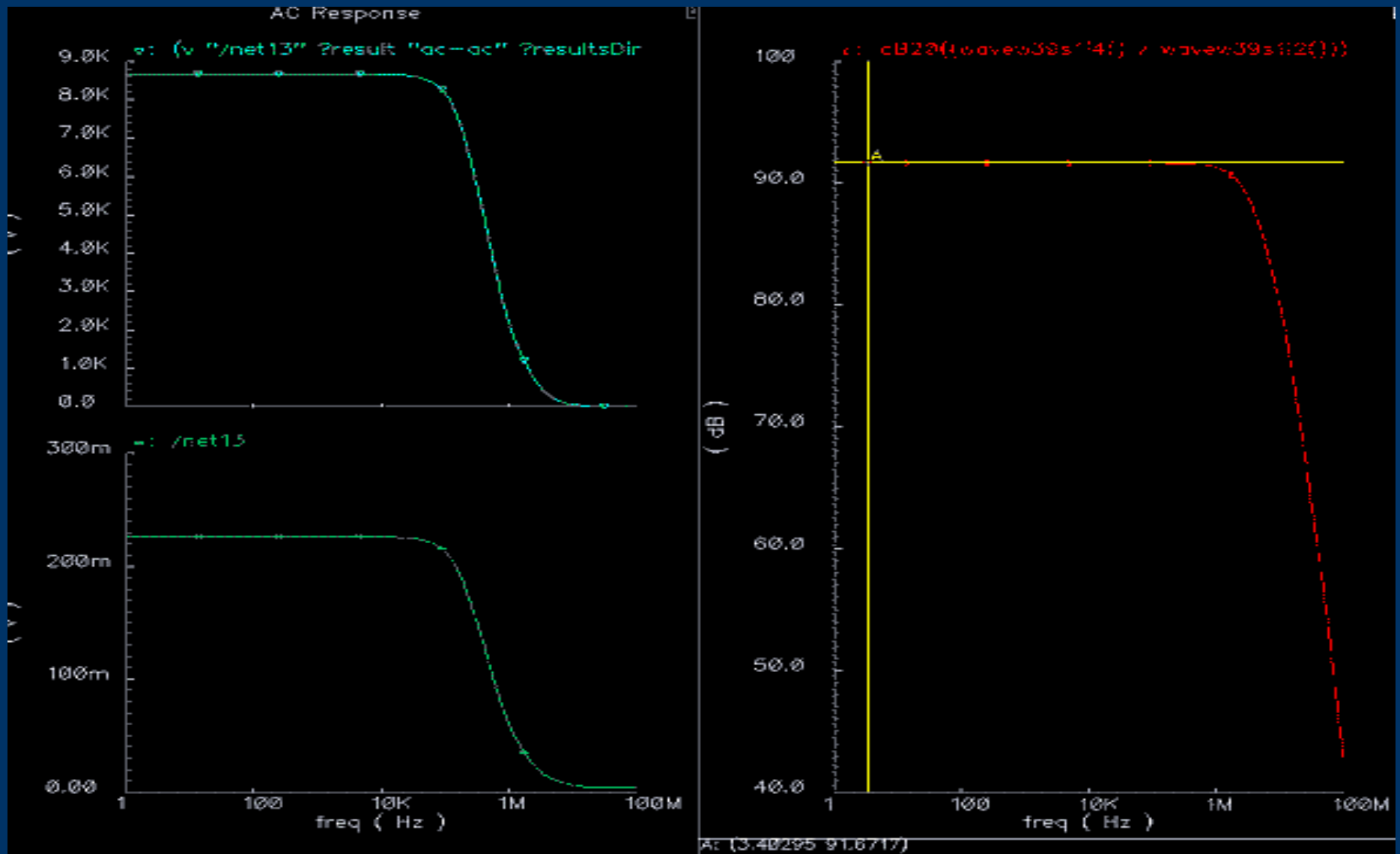


Verifizierung – Gain und GBW

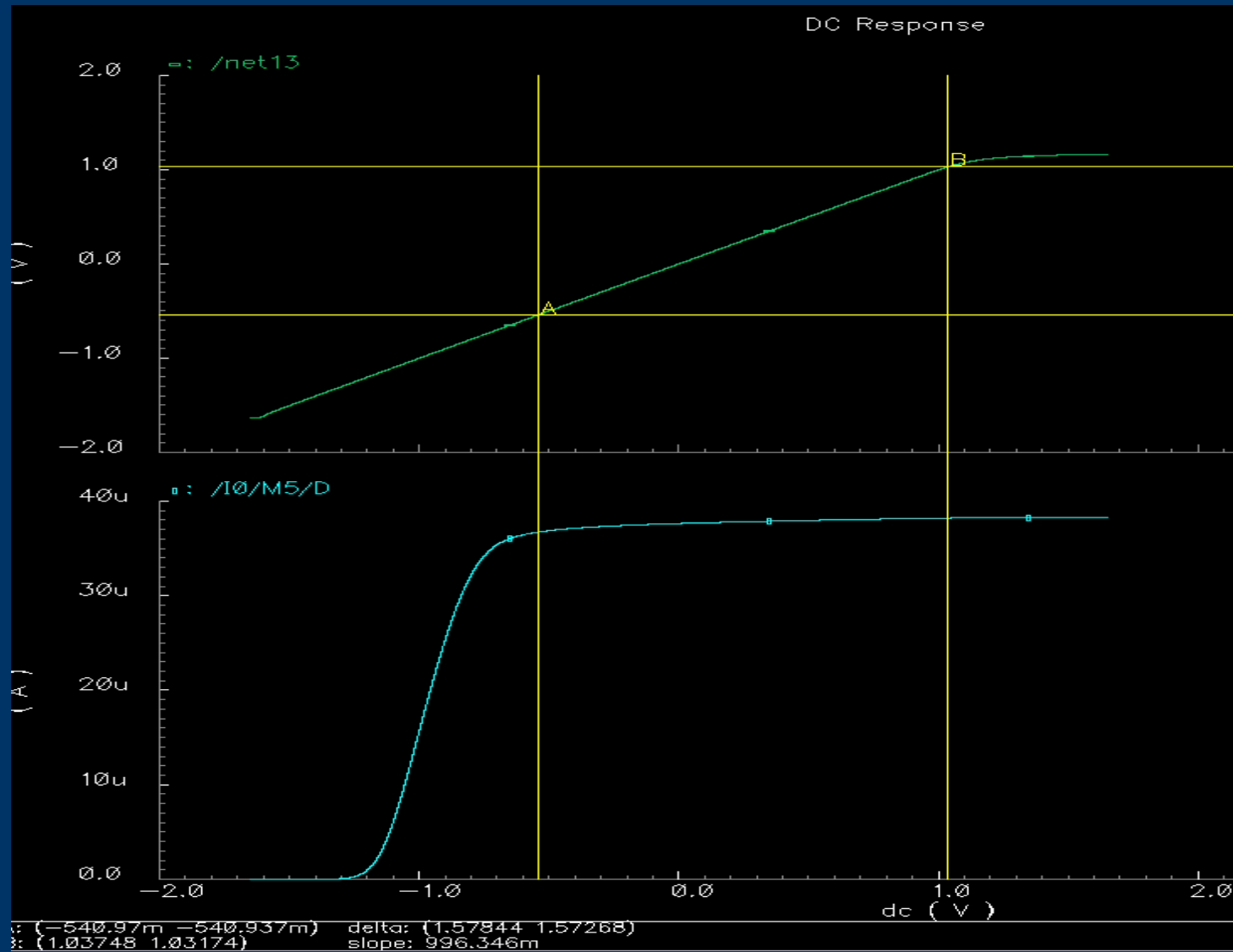
course_HM Comparator_test-openloopgain schematic : Nov 23 11:49:45 2007



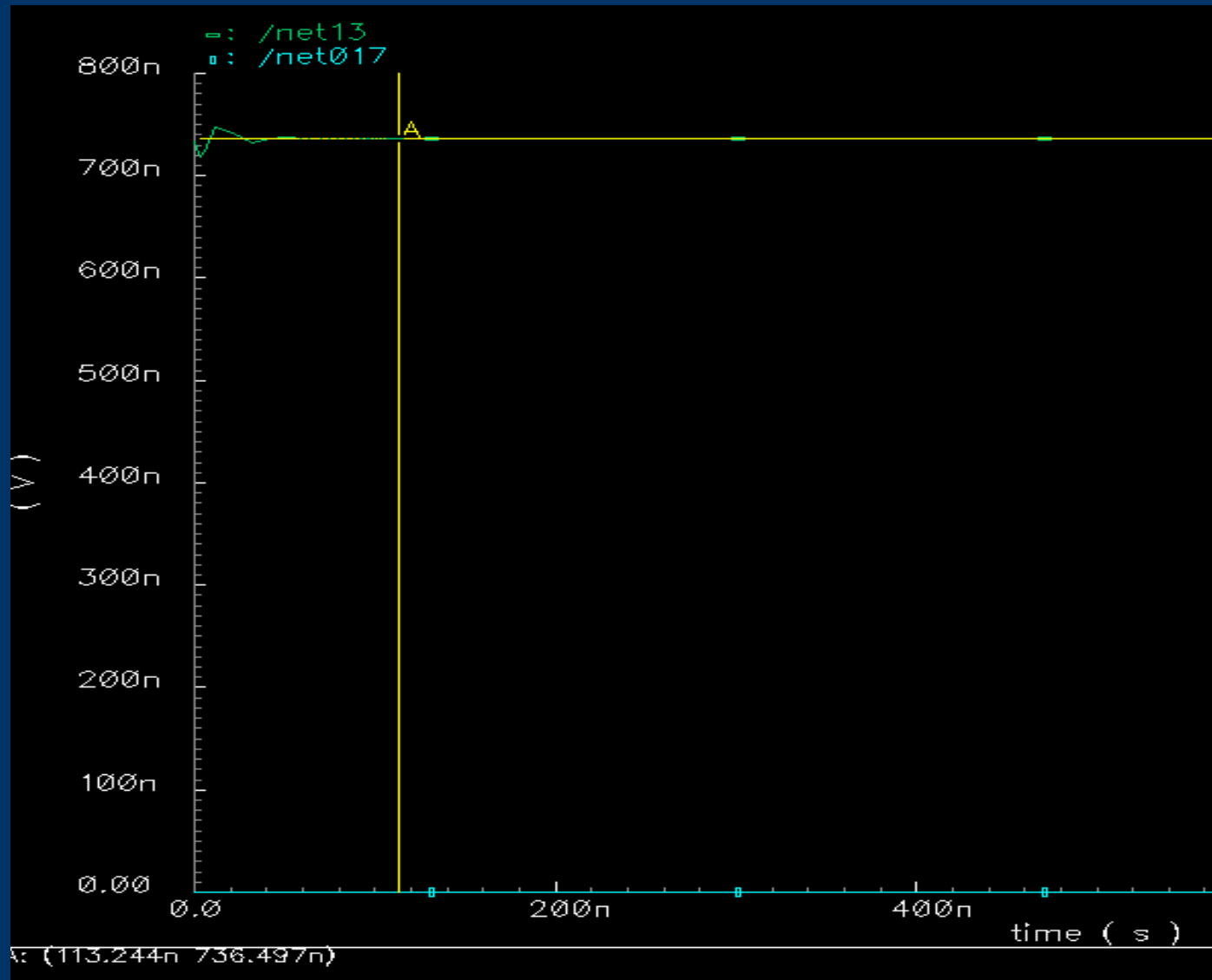
Verifizierung - CMRR



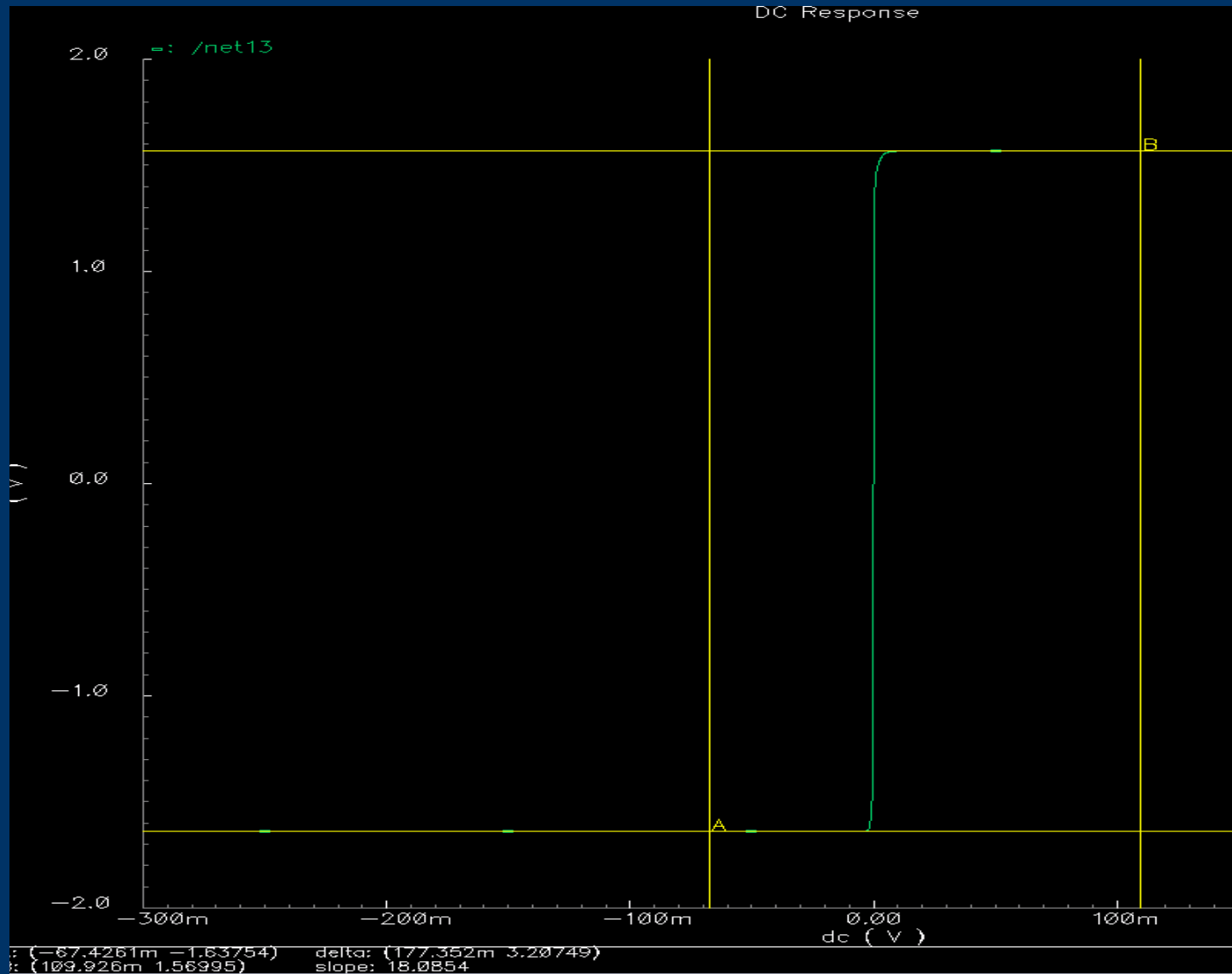
Verifizierung - CMR



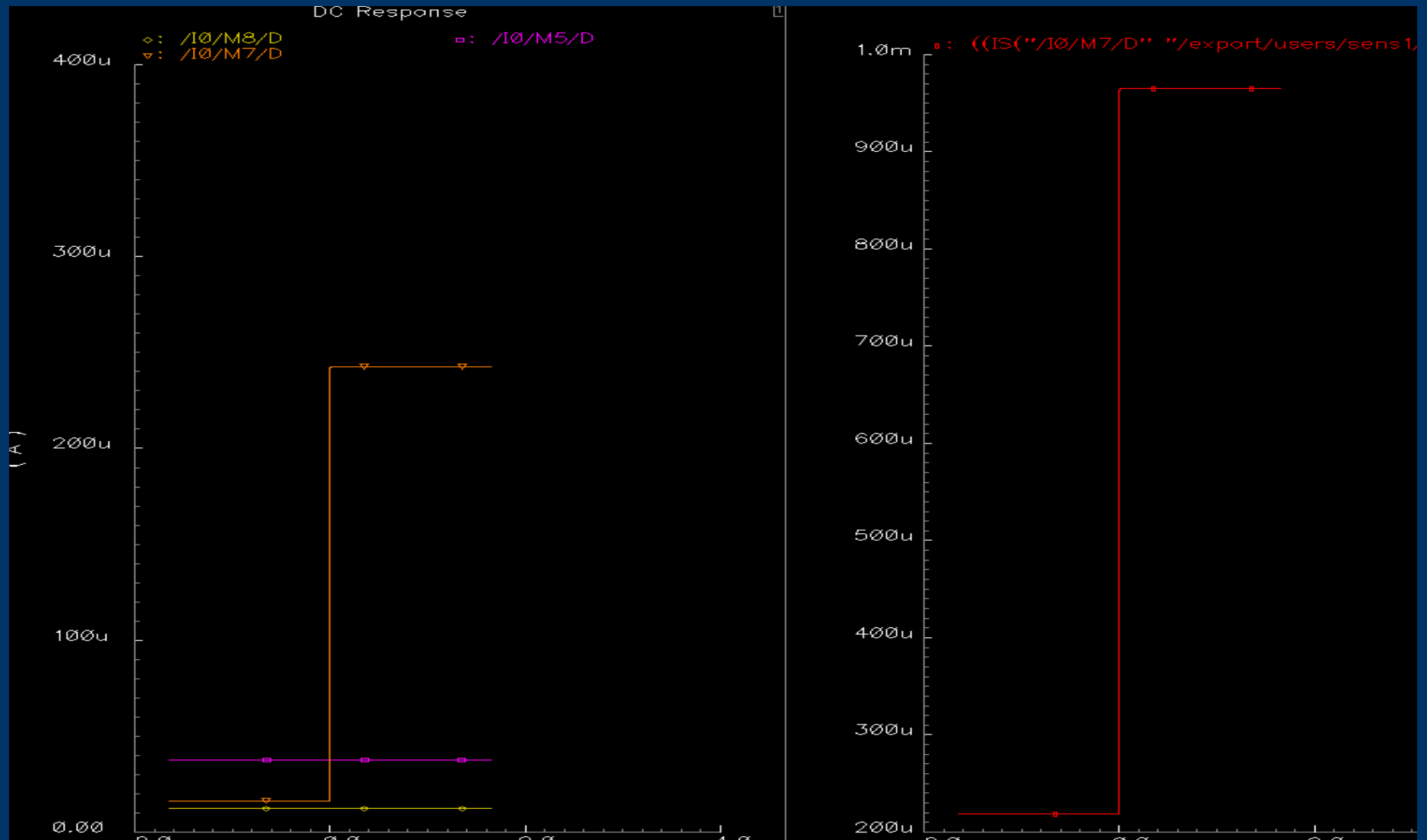
Verifizierung - Offset



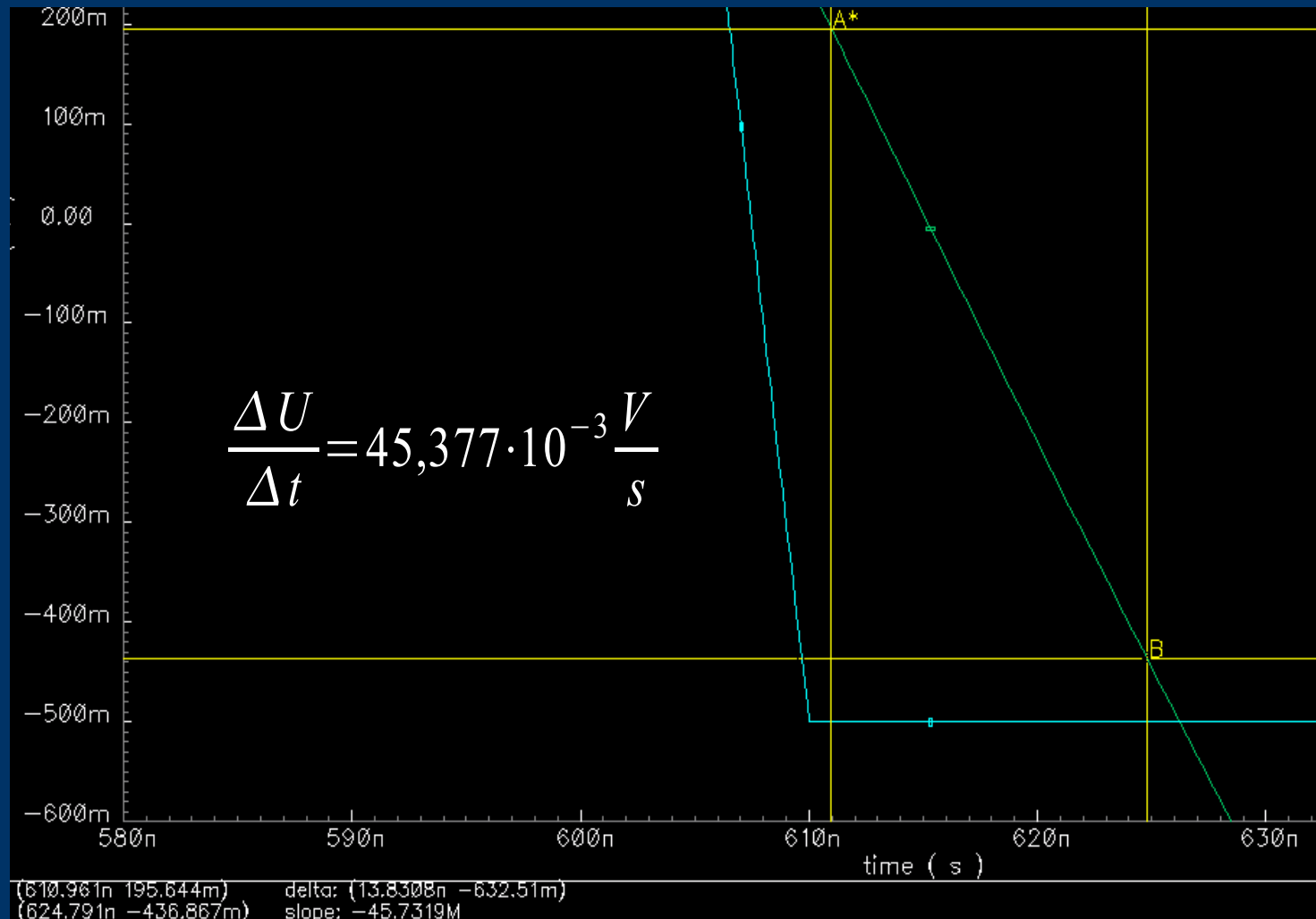
Verifizierung - Voltageswing



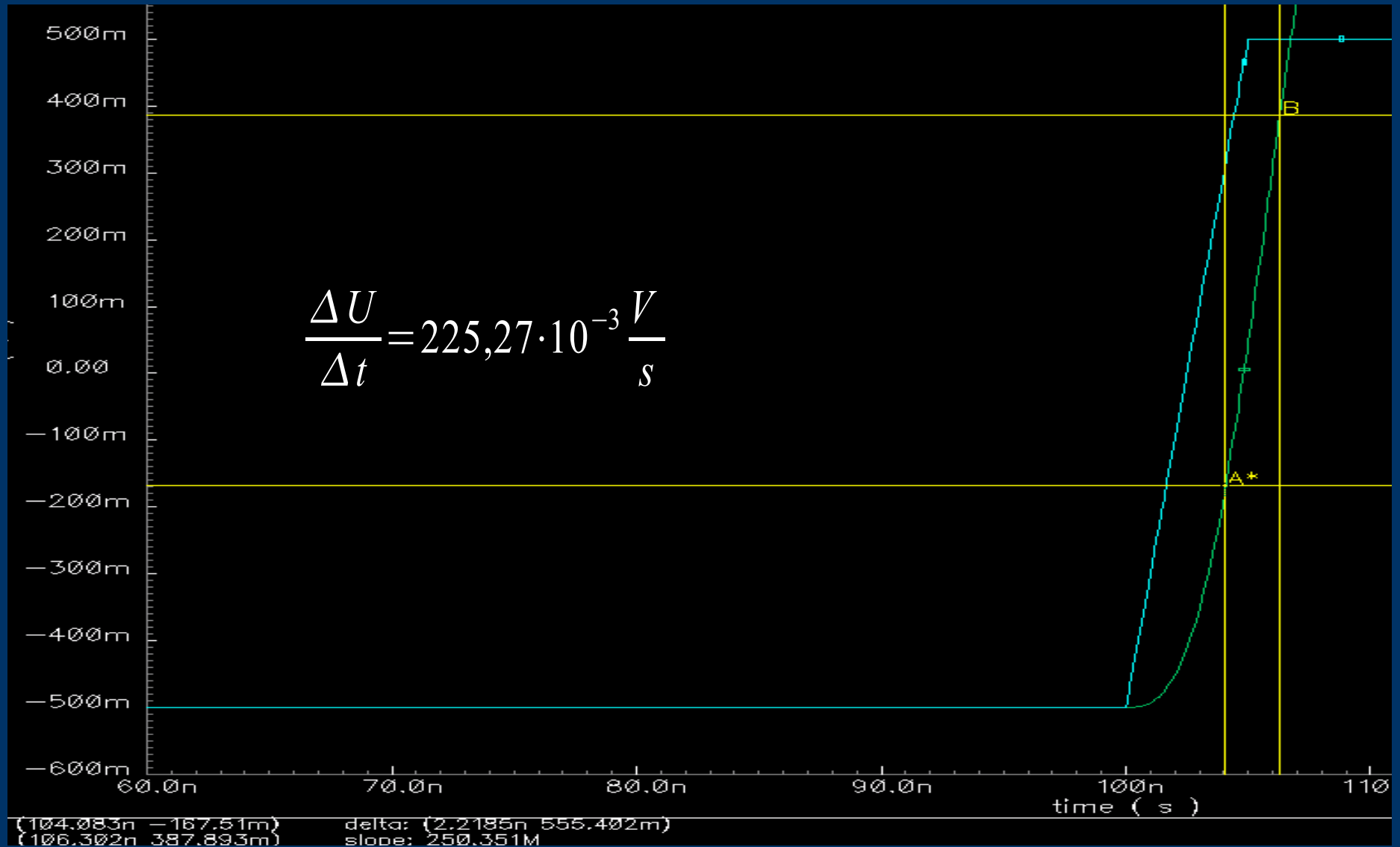
Verifizierung - Powerdissipation



Verifizierung - Slewrate



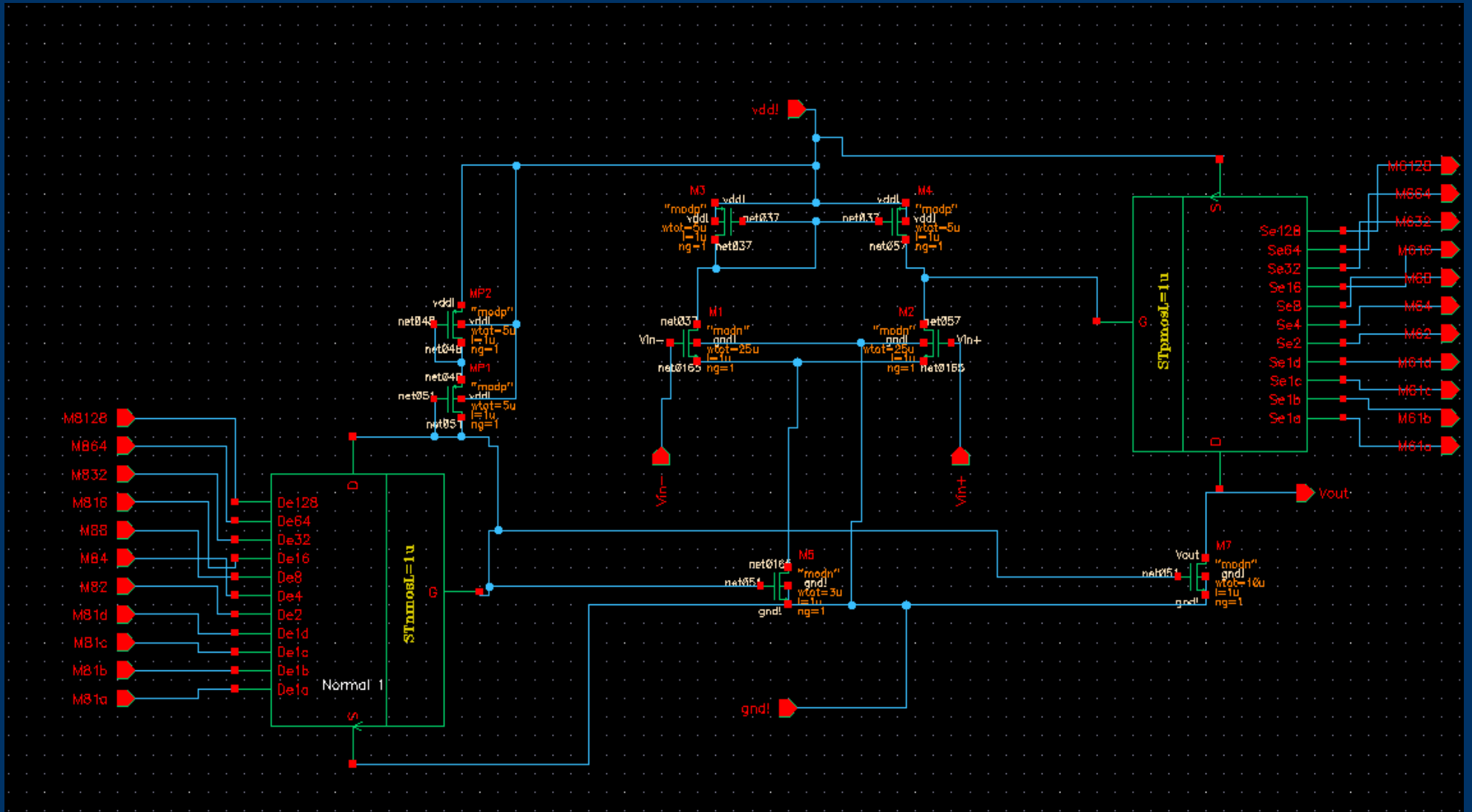
Verifizierung – Slewrate II



Verifizierung - Übersicht

Open Loop Gain	75	76,3
Gain Bandwidth	1,00E+07	7,87E+07
Slew Rate	10	45,37
Offset	1,00E-06	7,36E-07
CMR -	-0,5	-0,54
CMR +	1	1,03
Output swing -	-0,35	-1,6
Output swing +	0,35	1,5
Cmrr	80	91,6
Power dissipation	1,00E-03	9,70E-04

Scalable Devices

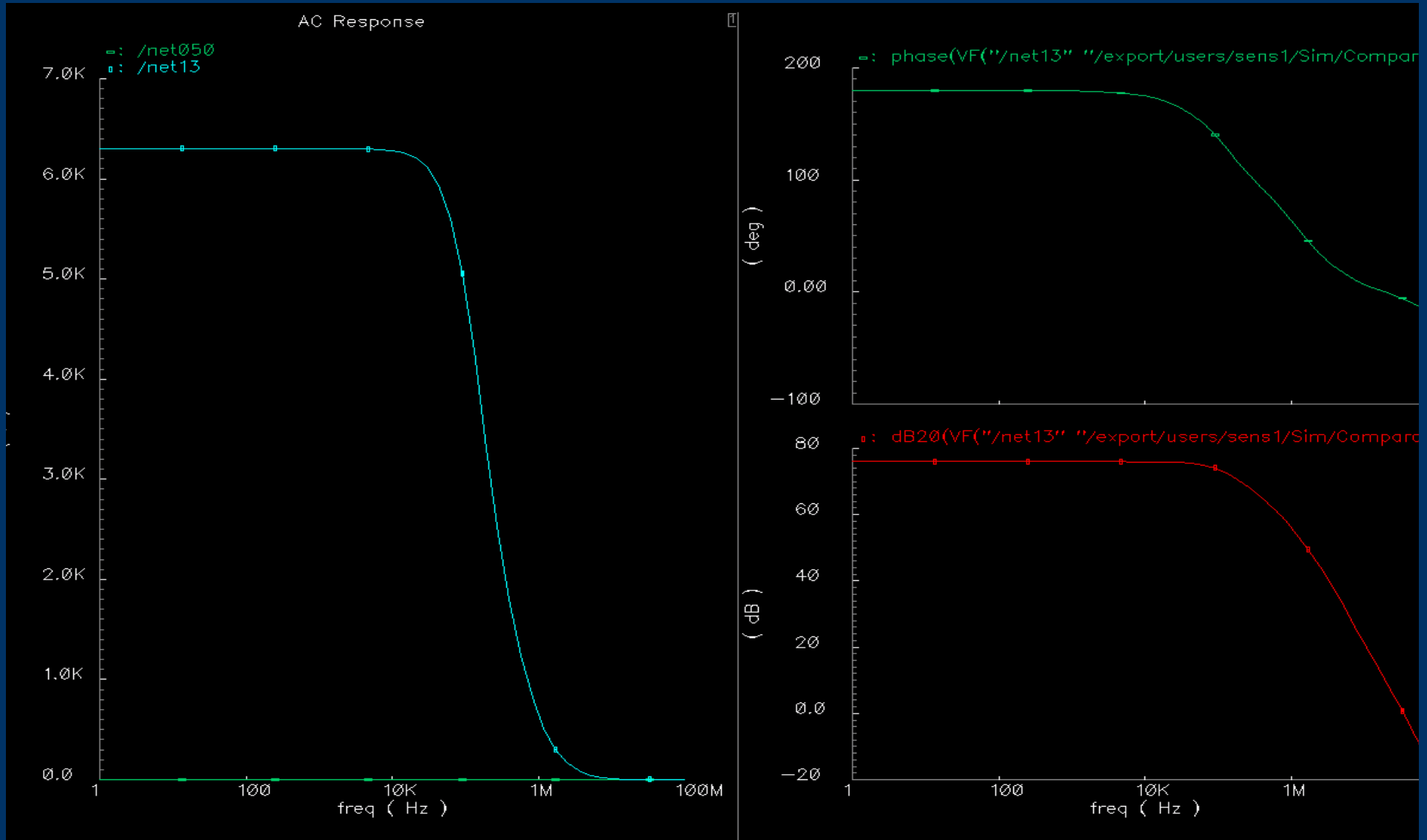


Scalable Devices

M 1	25
M 2	25
M 3	5
M 4	5
M 5	3
M 6	73
M 7	10

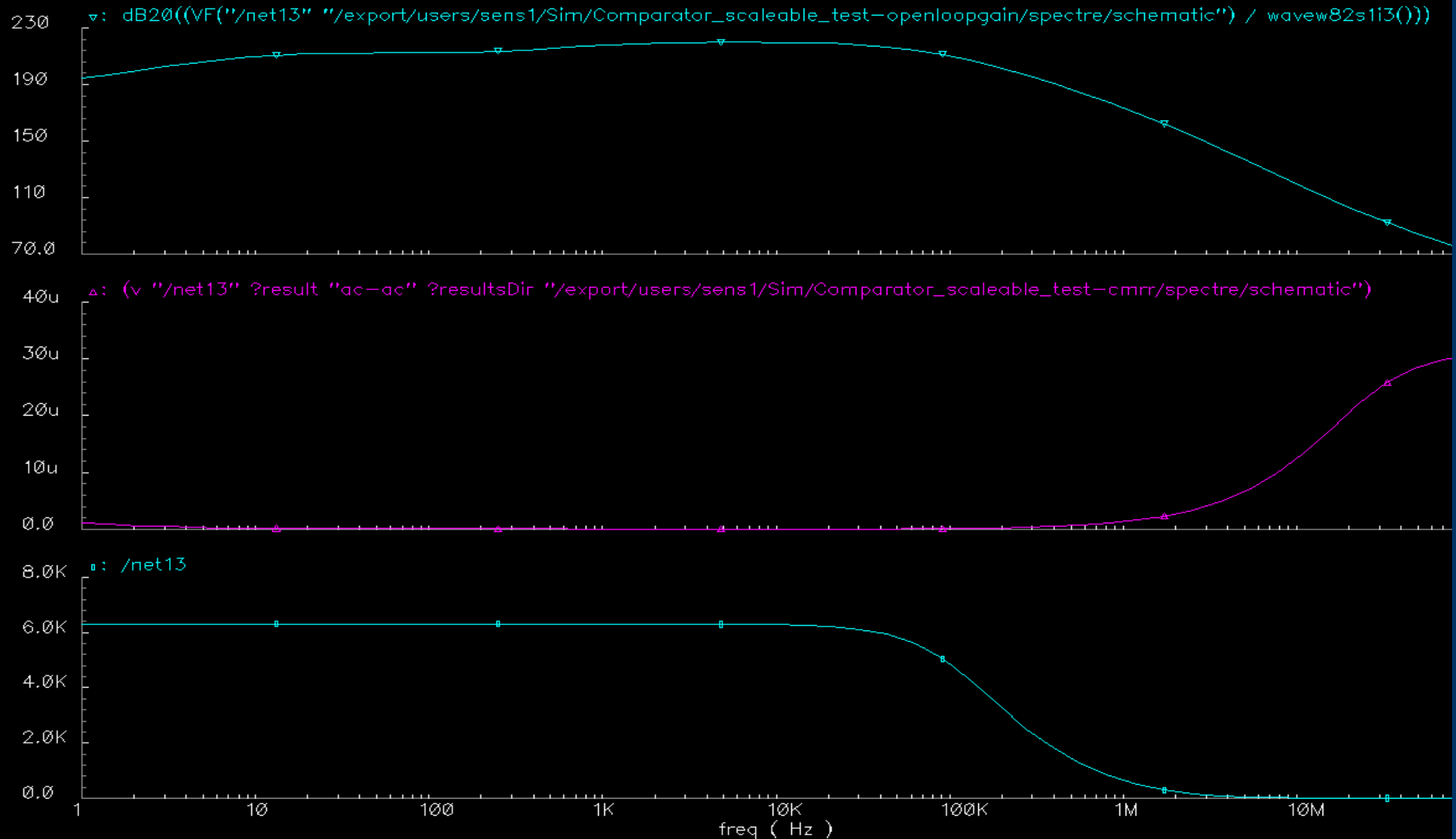
Werte nach einer
Offsetanpassung
aufgrund des hohen
Innenwiderstands der
SD's.

Verifizierung – Gain und GBW

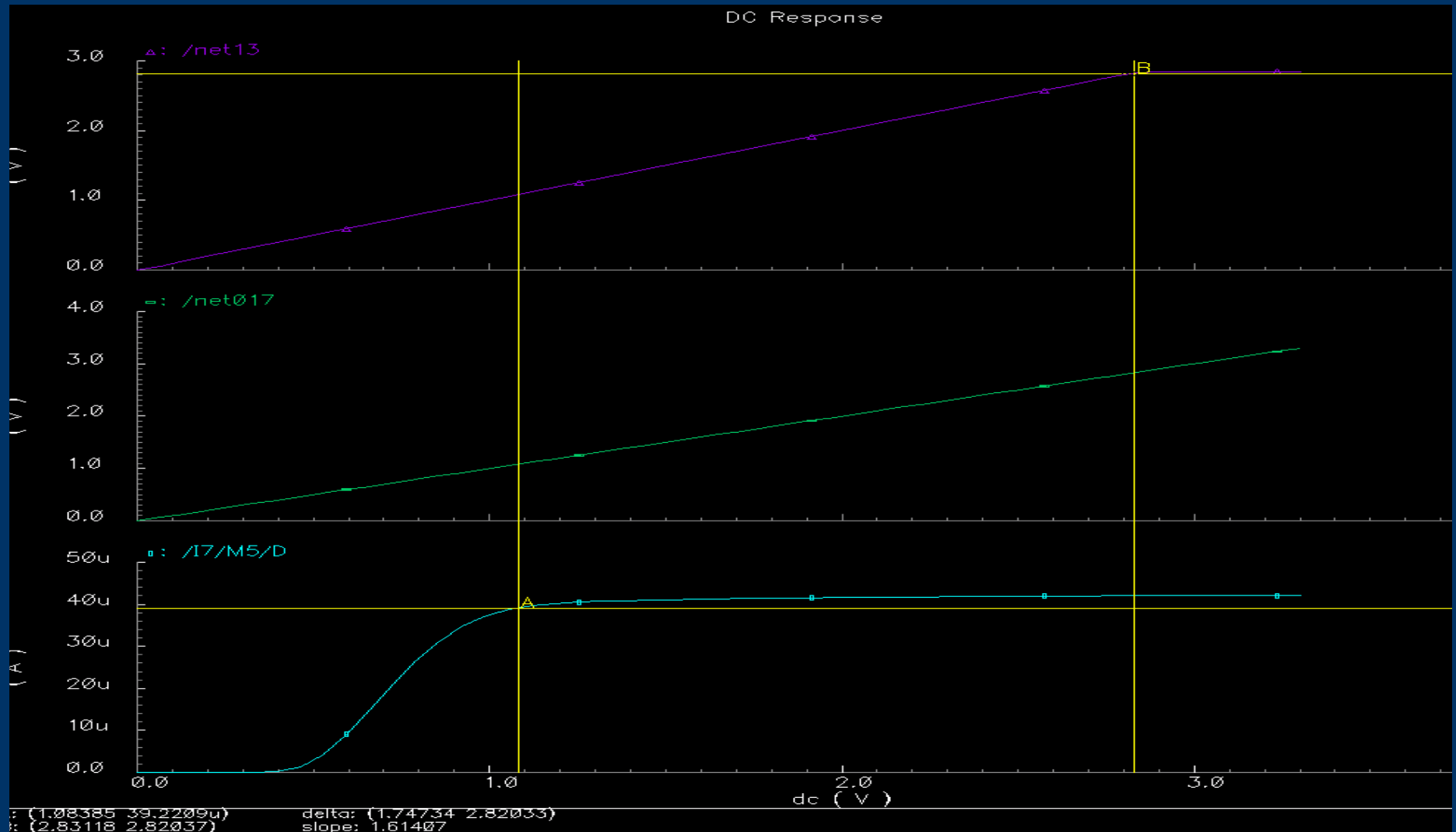


Verifizierung - CMRR

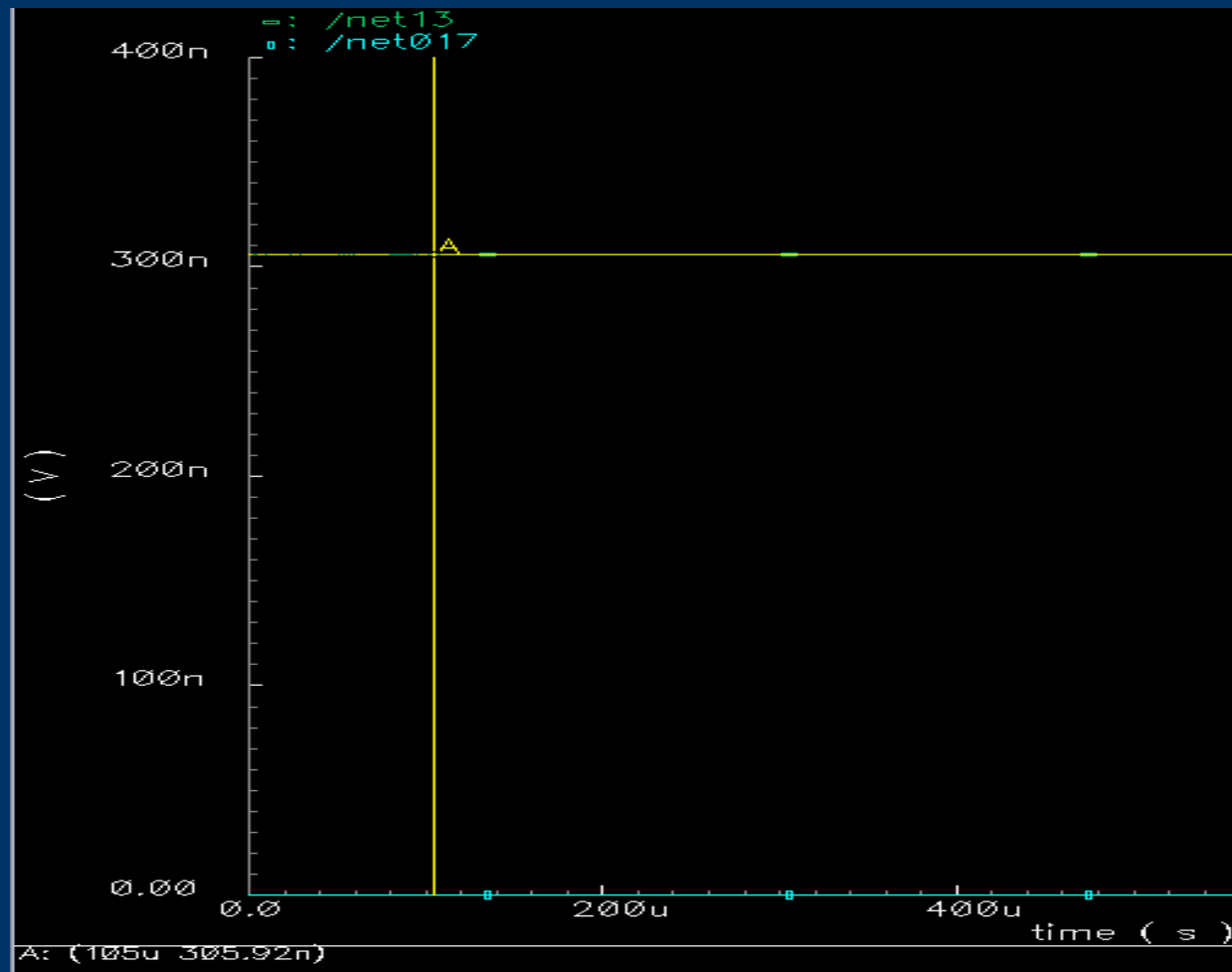
AC Response



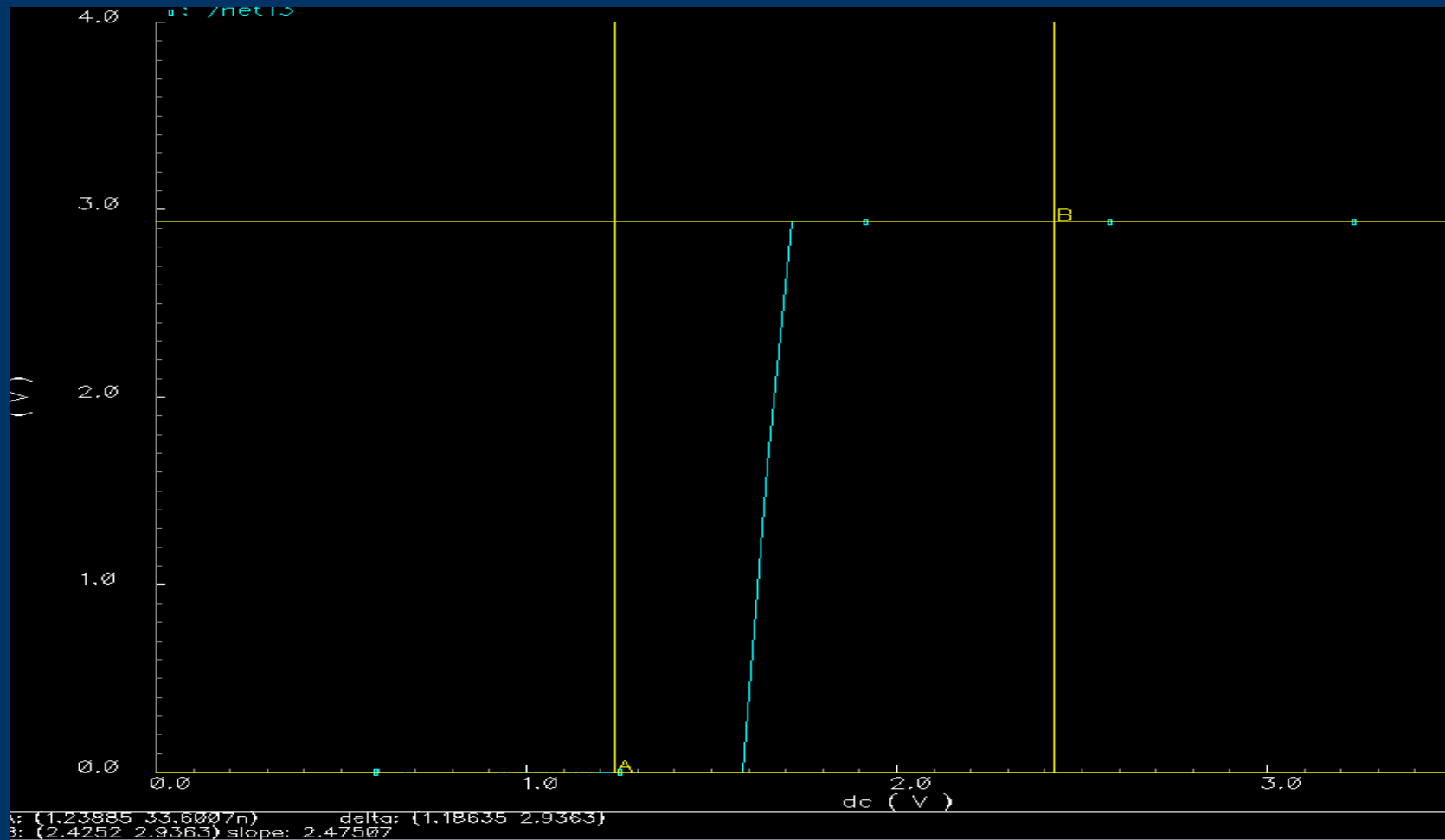
Verifizierung - CMR



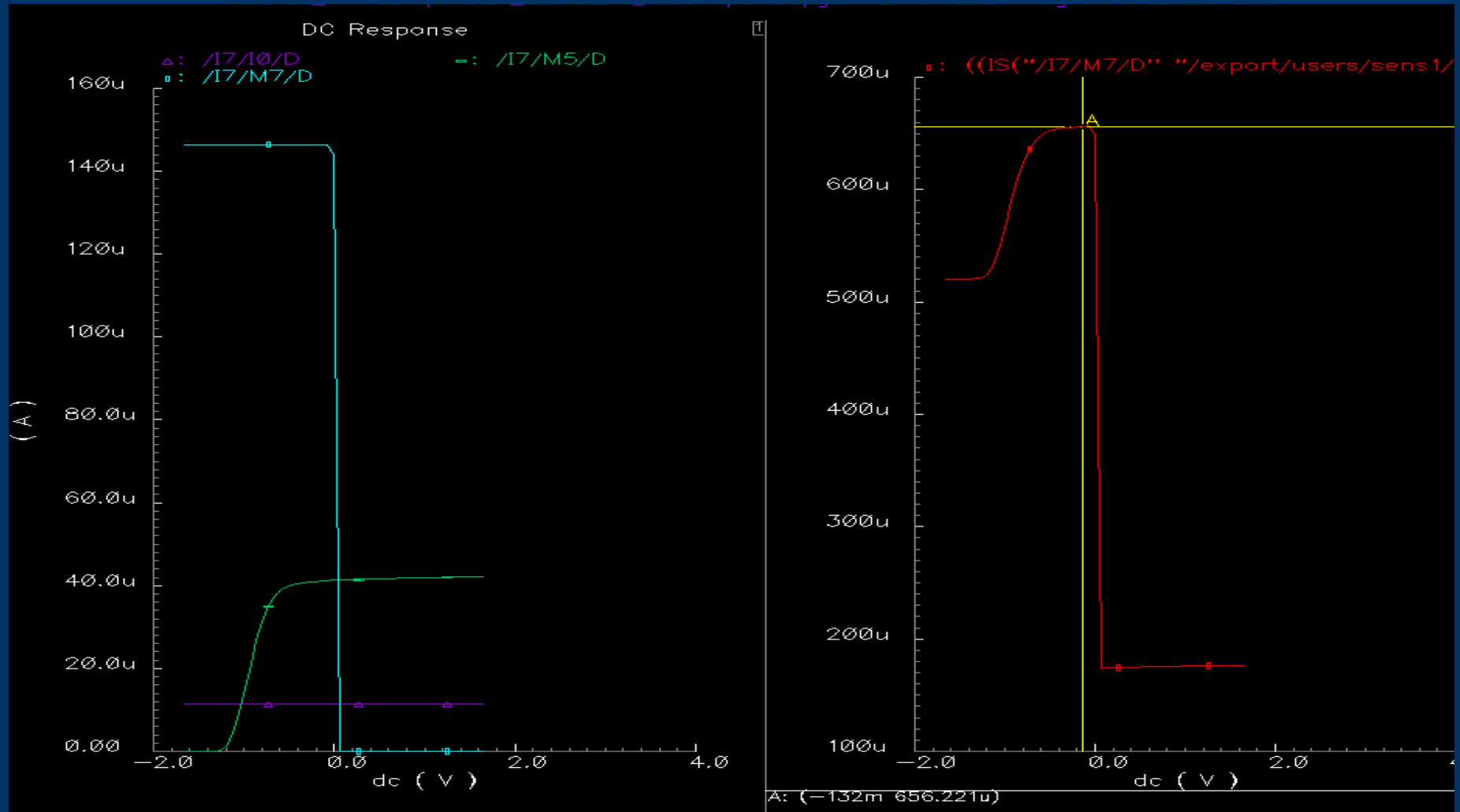
Verifizierung - Offset



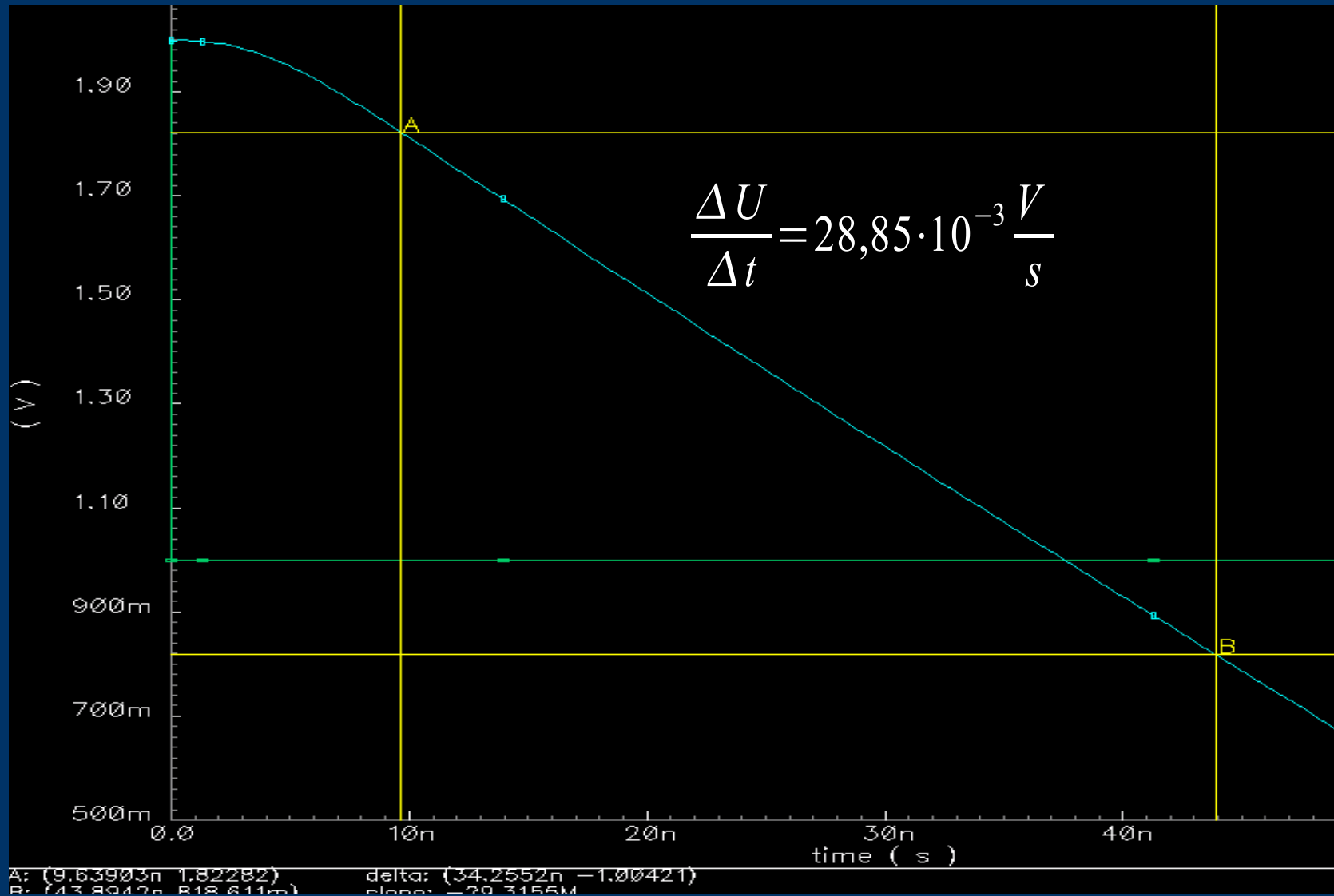
Verifizierung - Voltageswing



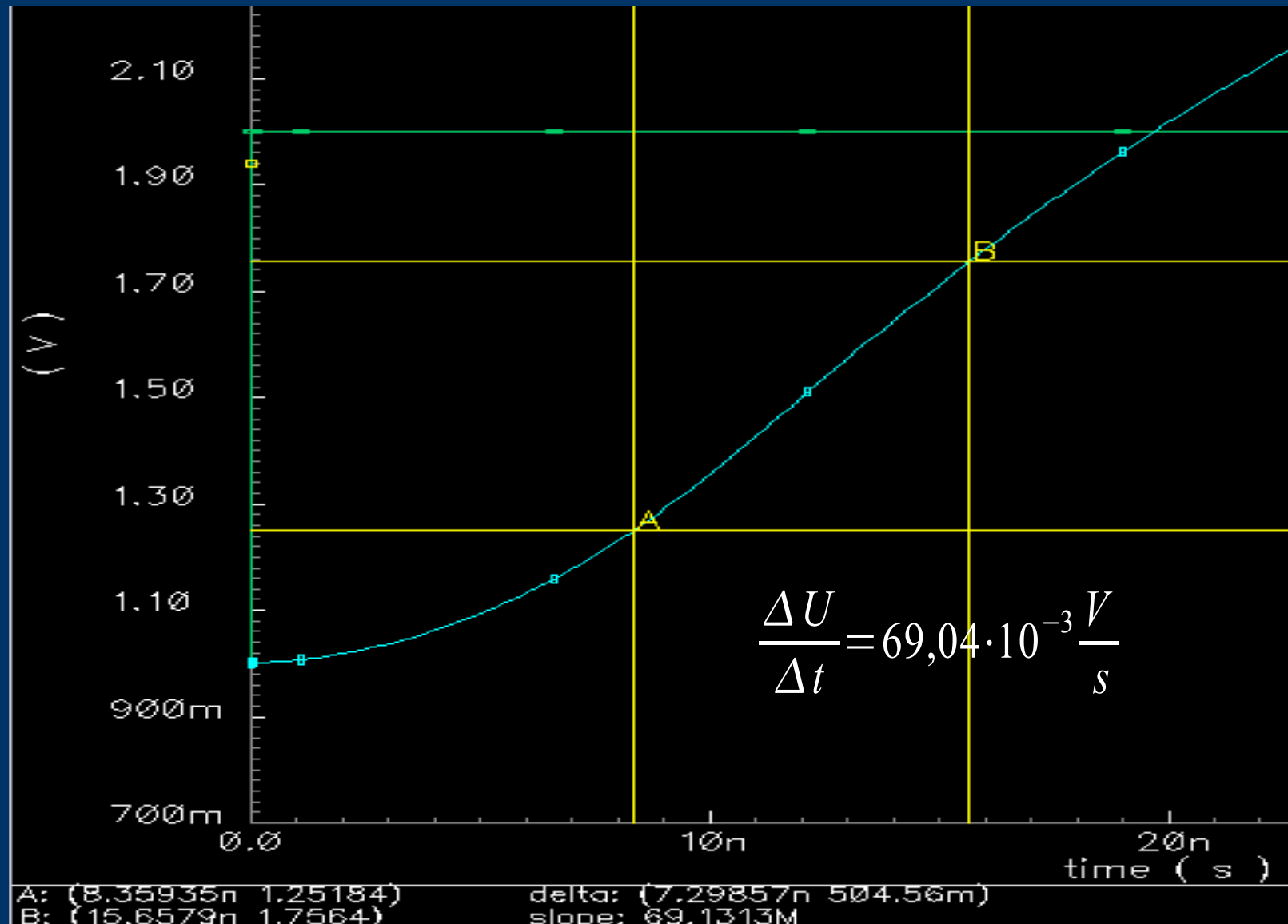
Verifizierung - Powerdissipation



Verifizierung - Slewrate



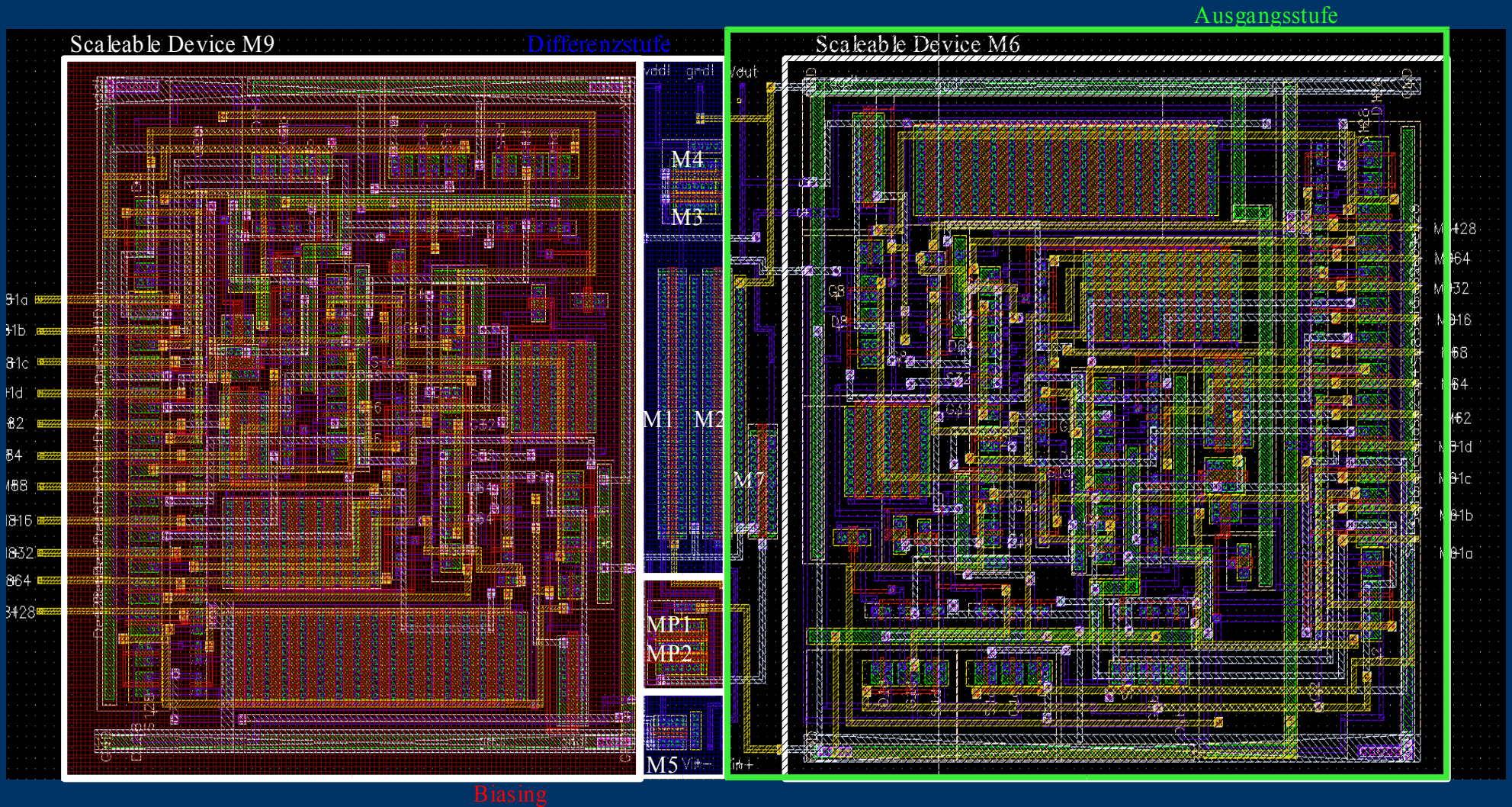
Verifizierung - Slewrate



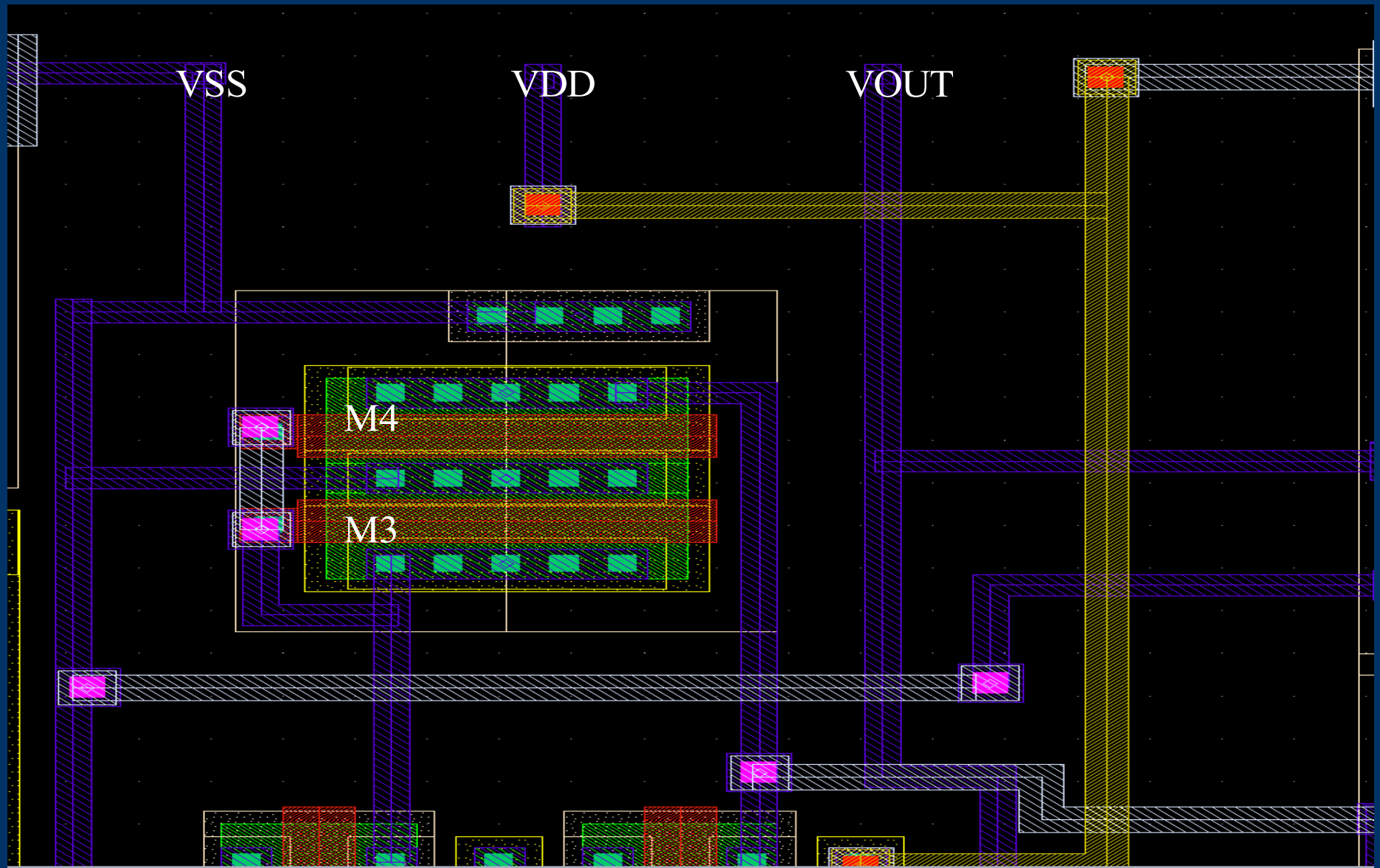
Verifizierung - Übersicht

	Vorgabe	Schematic	Scaleable
Open Loop Gain	75	76,3	78
Gain Bandwidth	1,00E+07	7,87E+07	~ 7,7E+07
Slew Rate	10	45,37	28,85
Offset	1,00E-06	7,36E-07	3,50E-07
CMR -	-0,5	-0,54	-0,56
CMR +	1	1,03	1,18
Output swing -	-0,35	-1,6	-1,64
Output swing +	0,35	1,5	1,28
Cmrr	80	91,6	~200
Power dissipation	1,00E-03	9,70E-04	6,50E-04

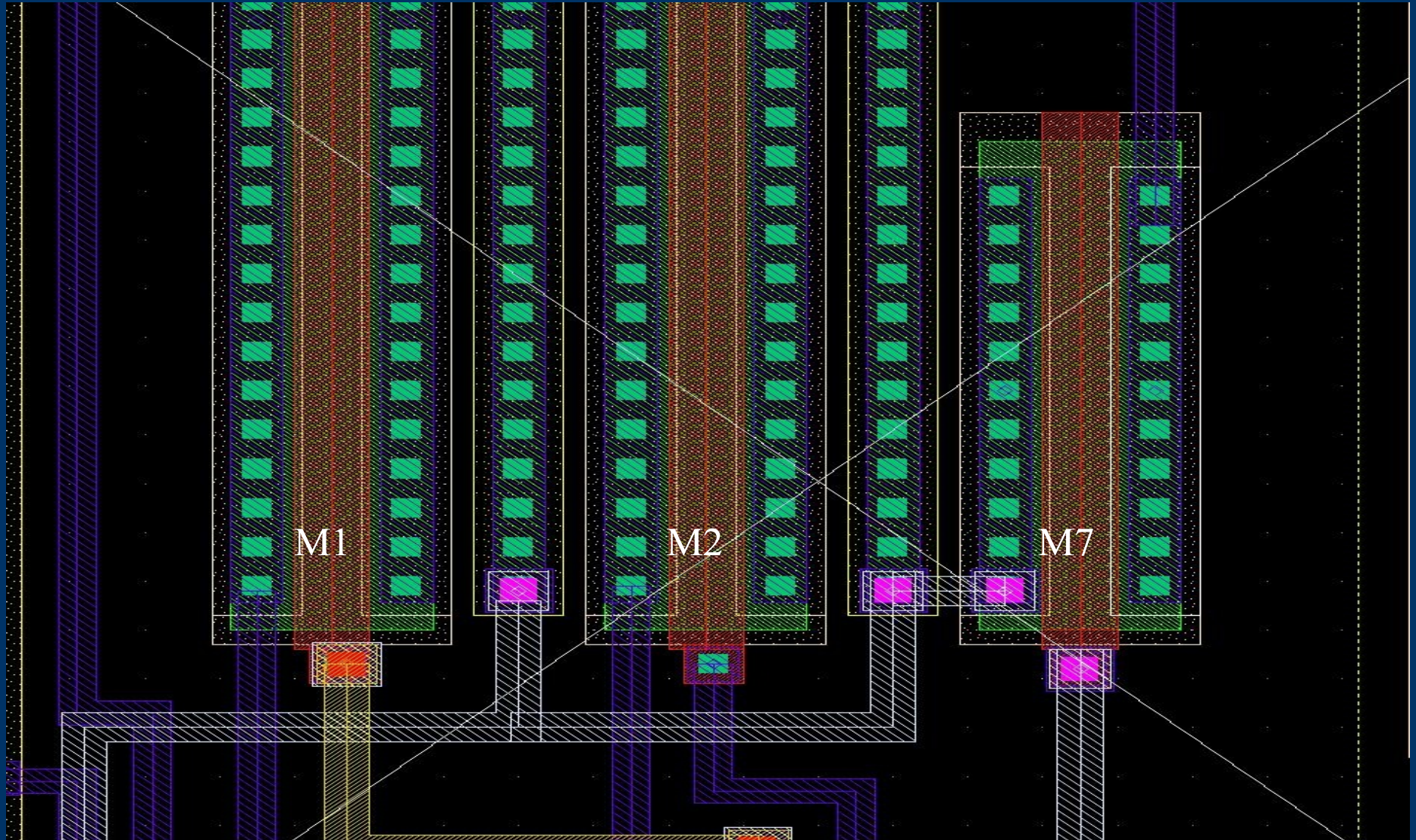
Layout



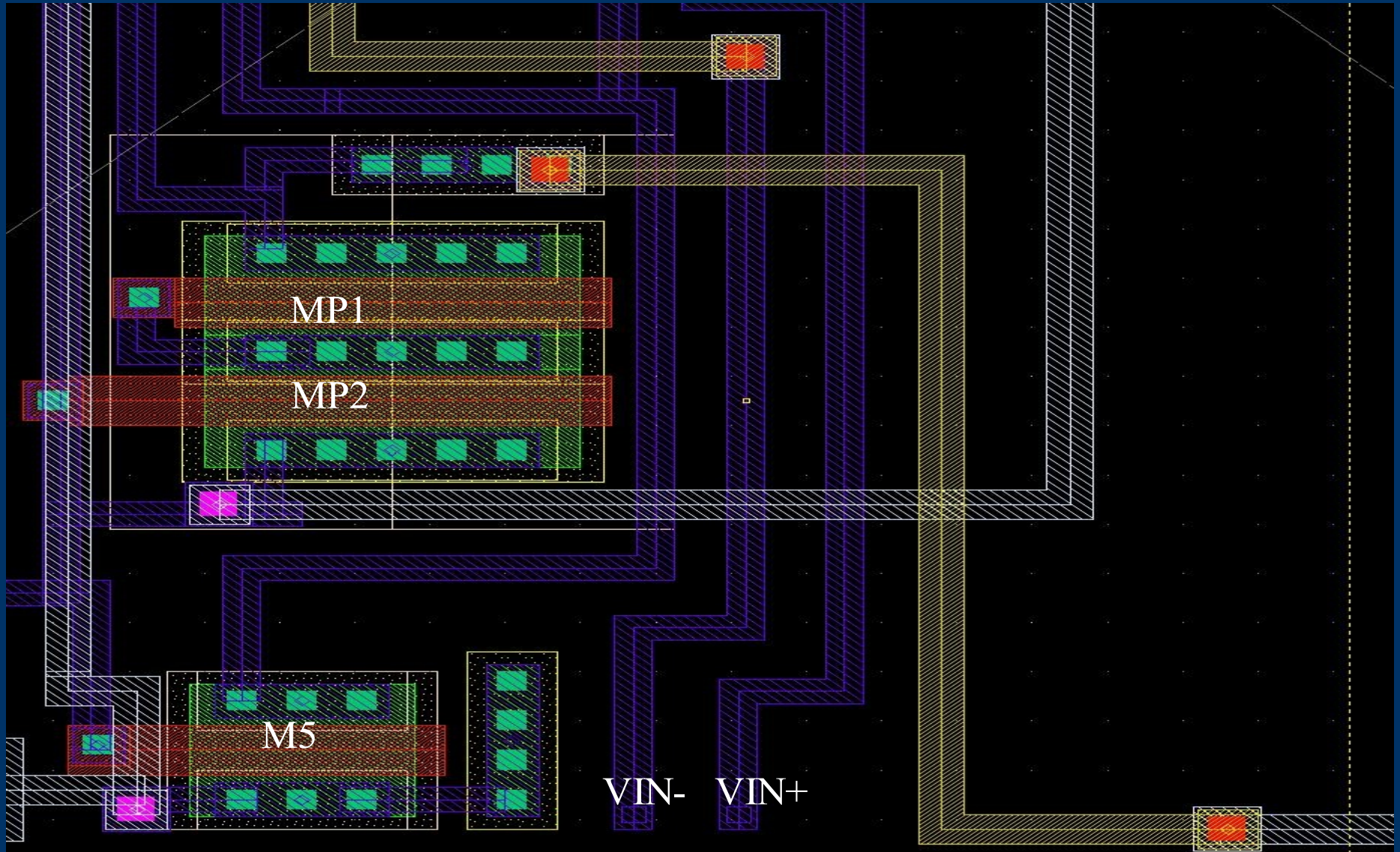
Layout - Detail



Layout - Detail



Layout - Detail



LVS-Check

Running simulation in directory: "/export/users/sens1/LVS".

Loading all available p-cell functions
ROD pcell code loaded

```
Begin netlist: Nov 7 11:56:37 2007
  view name list = ("auLvs" "extracted" "schematic" "symbol")
  stop name list = ("auLvs")
  library name   = "course HM"
  cell name     = "Comparator scaleable"
  view name     = "extracted"
  globals lib   = "basic"
Running Artist Flat Netlisting
End netlist:   Nov 7 11:56:38 2007
```

```
Moving original netlist to extNetlist
Removing parasitic components from netlist
presistors removed: 0
pcapacitors removed: 0
pinductors removed: 0
pdiodes removed: 11
trans lines removed: 0
100 nodes merged into 100 nodes
```

```
Begin netlist: Nov 7 11:56:38 2007
  view name list = ("auLvs" "schematic" "cmos_sch" "netlist" "symbol")
  stop name list = ("auLvs")
  library name   = "course HM"
  cell name     = "Comparator scaleable"
  view name     = "schematic"
  globals lib   = "basic"
Running Artist Flat Netlisting
End netlist:   Nov 7 11:56:39 2007
```

```
Moving original netlist to extNetlist
Removing parasitic components from netlist
presistors removed: 0
pcapacitors removed: 0
pinductors removed: 0
pdiodes removed: 0
trans lines removed: 0
130 nodes merged into 130 nodes
```

LVS-Check

```
Running netlist comparison program: LVS
Begin comparison: Nov 7 11:56:39 2007
LVS version 5.0.0 05/30/2003 19:44 (cds11939) $
Warning: Unknown device "zd2sm24" on a compareDeviceProperty command.
[.]
Warning: Unknown device "nd" on a permuteDevice command.
```

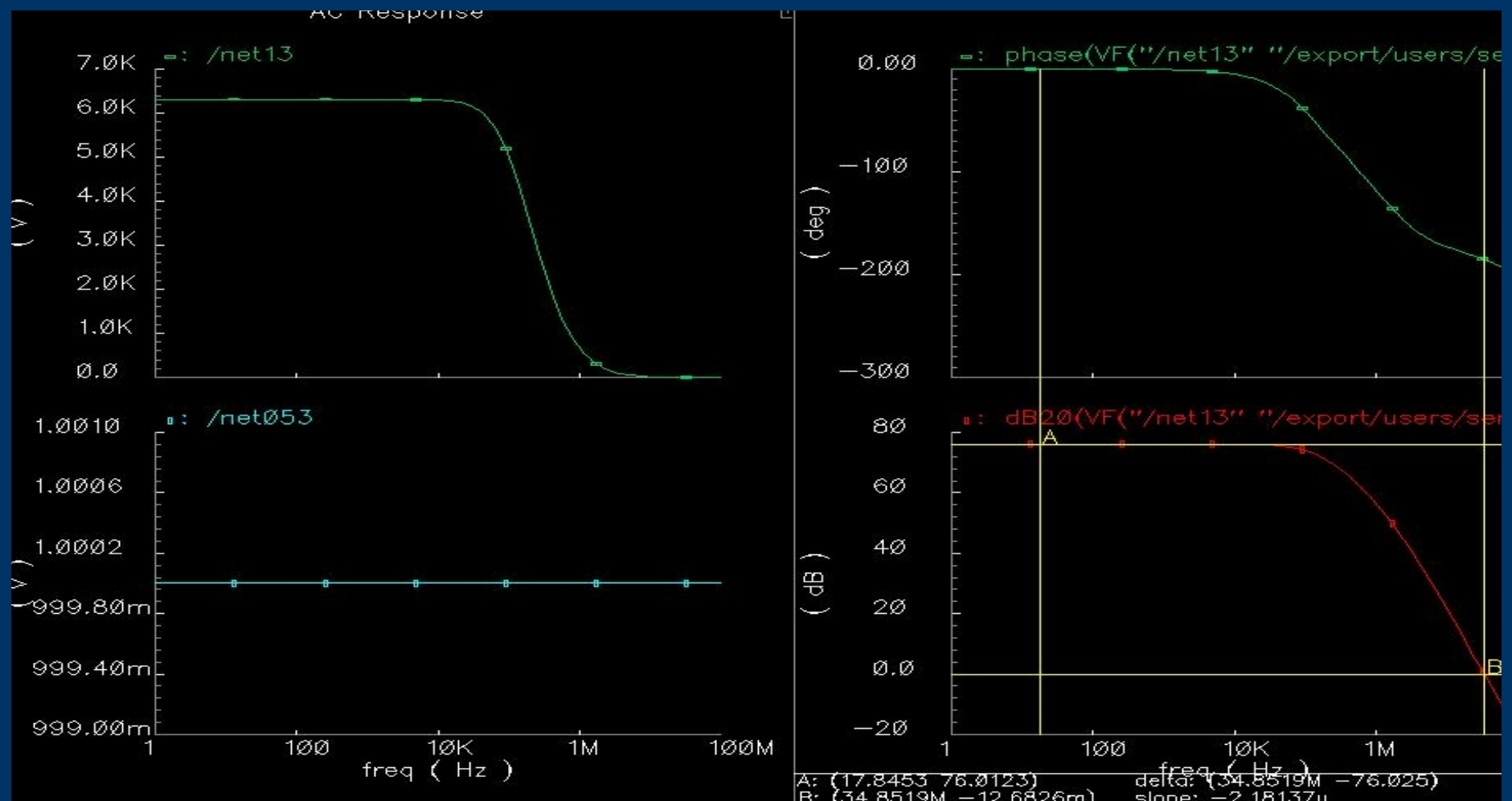
The net-lists match.

	layout	schematic
	instances	
un-matched	0	0
rewired	0	0
size errors	0	0
pruned	0	0
active	258	206
total	258	206
	nets	
un-matched	0	0
merged	0	0
pruned	0	0
active	100	100
total	100	100
	terminals	
un-matched	0	0
matched but different type	0	0
total	27	27

```
End comparison: Nov 7 11:56:39 2007
```

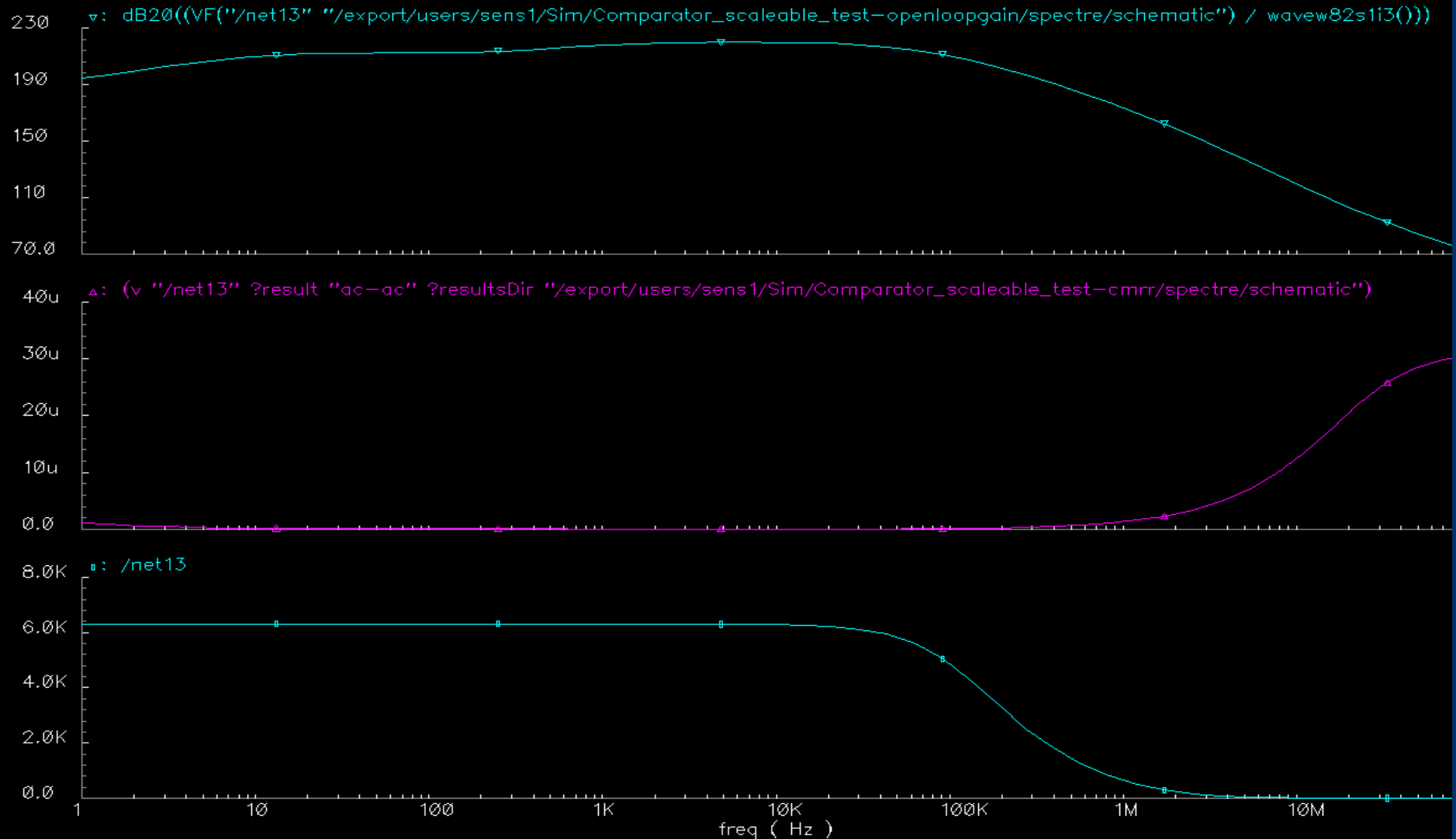
Comparison program completed successfully.

Verifizierung – Gain und GBW

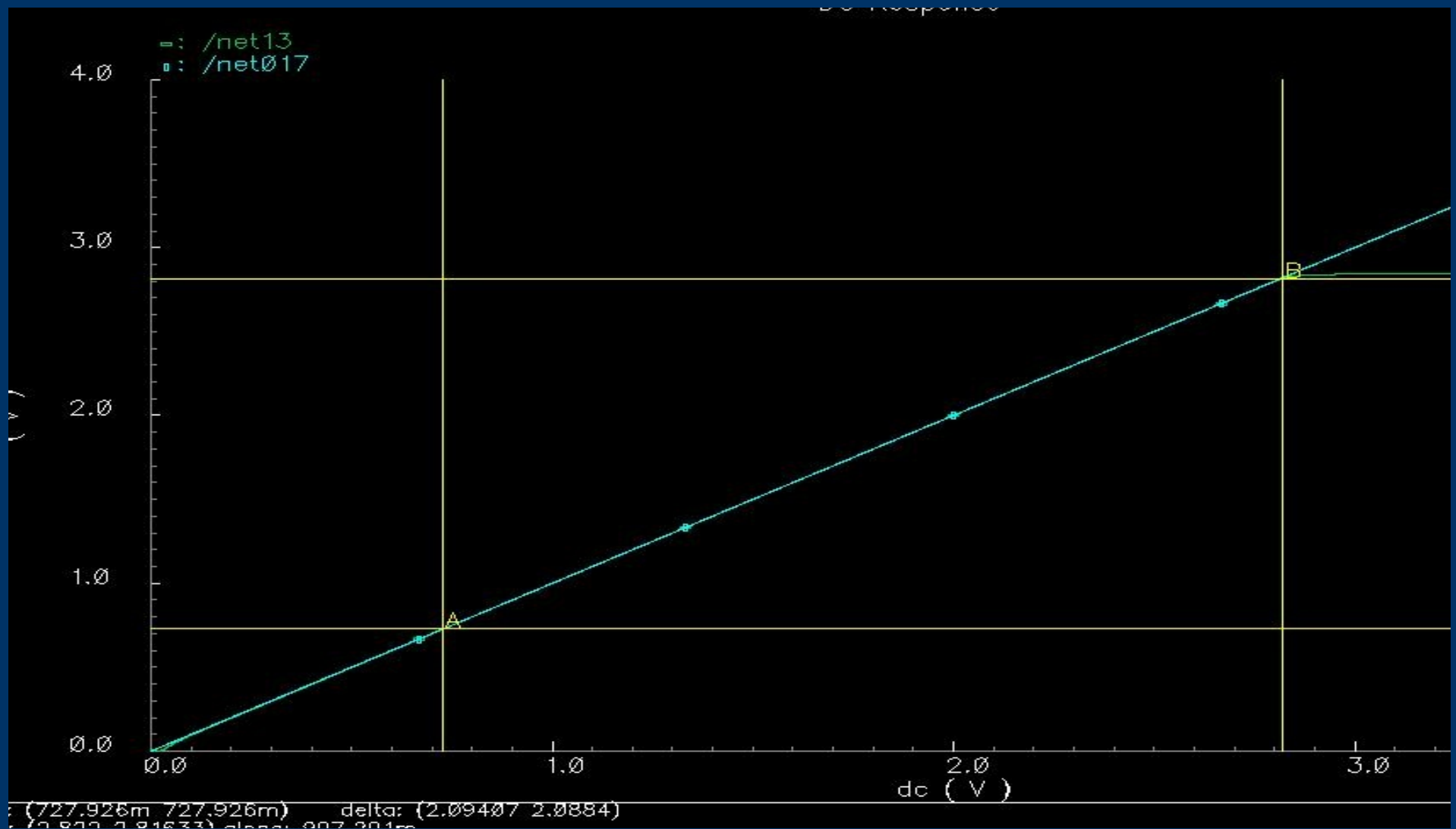


Verifizierung - CMRR

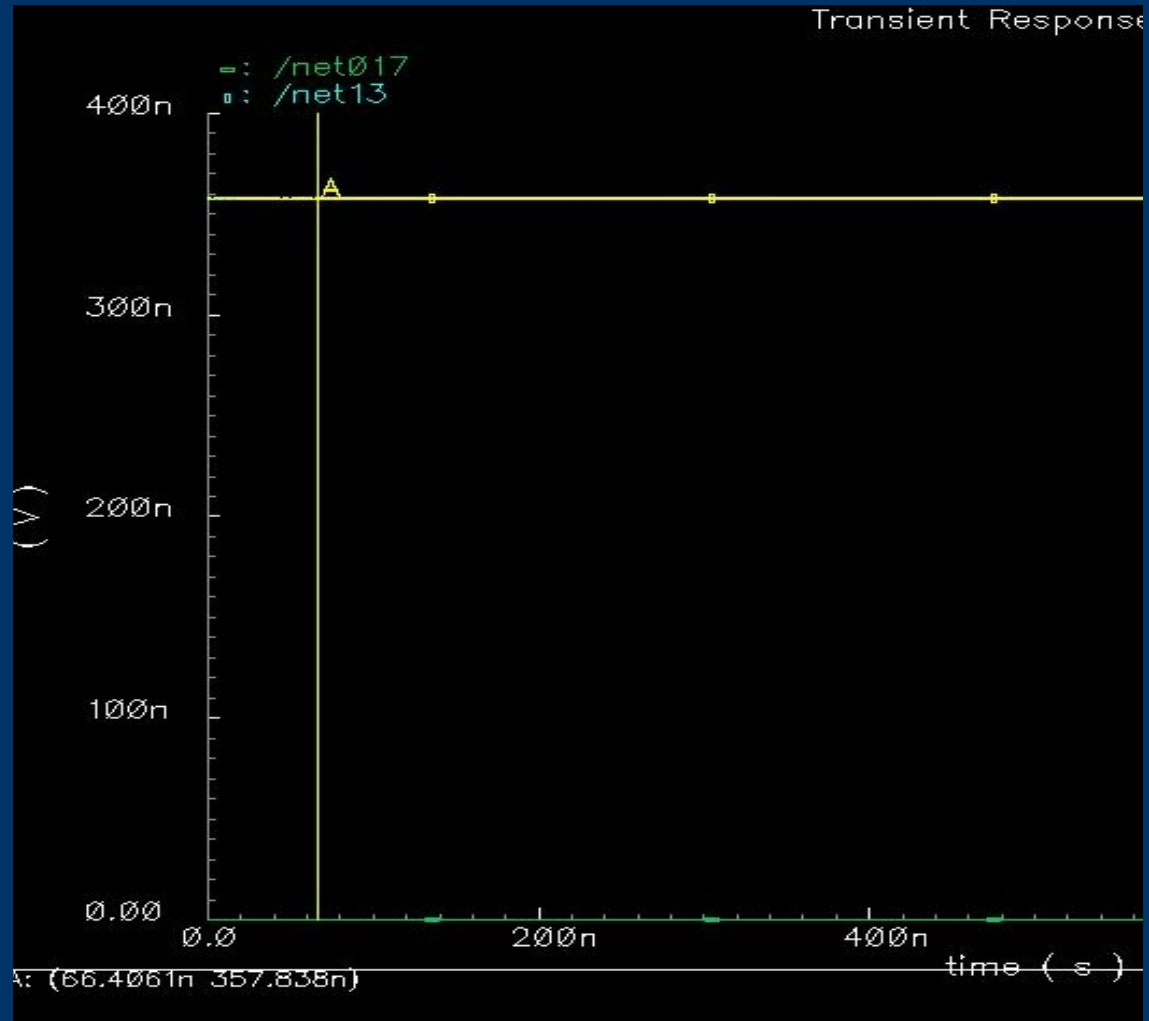
AC Response



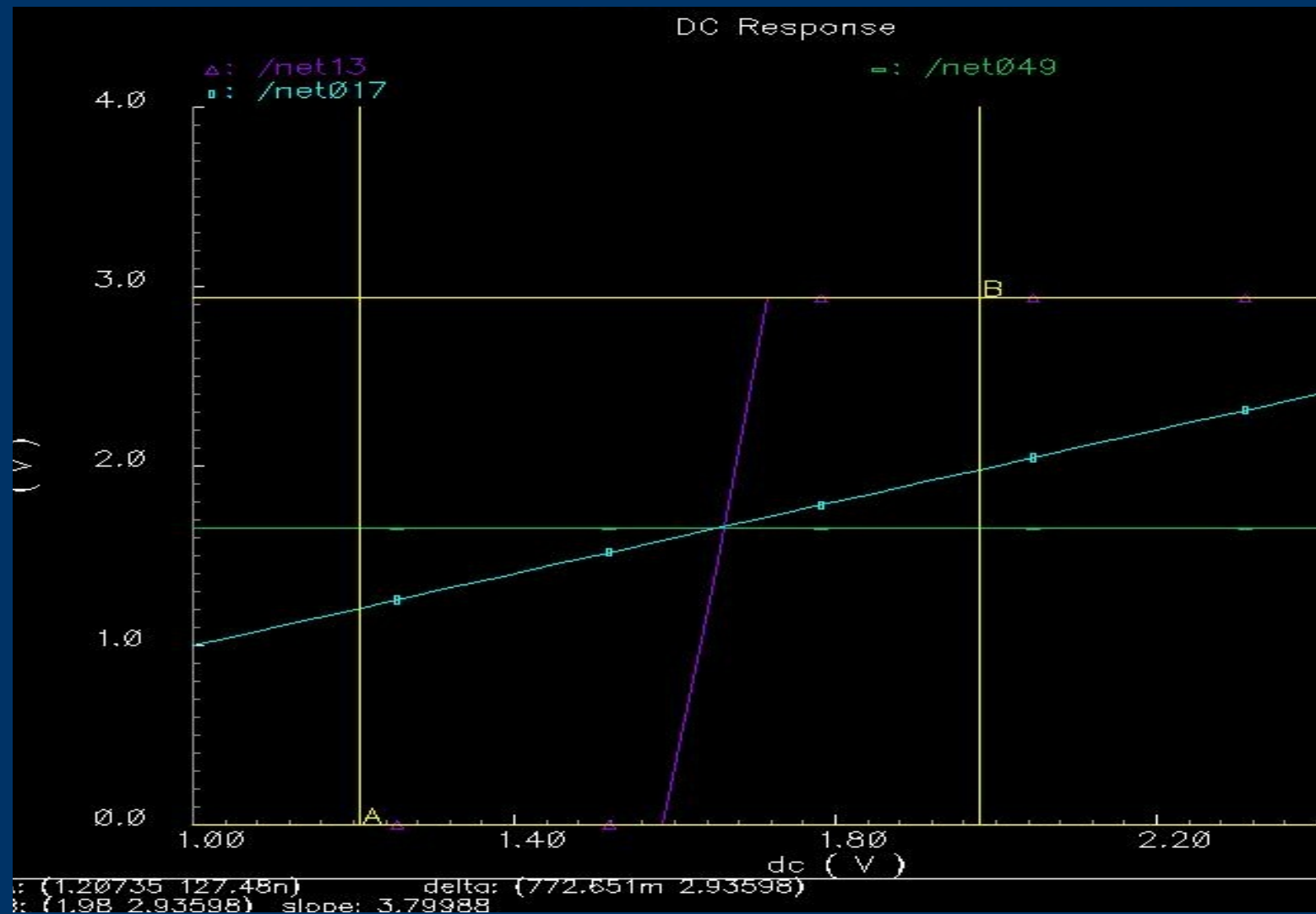
Verifizierung - CMR



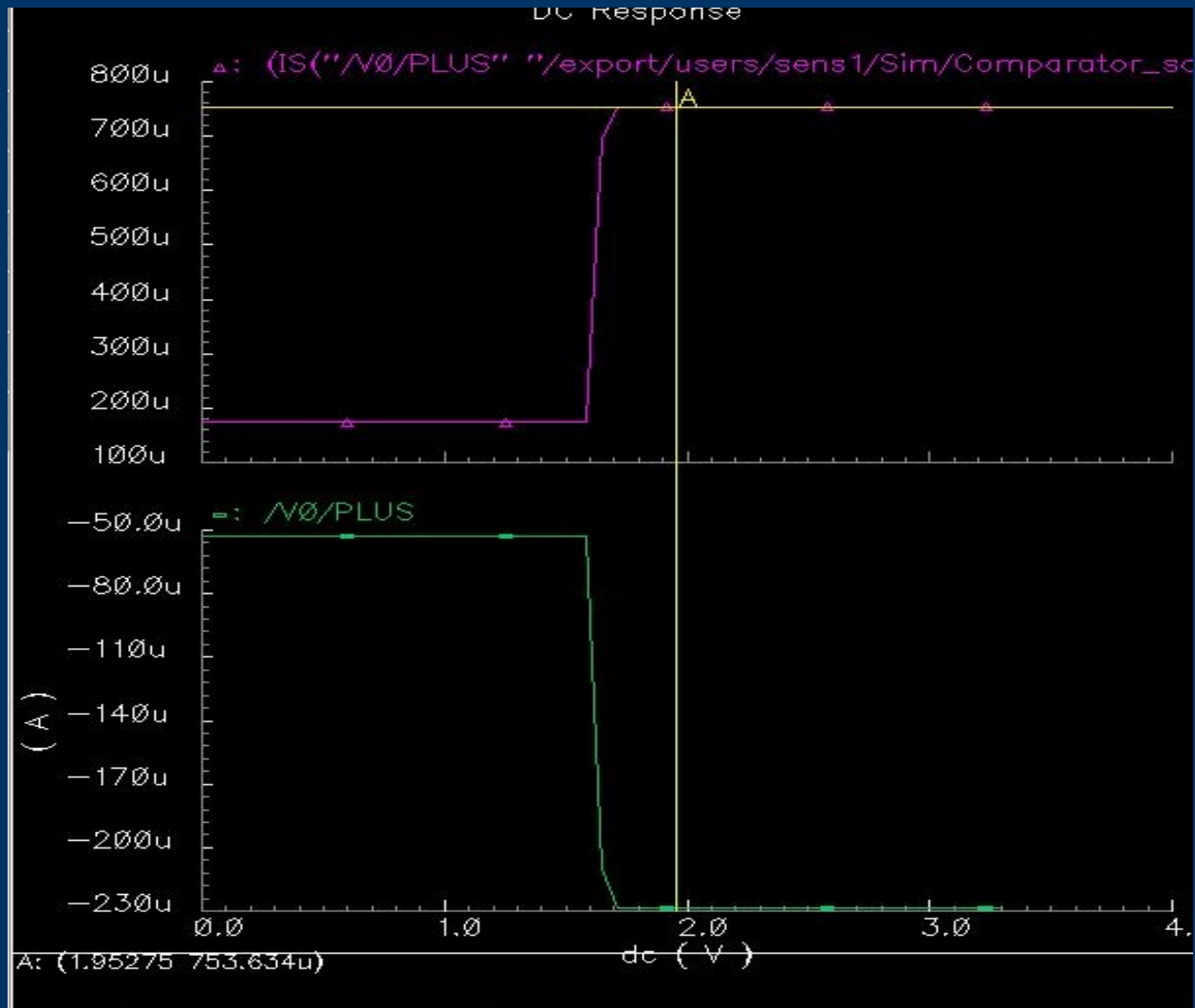
Verifizierung - Offset



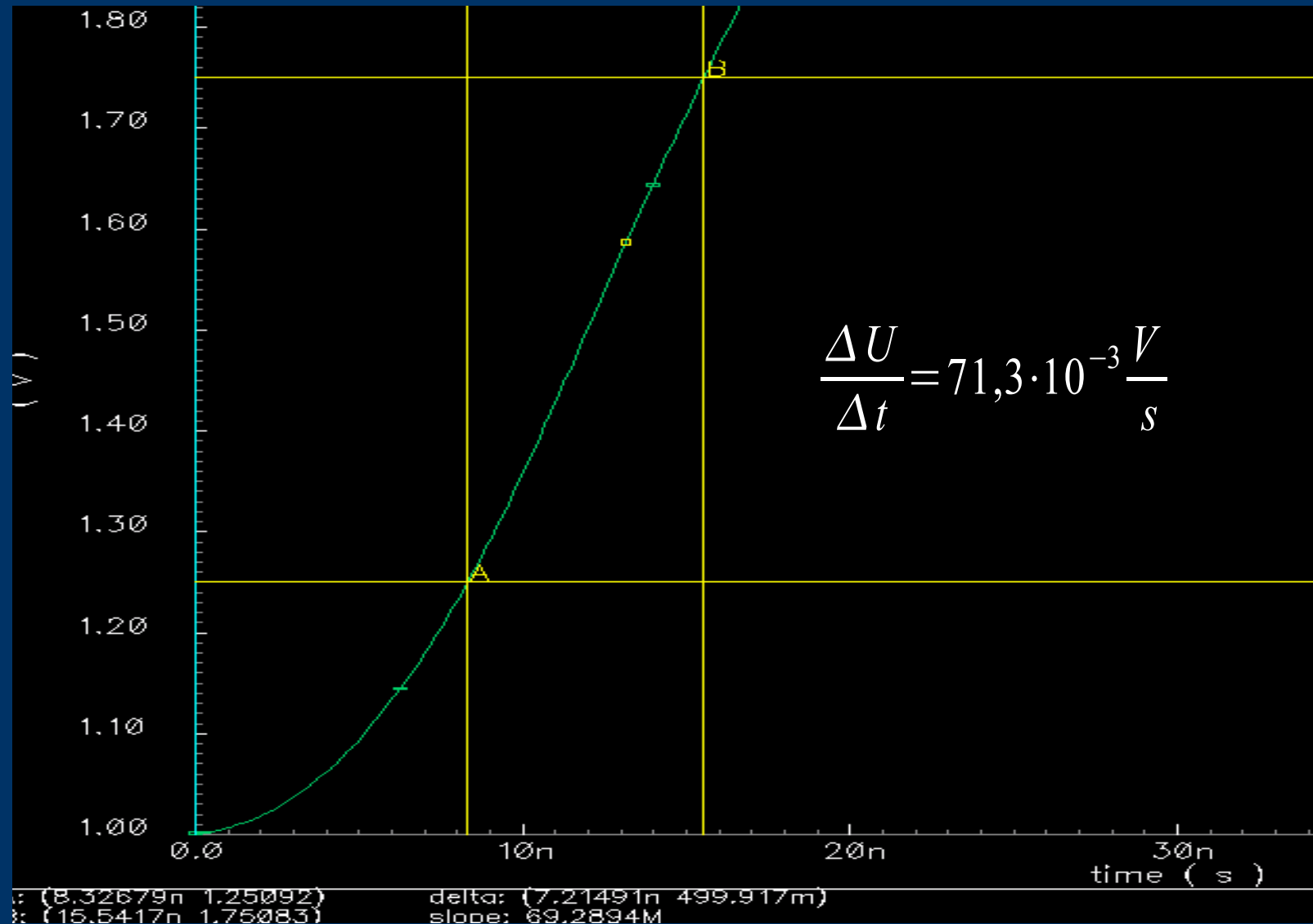
Verifizierung - Voltageswing



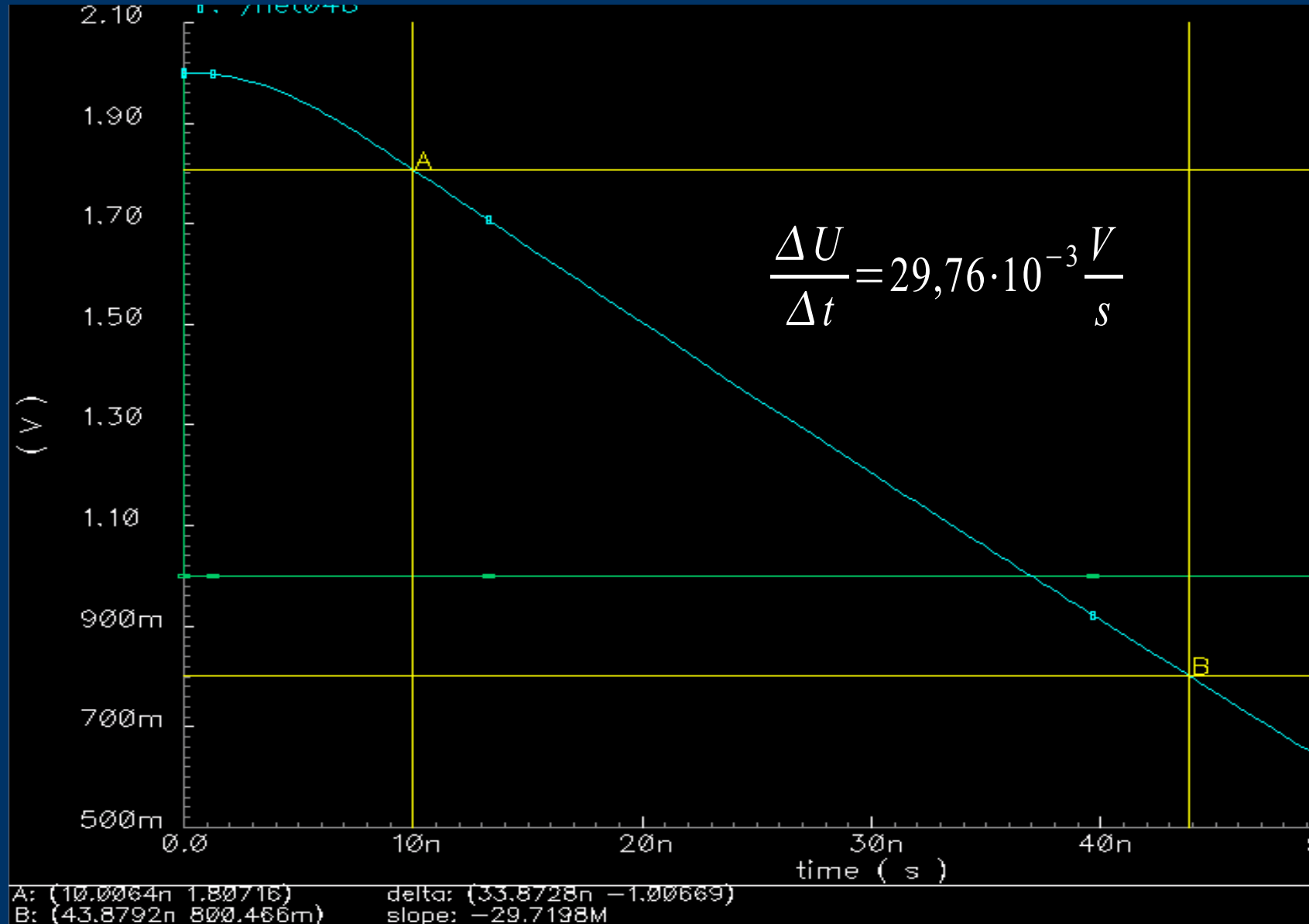
Verifizierung - Powerdissipation



Verifizierung - Slewrate



Verifizierung - Slewrate



Verifizierung - Übersicht

	Vorgabe	Schematic	Scaleable	Extracted
Open Loop Gain	75	76,3	76	78,08
Gain Bandwidth	1,00E+07	7,87E+07	~7,7E+07	~7,6E+07
Slew Rate	10	45,37	28,85	29,76
Offset	1,00E-06	7,36E-07	3,50E-07	3,57E-07
CMR -	-0,5	-0,54	-0,56	~ -0,92
CMR +	1	1,03	1,18	1,17
Output swing -	-0,35	-1,6	-1,64	-1,64
Output swing +	0,35	1,5	1,28	1,28
Cmrr	80	91,6	~200	~200
Power dissipation	1,00E-03	9,70E-04	6,50E-04	7,50E-04