Miller-Verstärker

Vom Entwurf über die Simulation zum Layout-Design.

Eine Projektarbeit zum Fach Sensorelektronik SS07 von

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29.11.07

Inhalt:

- Entwurf der Schaltung über Allen/Holberg und Kursgrundlagen
- Simulation und Anpassung der Werte
- Einführen von 2 skalierbaren Transistoren
- Erneute Simulation
- Layout-Design und LVS-Check

Vorgaben:

Open Loop Gain	>80 db	Output Swing	+/- 0,35 V
Gain Bandwith	10 MHZ	CMRR	>80 db
Phase Margin	>65°	Power Dissipation	<1m W
Settling Time	<1µ s	Voltage Supply	0-3.3 V
Slew Rate	1V/µ s	Load Capacitance	5p F
Offset	<<1µ V	Load Resistance	100K Ω
Input CMR	+/- 1 V		

Berechnung der Millerkapazität:

Phasenrand:

$$\Phi_M = 65° = \pm 180° - \tan^{-1}\left(\frac{GB}{|p_1|}\right) - \tan^{-1}\left(\frac{GB}{|p_2|}\right) - \tan^{-1}\left(\frac{GB}{|z_1|}\right)$$

Mit den Verhältnissen:

$$\left(\frac{GB}{|z_1|}\right) = 1:10$$

$$\tan^{-1}\left(\frac{GB}{|p_1|}\right) = 90°$$

Ergibt sich eine Millerkapazität von:

$$C_C = 0.285 \cdot C_L = 1.43\,\mathrm{pF}$$

Aspect-Ratios:

Bestimmung nach Allen/Holberg:

$$S_1 = S_2 = \frac{g_{m2}^2}{K_2 I_5}$$

$$S_3 = S_4 = \frac{I_5}{K_3[V_{DD} - V_{in}(\max) - |V_{T03}|(\max) + V_{T1}(\min)]^2} \geq 1$$

$$S_5 = \frac{2 I_5}{K_5[V_{DS5}(sat)]^2}$$

$$S_6 = \frac{g_{m6}}{K_6 V_{DS6}(sat.)}$$

$$S_7 = \frac{I_6}{I_5} S_5$$

Excel - Entwurf

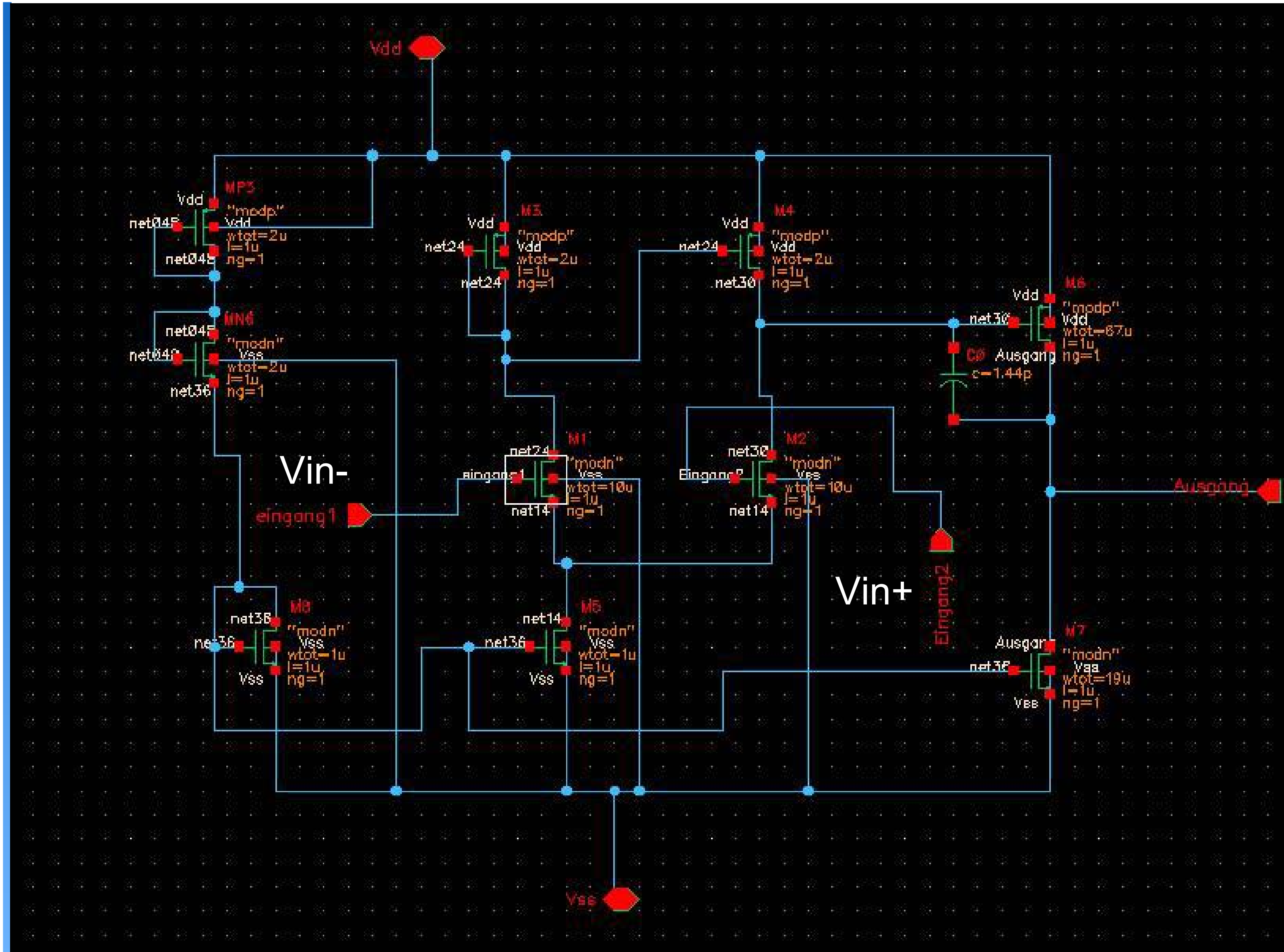
Cl [F]	Cc [F]	SR [V/s]	I [A]	CMR+ [V]	CMR- [V]	K' (N/P) [A/V	S=W/L	gm [S]	GB [Hz]
5E-12	1,43E-12	1,00E+06		0,5	-0,5	1,70E-04	1,00E+00	1,43E-05	1,00E
						5,80E-05	1,00E+00		
Cc/Cl * 10	φm [°]						1,00E+00		
2,8579996	65,00000004		1,18E-05				1,00E+00	5,22982E-05	
			2,36E-05				8,80E+00		
			6,44E-05				2,73E+00	1,43E-04	
							2,40E+01		
Vt(min) (N/F	Vt(max) [V]	λ (N/P) [1/V	β [A/V²]	Vds5 [V]	Vds7 [V]	Av	Pdiss [Watt]	ST [s]	
0,4	0,6	9,45E-03	1,70E-04	1,78E-01	0,177579486	2,14E+03	0,000290415	1,00E-06	
-0,55	-0,75	2,60E-02	5,80E-05						
				Vout_max	Vout_min				
				1,47E+00	1,472420514				

Aspect-Ratios:

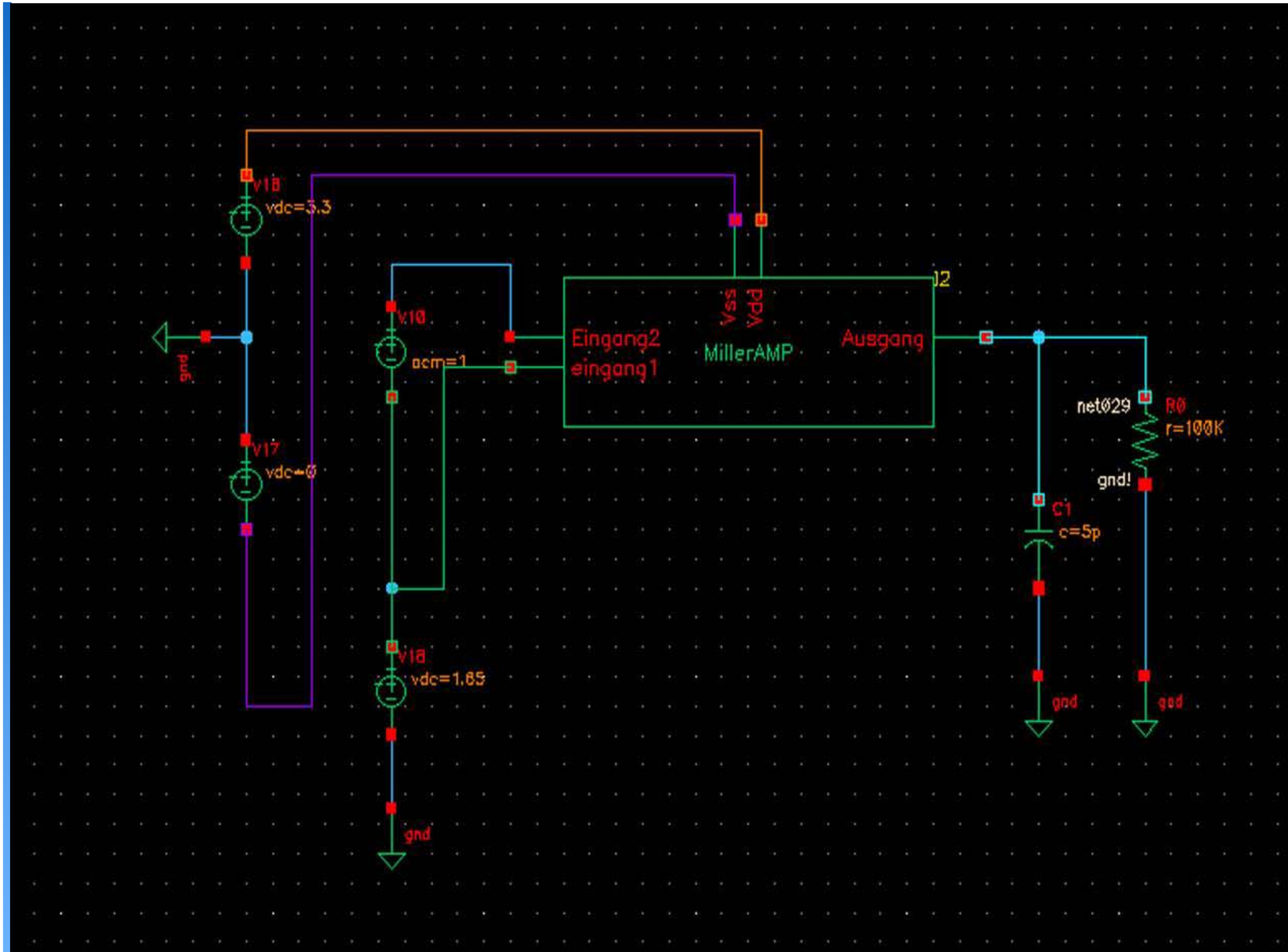
- Folgende Werte erhält man, nach Einsetzen der Formeln:

W/L_1	**1**
W/L_2	**1**
W/L_3	**1**
W/L_4	**1**
W/L_5	**8.8**
W/L_6	**2.73**
W/L_7	**2.40**

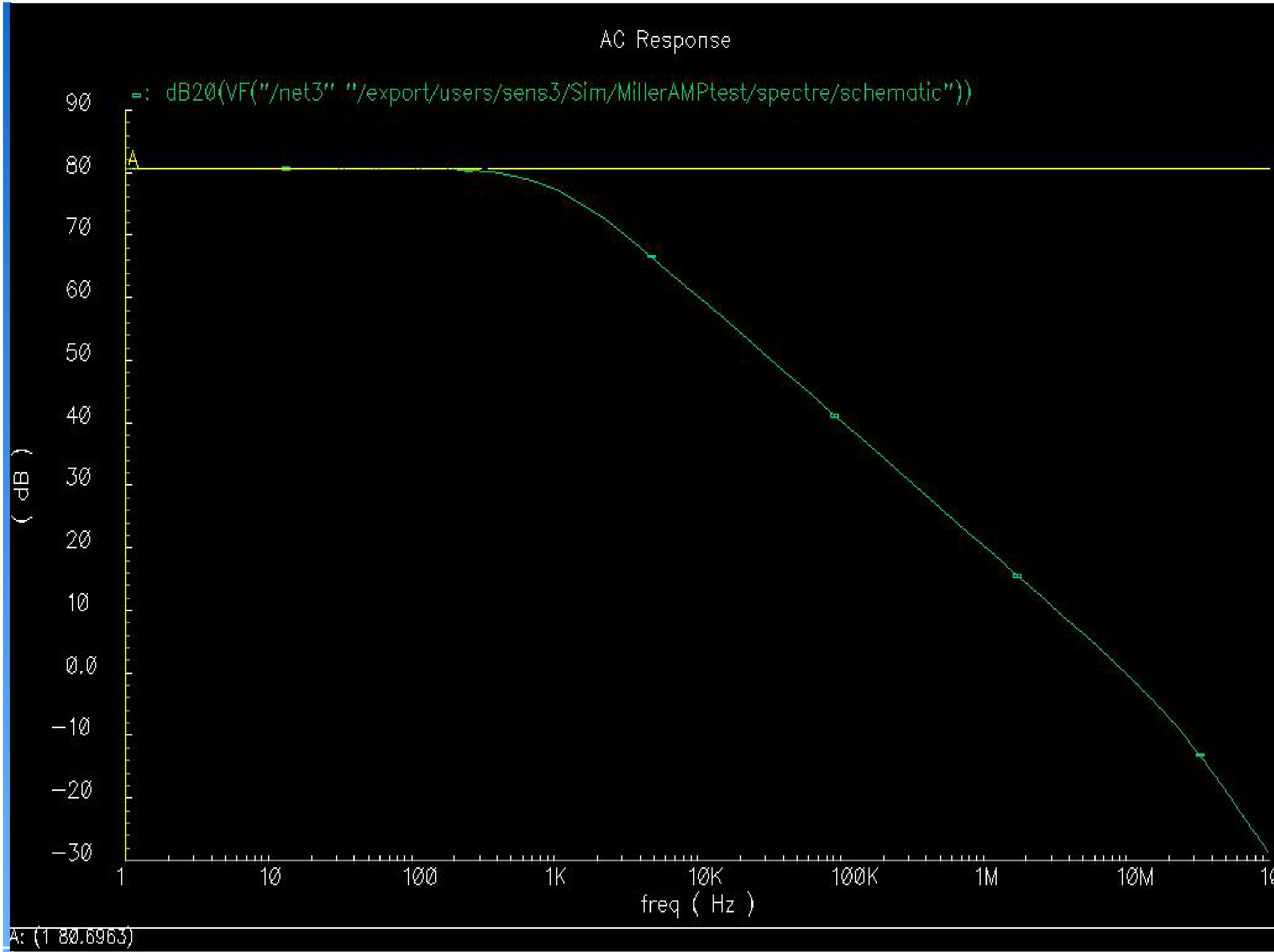
Simulation:


Vdd
MP3
"modp"
Vdd
wtot=2u
l=1u
ng=1
M3
"modp"
Vdd
wtot=2u
l=1u
ng=1
M4
"modp"
Vdd
wtot=2u
l=1u
ng=1
M6
"modp"
Vdd
wtot=87u
l=1u
ng=1
C0
c=1.44p
Ausgang
MN6
"modn"
Vss
wtot=2u
l=1u
ng=1
M1
"modn"
Vss
wtot=10u
l=1u
ng=1
M2
"modn"
Vss
wtot=10u
l=1u
ng=1
Vin-
eingang1
Eingang2
Vin+
M8
"modn"
Vss
wtot=1u
l=1u
ng=1
M5
"modn"
Vss
wtot=1u
l=1u
ng=1
M7
"modn"
Vss
wtot=19u
l=1u
ng=1
net24
net30
net36
net14
Vss

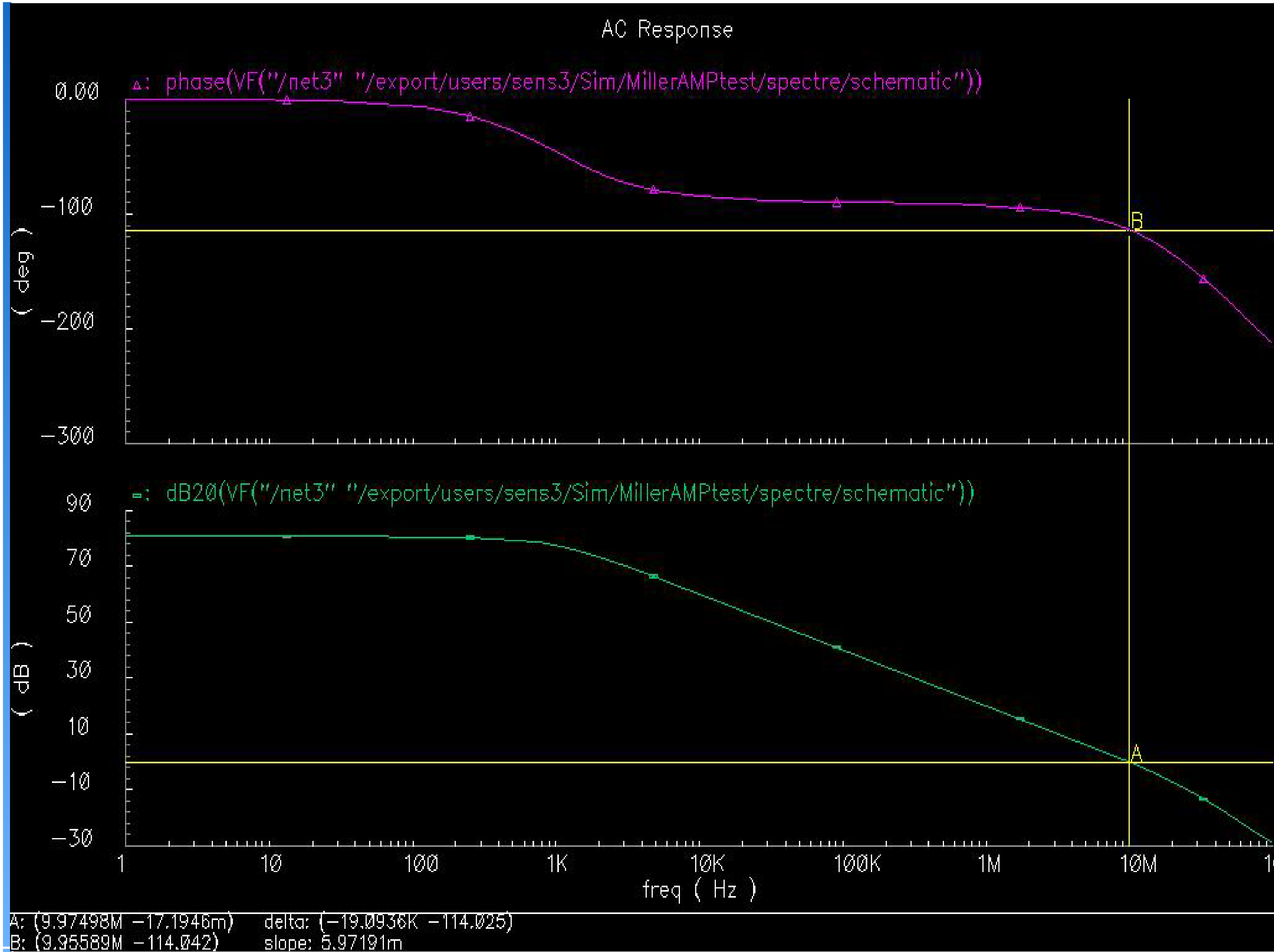
Ganze Schaltung



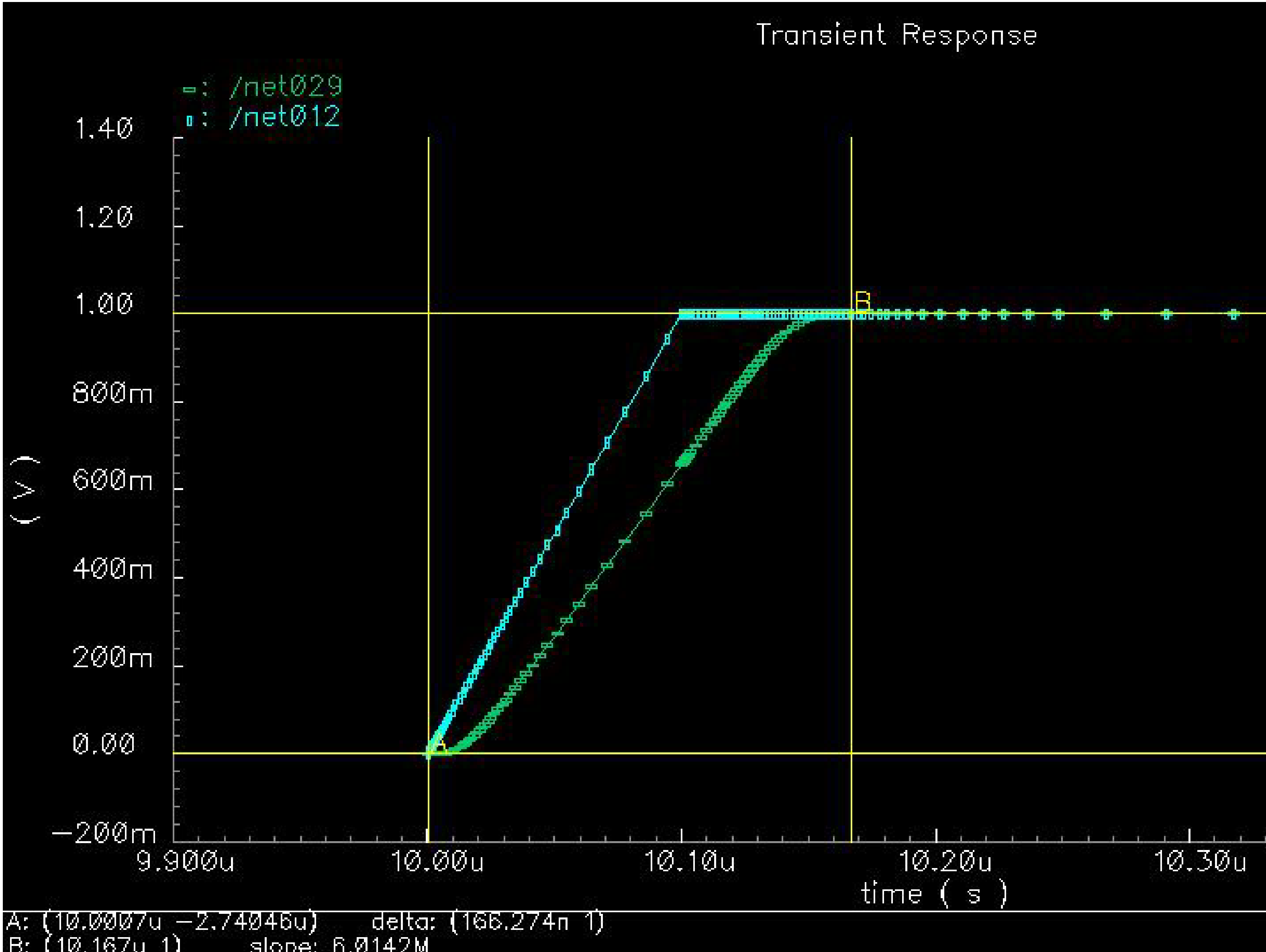
Simulation: Open Loop Gain



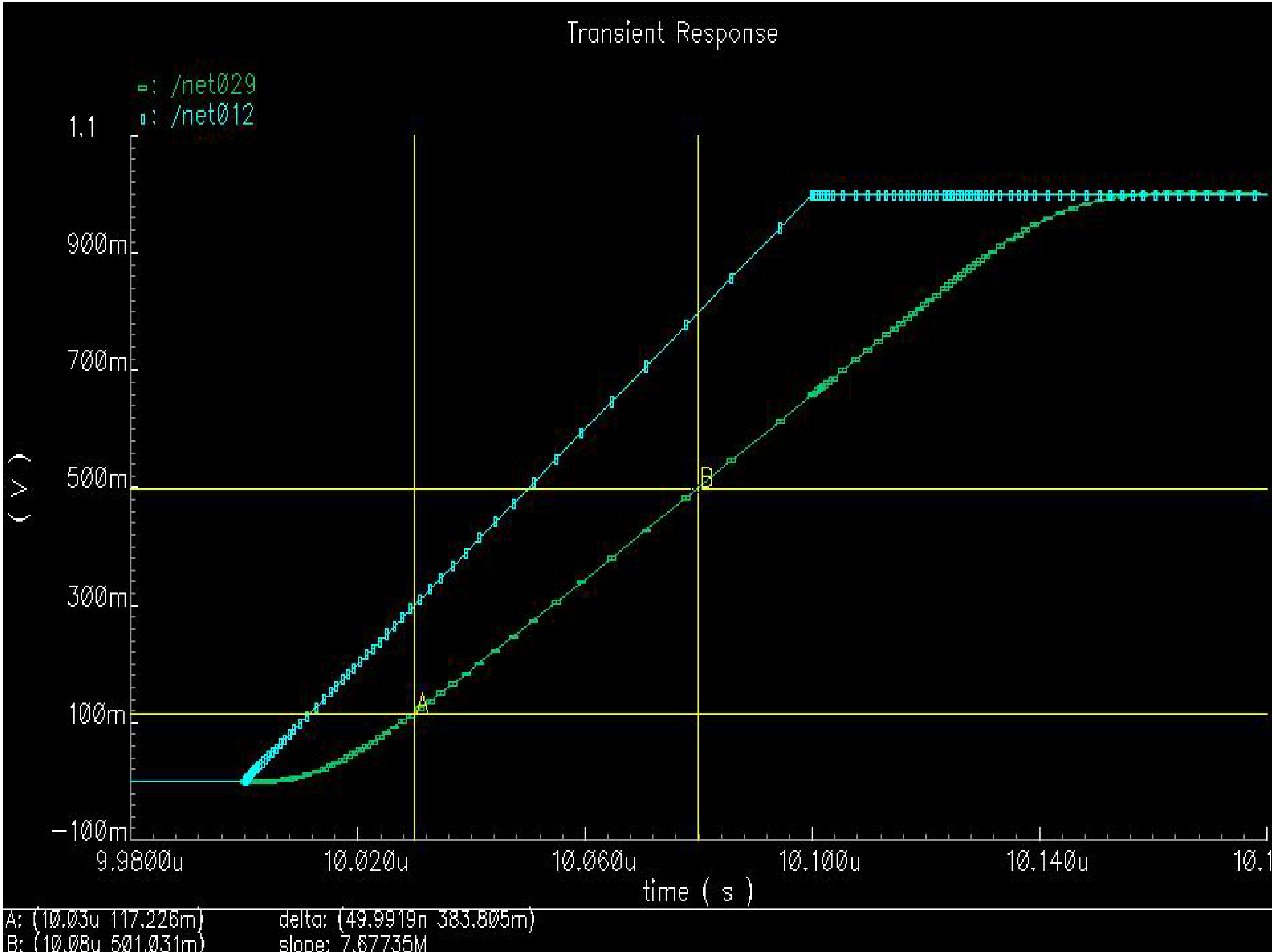
Simulation: Bodeplot



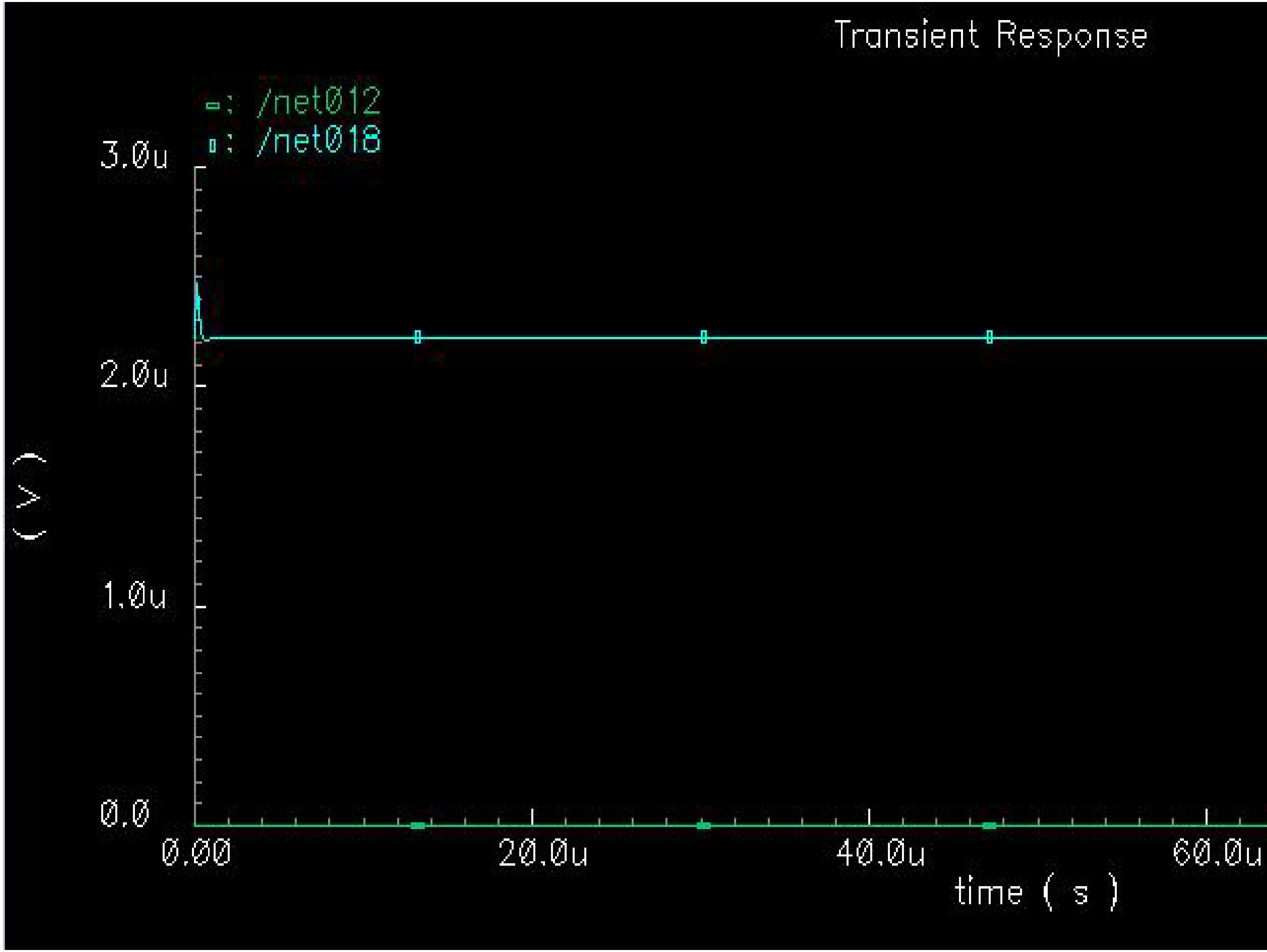
Simulation: Settling Time



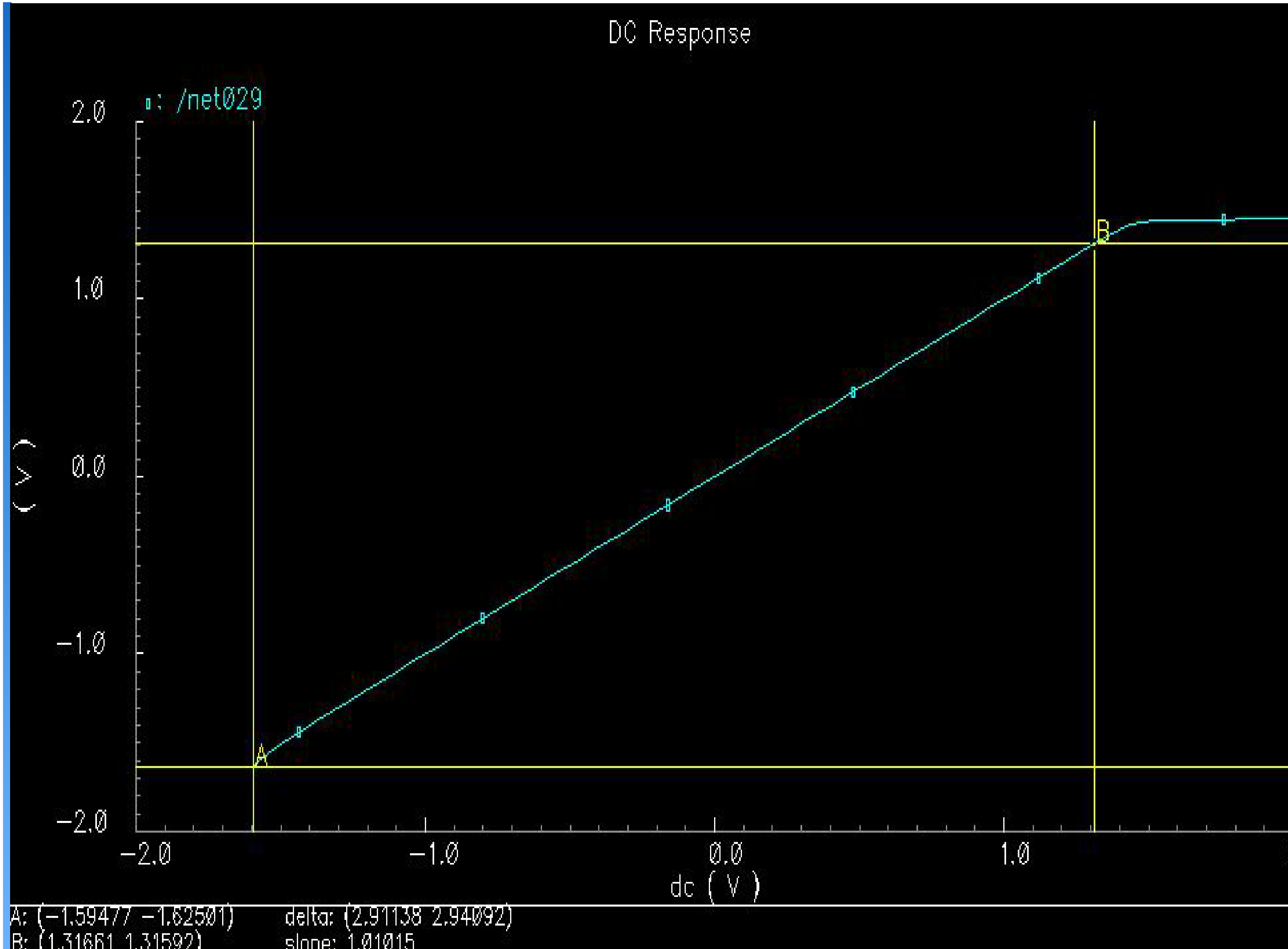
Simulation: Slew Rate



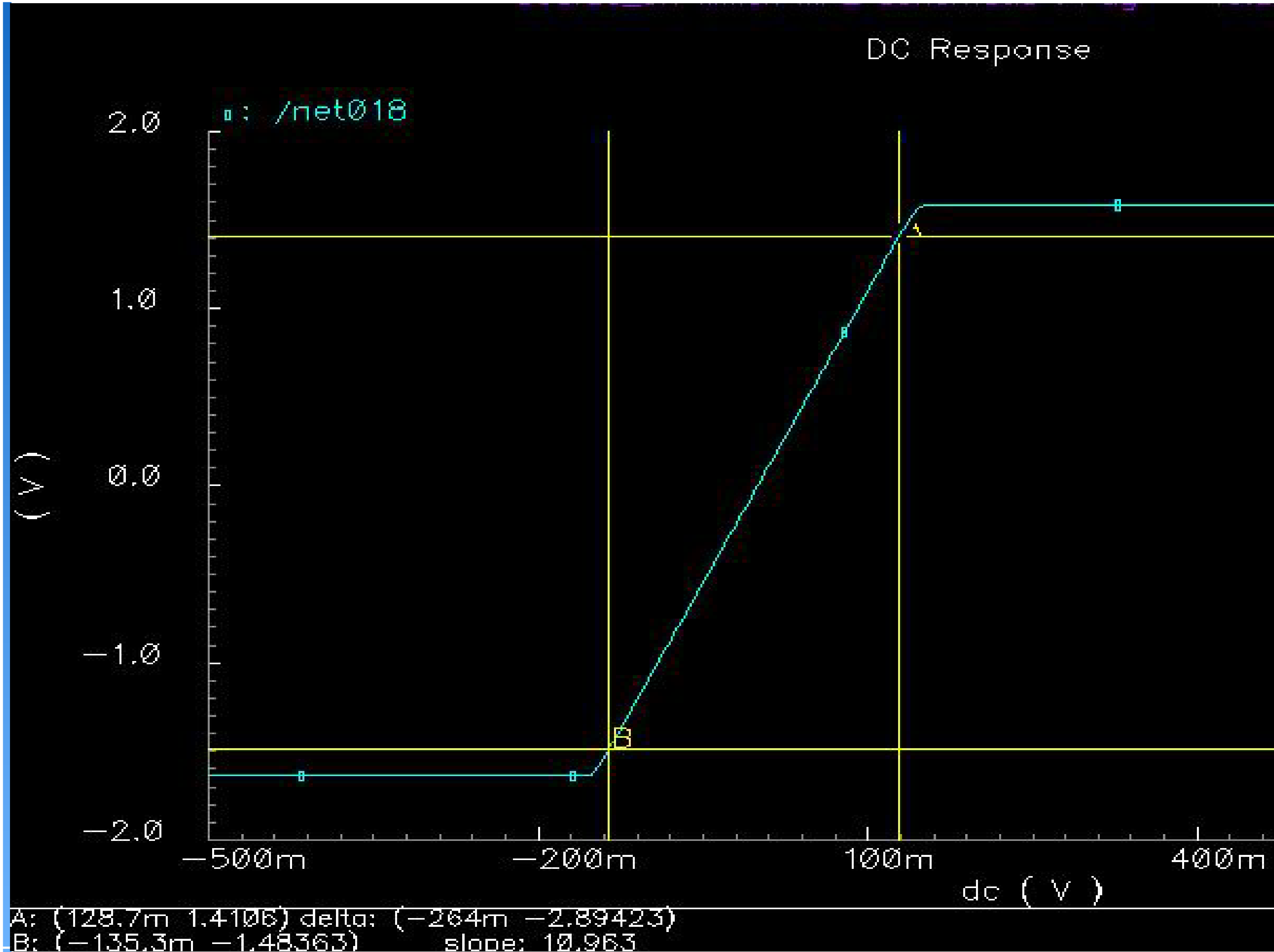
Simulation: Offset



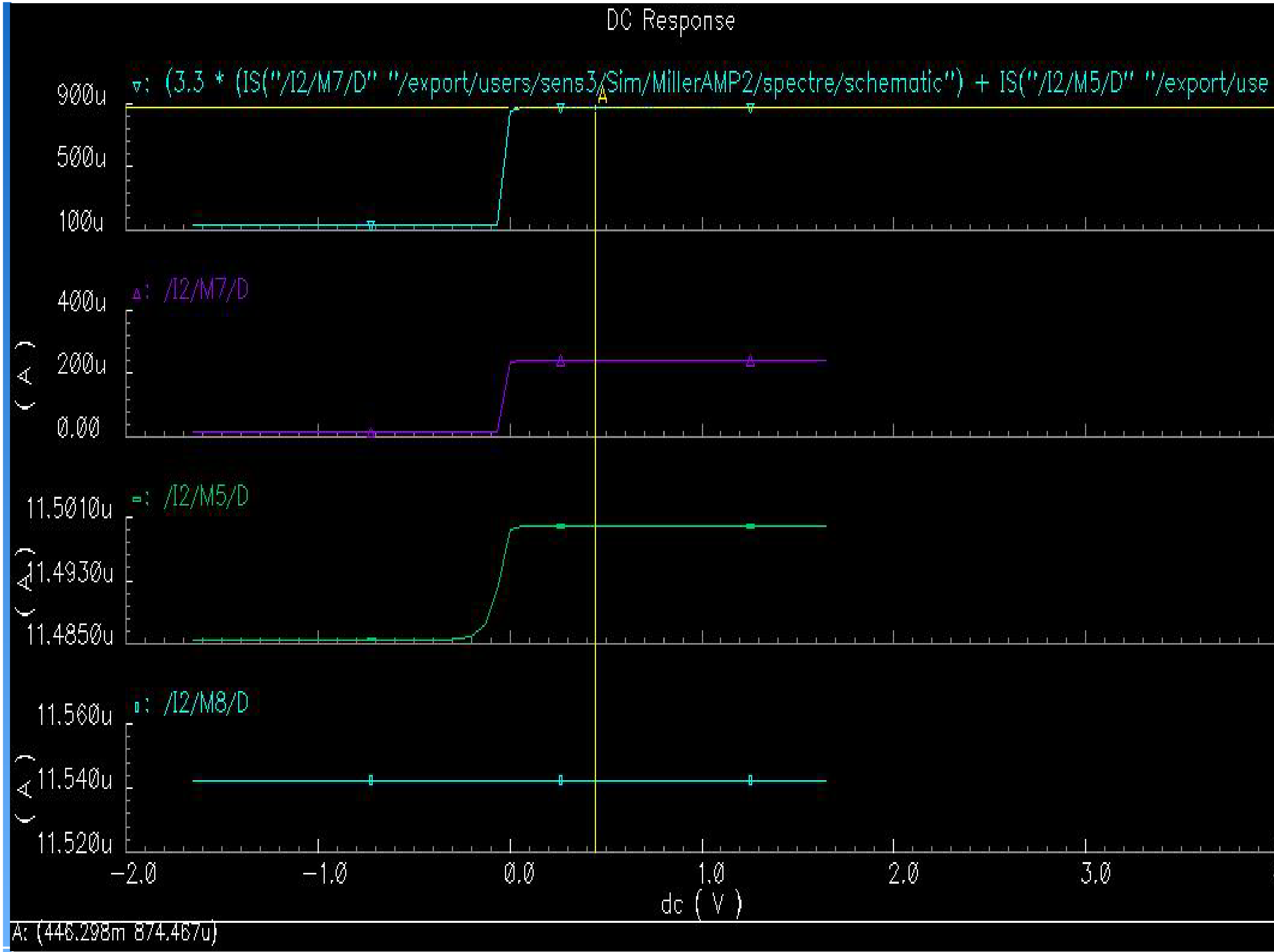
Simulation: ICMR



Simulation: Output Swing



Simulation: Power Dissipation



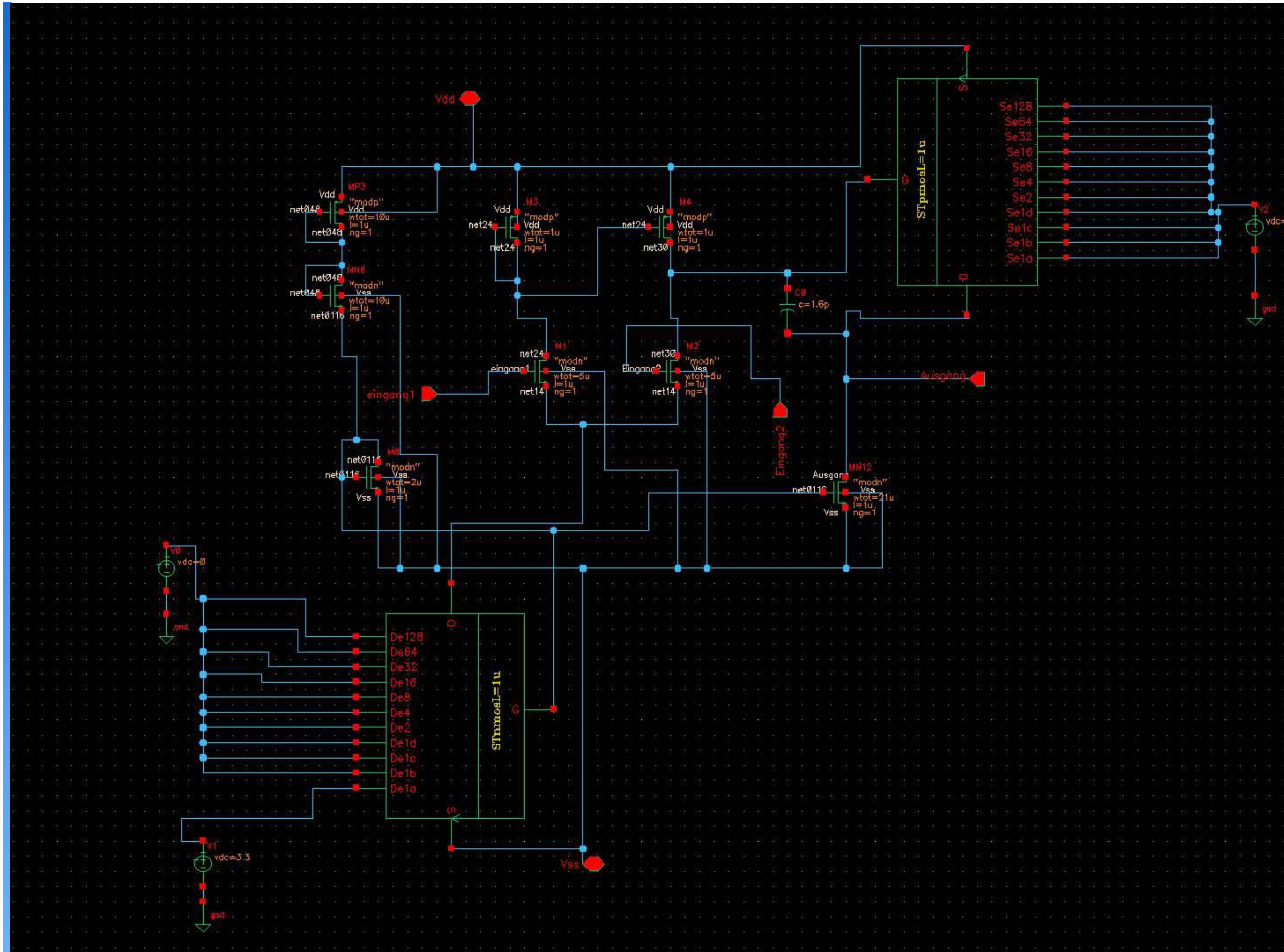
Anpassen der Aspect-Ratio‘s:

Transistorver.	Berechnung	Simulation
W/L_1	1	10
W/L_2	1	10
W/L_3	1	2
W/L_4	1	2
W/L_5	8.8	1
W/L_6	2.73	67
W/L_7	24.0	19

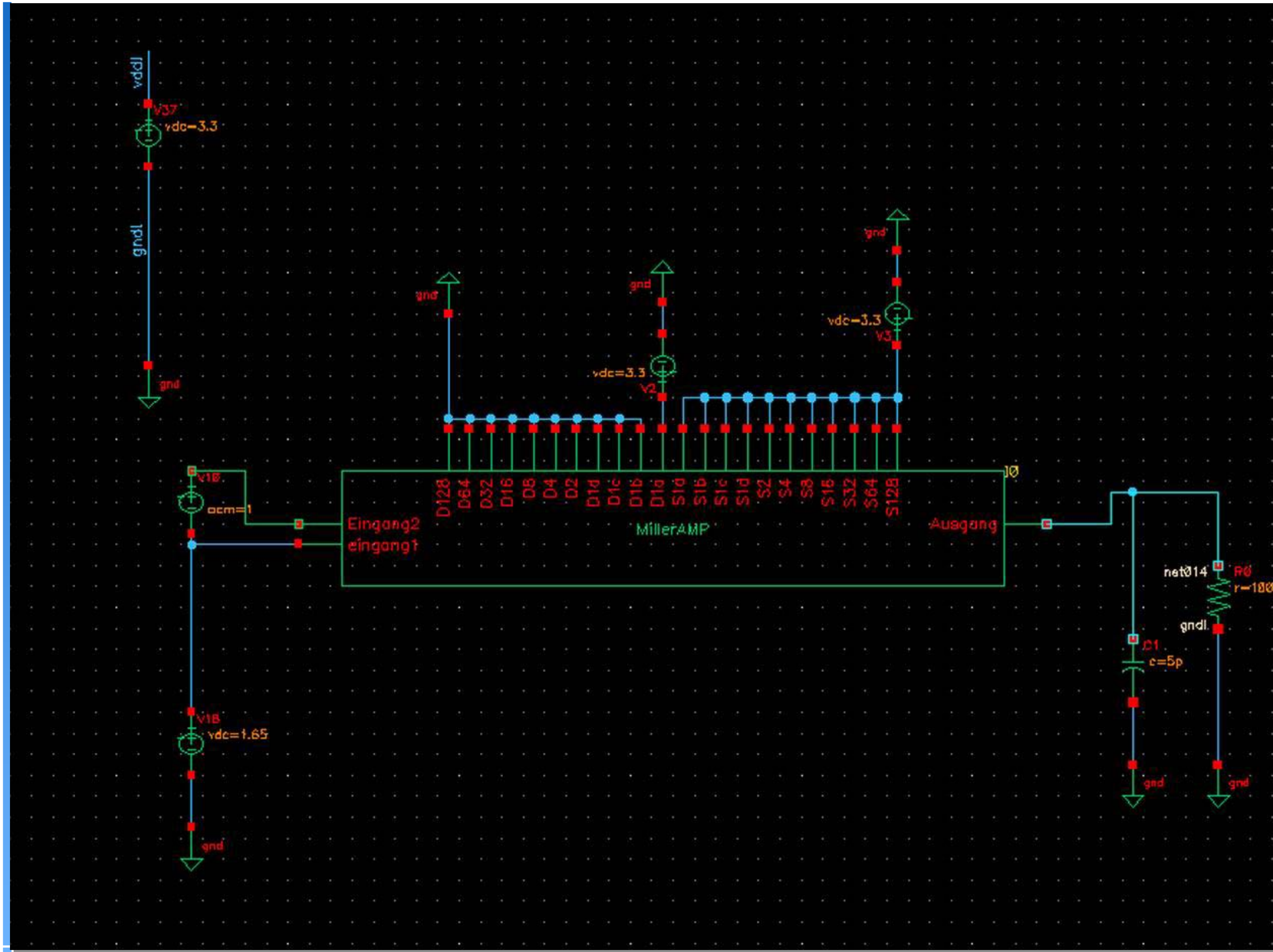
Zusammenfassung der Simulation

	Vorgaben	Simuliert
Open Loop Gain	>80 db	80,74 db
Gain Bandwith	10 MHZ	10 MHZ
Phase Margin	>65°	66°
Settling Time	<1µ s	180n s
Slew Rate	1V/µ s	8 V/µ s
Offset	<<1µ V	2,2µ V
Input CMR	+/- 1 V	+/- 1.3 V
Output Swing	+/- 0,35 V	-1.45/ +1.4
Power Dissipation	<1m W	874µ W

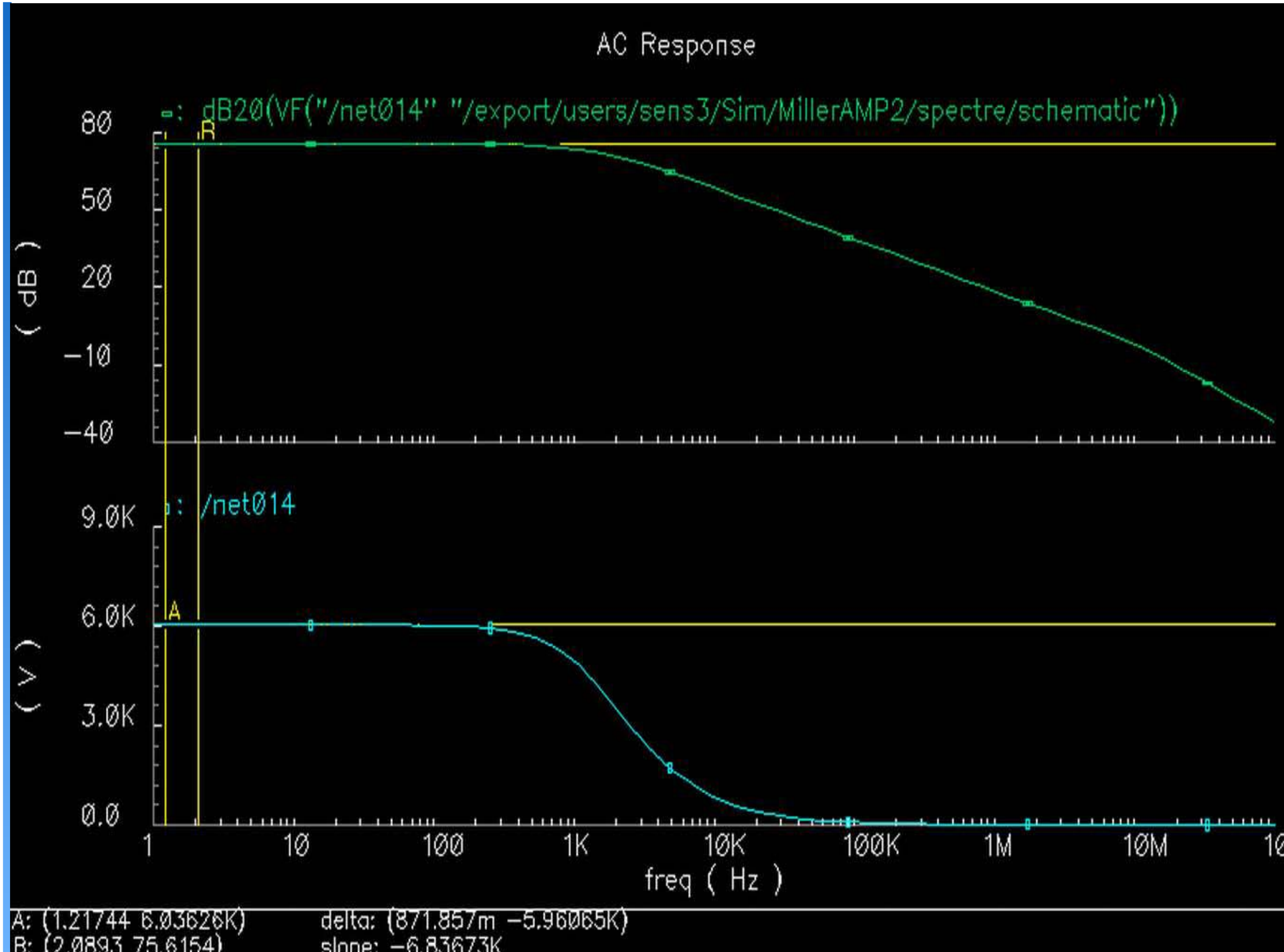
Einführen der Scaleable Devices



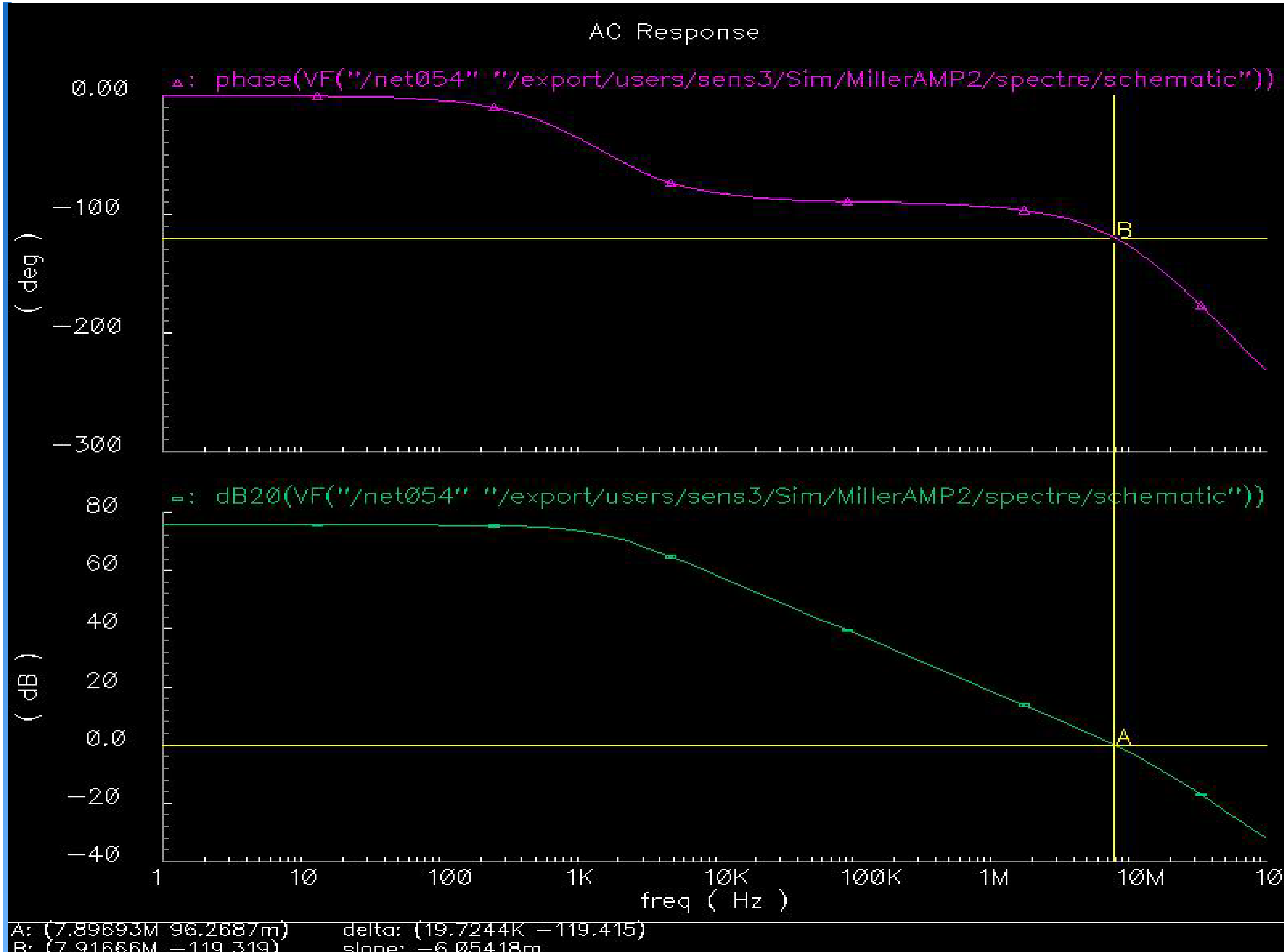
Ganze Schaltung



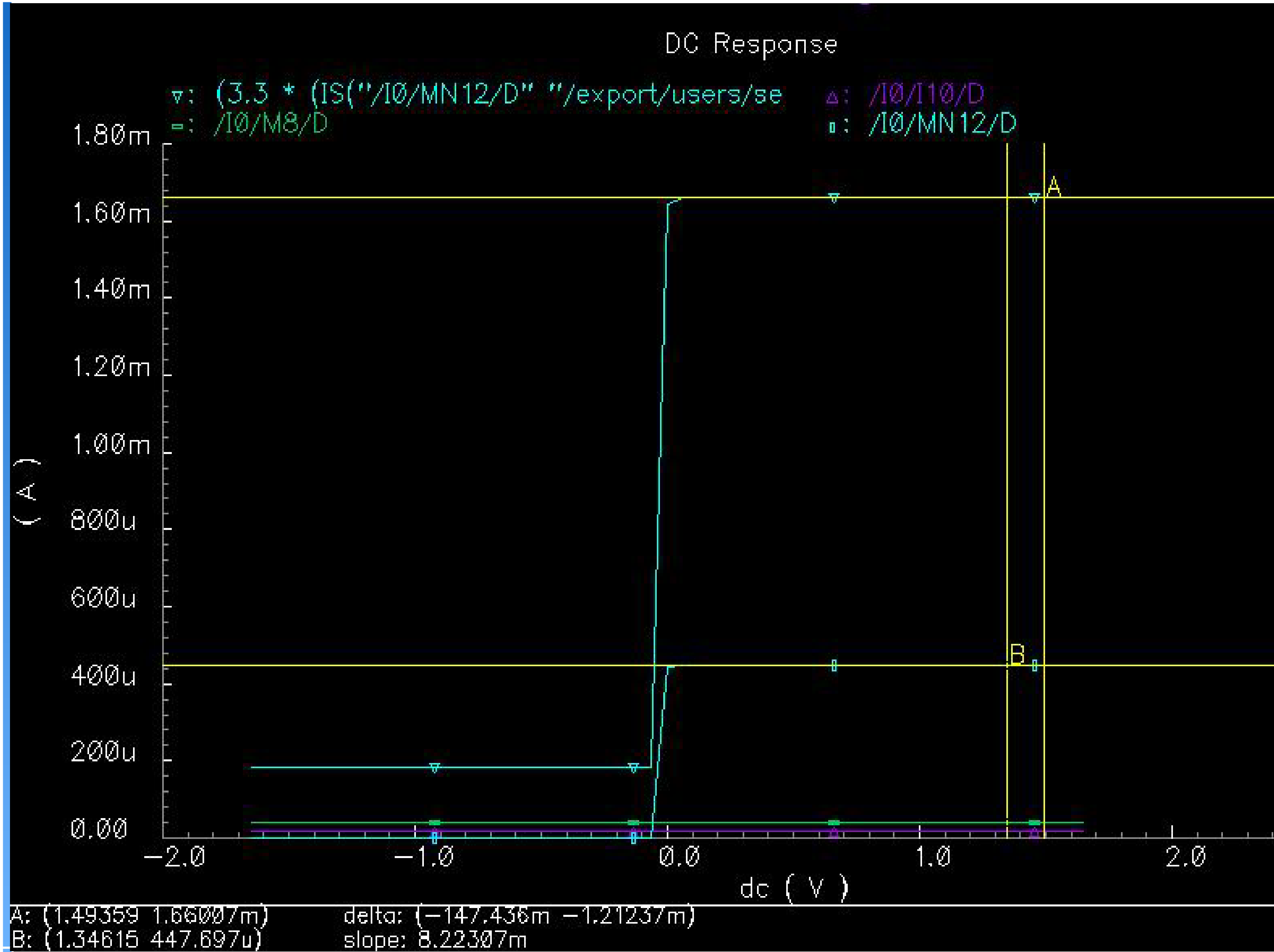
Simulation: Gain



Simulation: Bodeplot



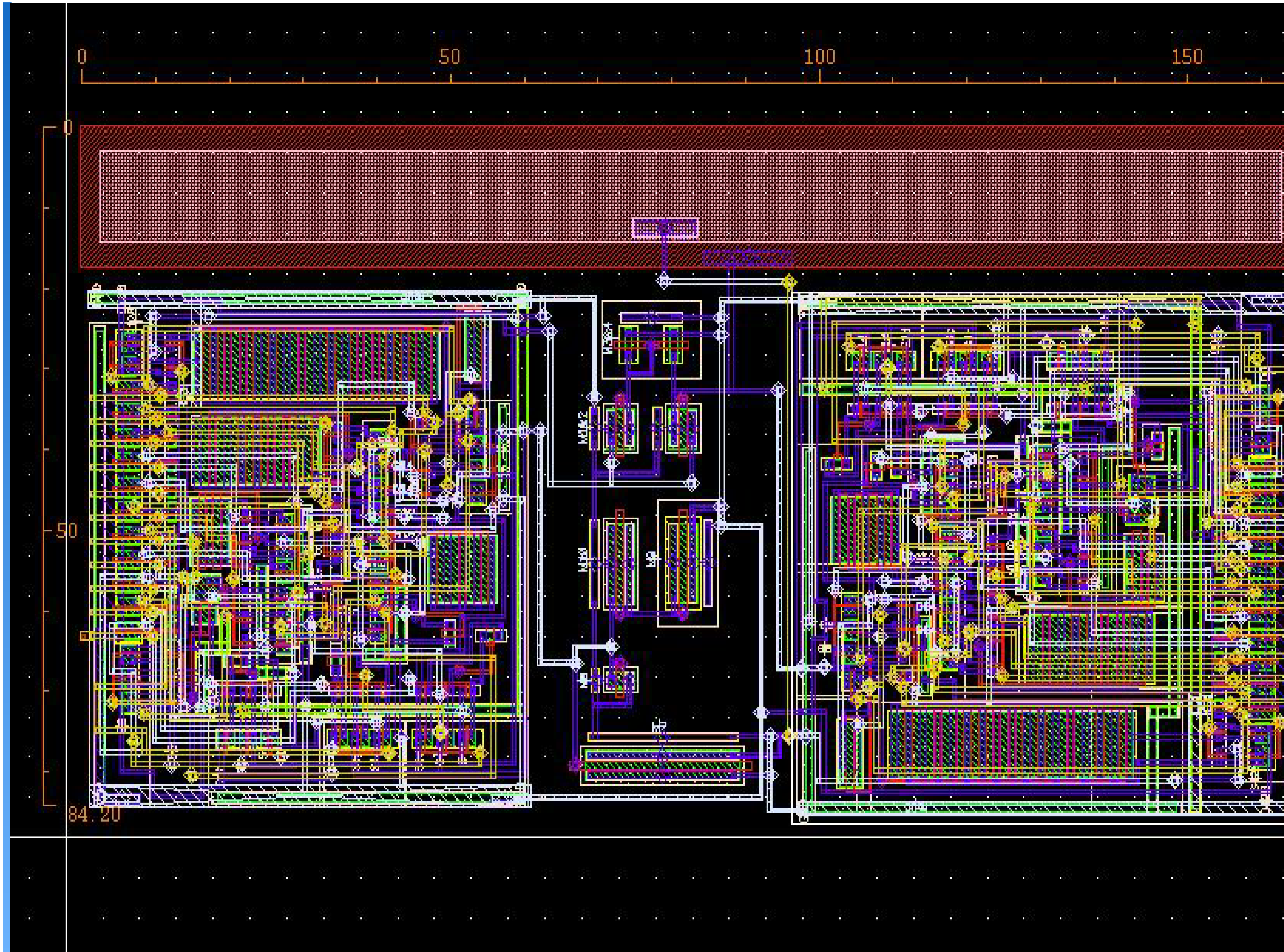
Simulation: Power dissipation



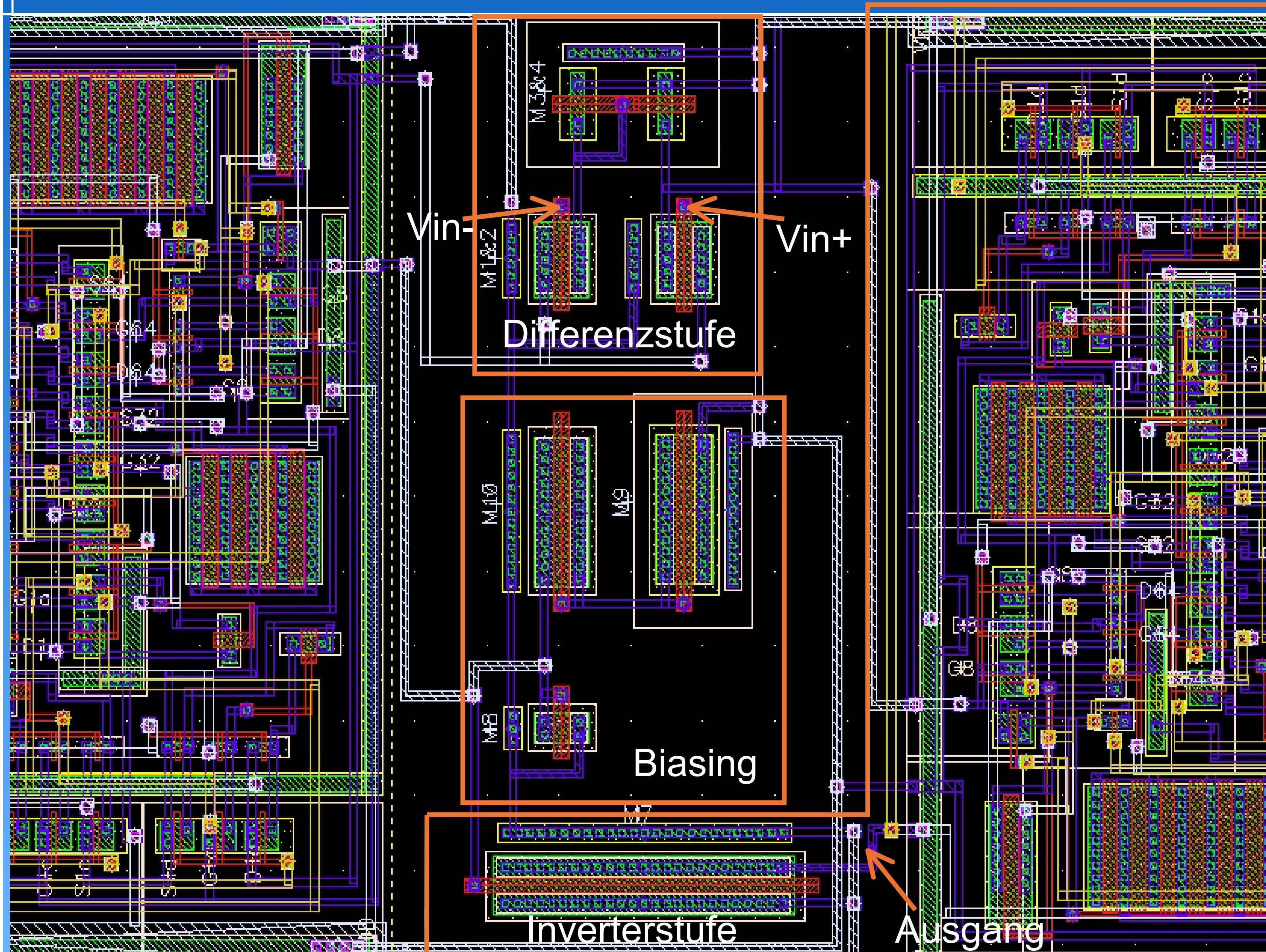
Zusammenfassung

	Vorgaben	Simuliert	Scaleable Dev.
Open Loop Gain	>80 db	80,74 db	75,6 db
Gain Bandwith	10 MHz	10 MHz	8 MHz
Phase Margin	>65°	66°	61,5°
Settling Time	<1µ s	180n s	180n s
Slew Rate	1V/µ s	8 V/µ s	5 V/µ s
Offset	<<1µ V	2,2µ V	1,47µ V
Input CMR	+/- 1 V	+/- 1.3 V	-1.45 V/+0.9 V
Output Swing	+/- 0,35 V	-1.45/ +1.4	-1.5 V/+1 V
Power Dissipation	<1m W	874µ W	1.67m W

Post Layout Simulation



Transistorpositionen



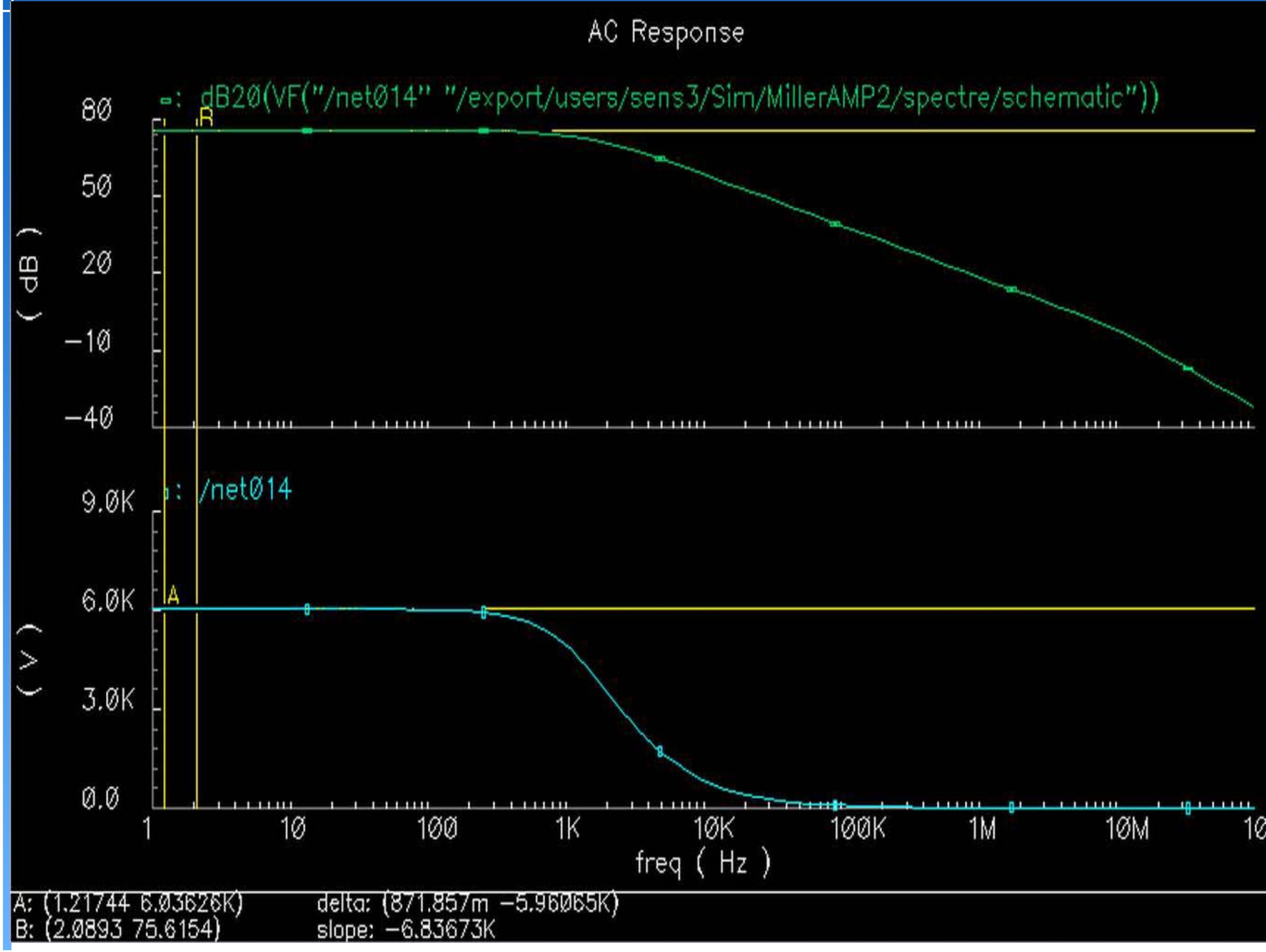
LVS Check

The net-lists match.

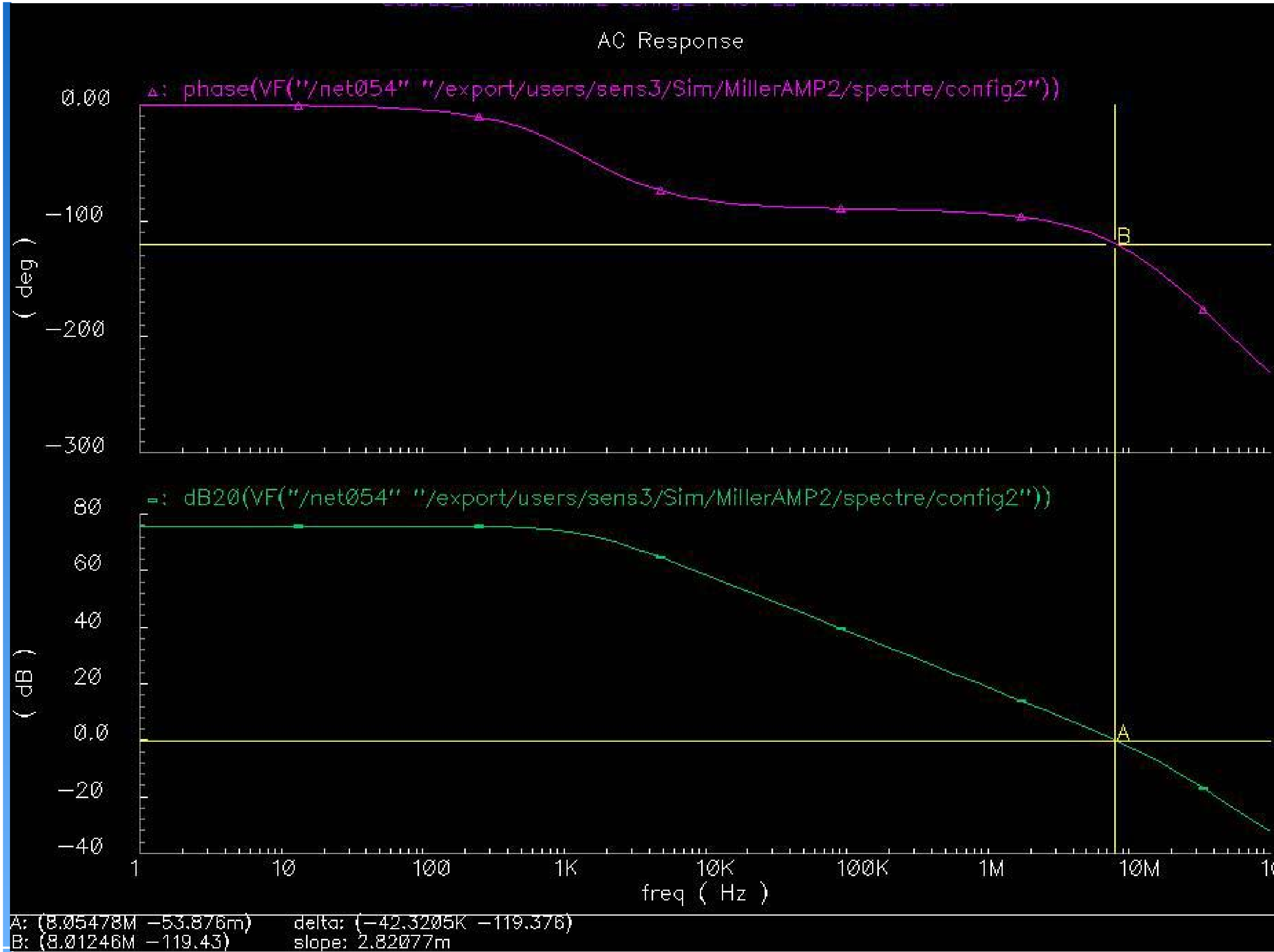
	layout	schematic
instances		
un-matched	0	0
rewired	0	0
size errors	0	0
pruned	0	0
active	259	207
total	259	207
nets		
un-matched	0	0
merged	0	0
pruned	0	0
active	100	100
total	100	100
terminals		
un-matched	0	0
matched but different type	0	0
total	27	27

Comparison program completed successfully.

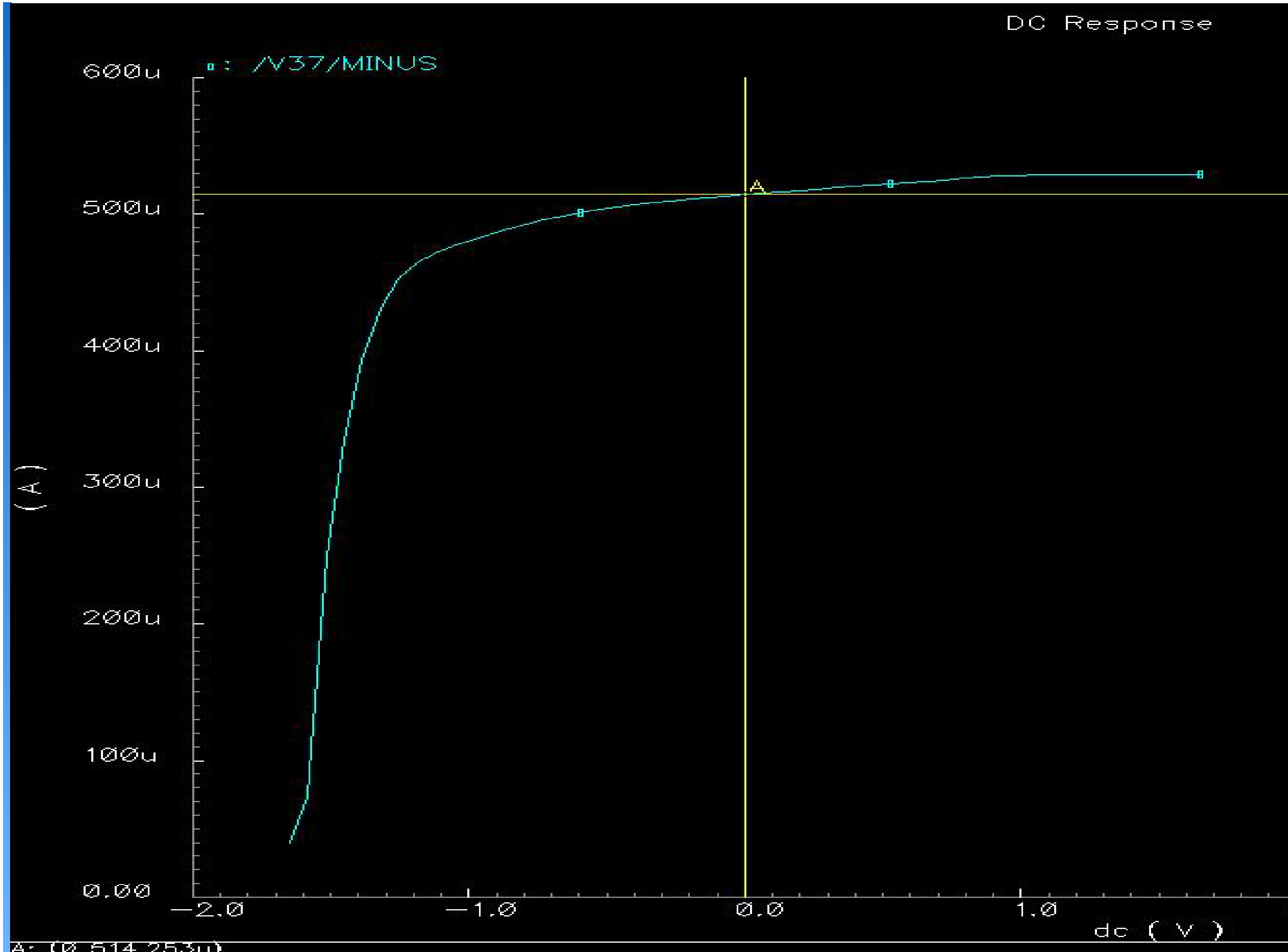
Simulation: Gain



Simulaton: Bodeplot



Simulation: Power Dissipation



Zusammenfassung

	Vorgaben	Simuliert	Scaleable Dev.	Ana. Extracted
Open Loop Gain	>80 db	80,74 db	75,6 db	75,6 db
Gain Bandwith	10 MHz	10 MHz	8 MHz	8 MHz
Phase Margin	>65°	66°	61,5°	61,5°
Settling Time	<1µ s	180n s	180n s	180n s
Slew Rate	1V/µ s	8 V/µ s	5 V/µ s	5 V/µ s
Offset	<<1µ V	2,2µ V	1,47µ V	1,47µ V
Input CMR	+/- 1 V	+/- 1.3 V	-1.45 V/+0.9 V	-1.45 V/+0.9 V
Output Swing	+/- 0.35 V	-1.45/ +1.4	-1.5 V/+1 V	-1.5 V/+1 V
Power Dissipation	<1m W	874µ W	1.67m W	1.7m W

Formelanhang

$$SR = \frac{I_5}{C_c}$$

$$GB = \frac{g_{m1}}{C_c}$$

$$V_{in}(\max) = V_{DD} - \sqrt{\frac{I_5}{\beta_3}} - |V_{T03}|(\max) + V_{T1}(\min)$$

$$V_{in}(\min) = V_{ss} + \sqrt{\frac{I_5}{\beta_1}} + V_{T1}(\max) + V_{DS5}(sat)$$

$$V_{DS}(sat) = \sqrt{\frac{2I_{DS}}{\beta}}$$

Formelanhang

$$g_{m1} = GB \cdot C_c$$

$$V_{DS5} = V_{in}(\min) - V_{SS} - \sqrt{\frac{I_5}{\beta_1}} - V_{T1}(\max)$$

$$g_{m6} = 2.857 \cdot g_{m2} \cdot \frac{C_L}{C_C}$$

$$I_6 = \frac{(g_{m6})^2}{2K_6S_6}$$

$$A_v = \frac{2 g_{m2} g_{m6}}{I_5(\lambda_2 + \lambda_4) \cdot I_6(\lambda_6 + \lambda_7)}$$

$$P_{diss} = (I_5 + I_6)(V_{DD} + |V_{SS}|)$$