Design of Active Pixel Cell using PMOS source follower

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PROJECT

Individual Task

To design an APS with PMOS source follower instead of an NMOS source follower.

Global Task

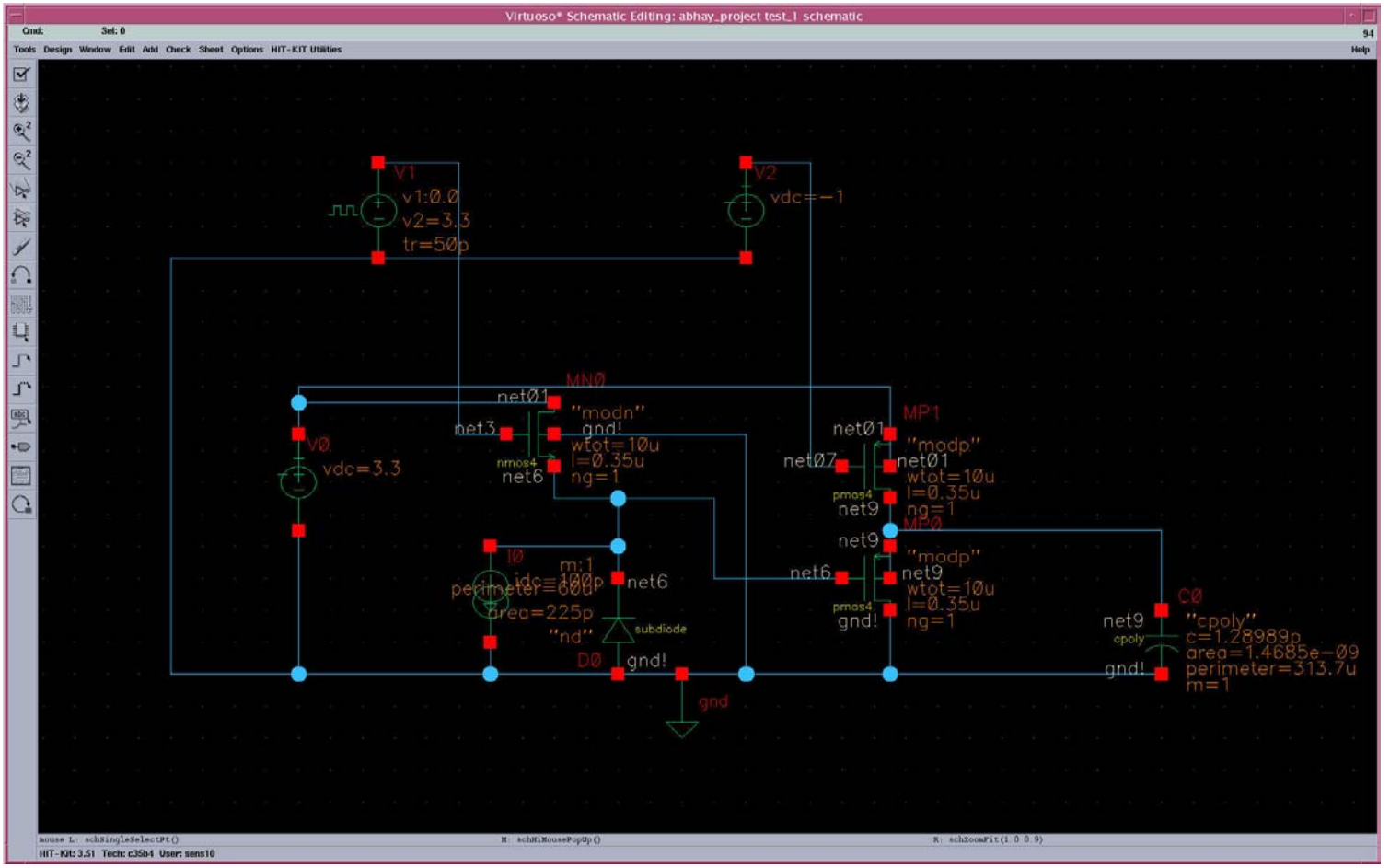
To design global decoder (4 bit decoder)

APS with PMOS source follower

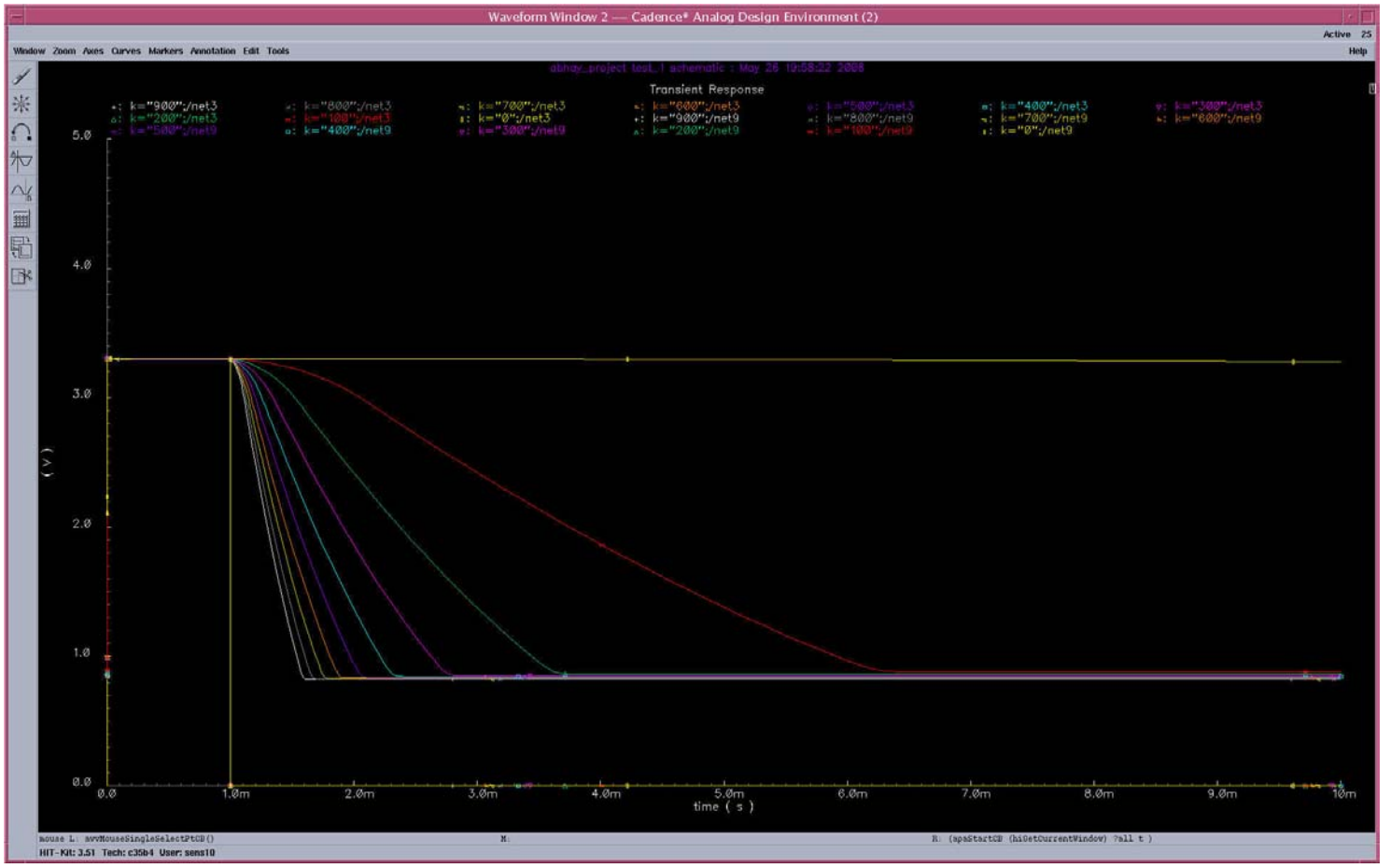
In order to design an active pixel cell with PMOS source follower instead of an NMOS source follower , the basic APS cell without the shutter or row-select switches was first taken and simulated .

A capacitive load of 1.3 pf is used while designing the single pixel cell.

APS with PMOS source follower

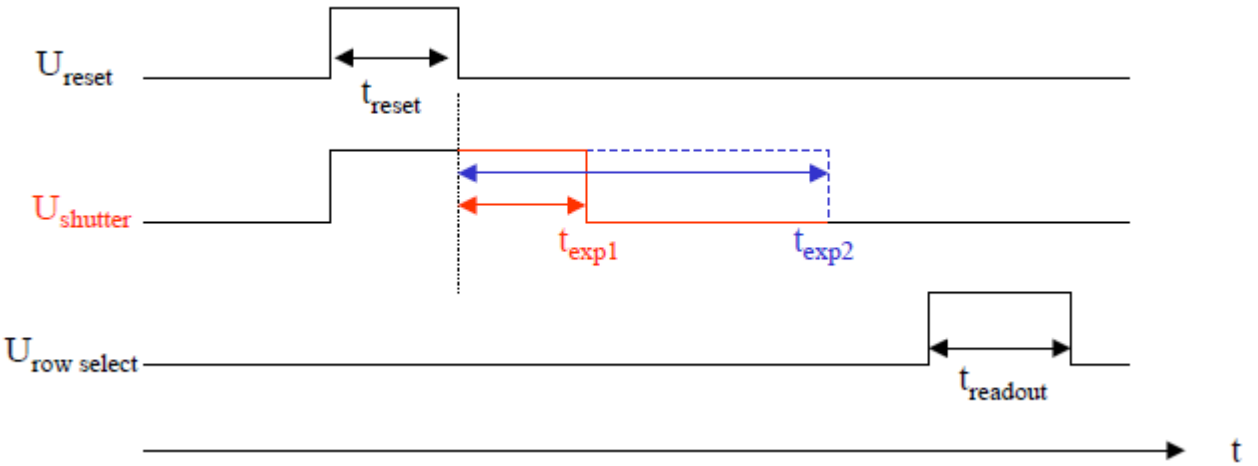


Parametric simulation

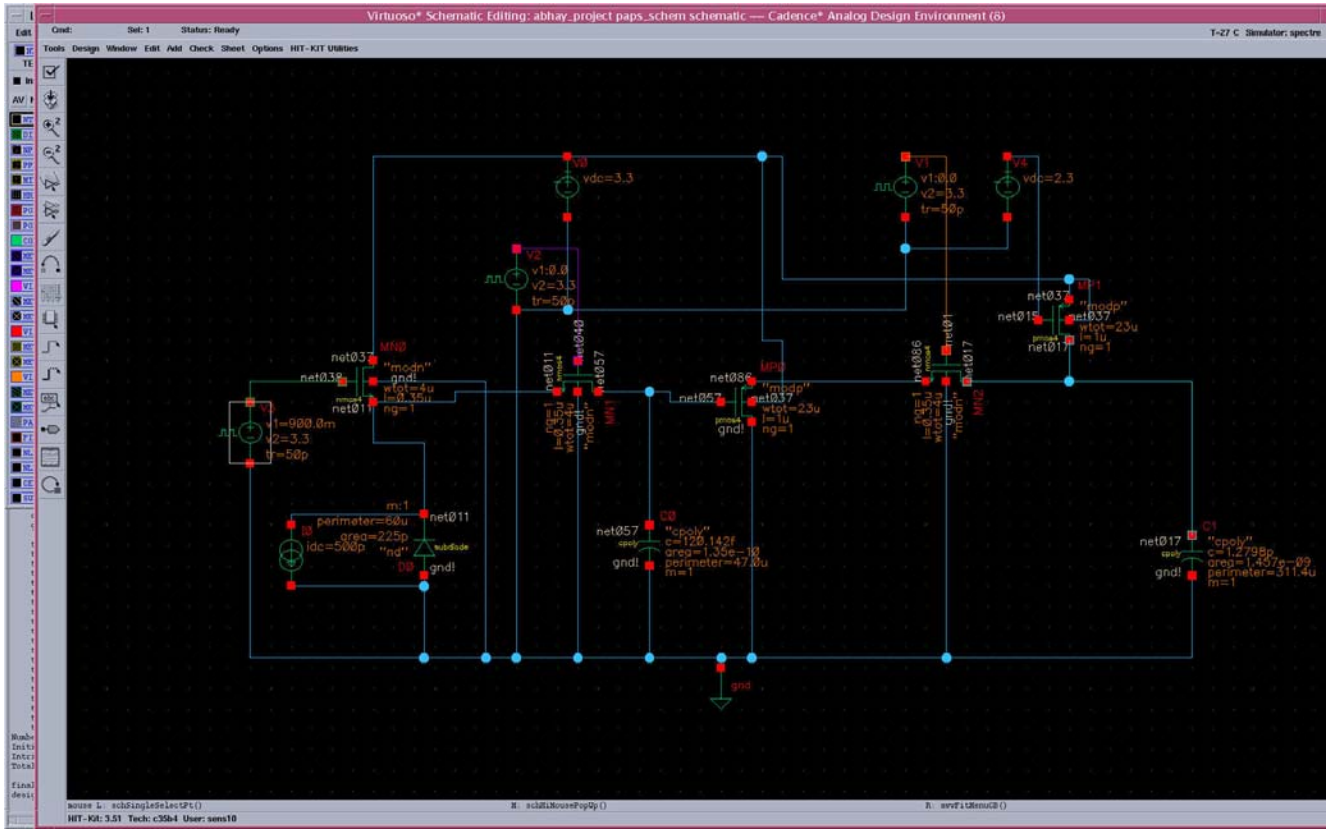


APS with Shutter and Row-select

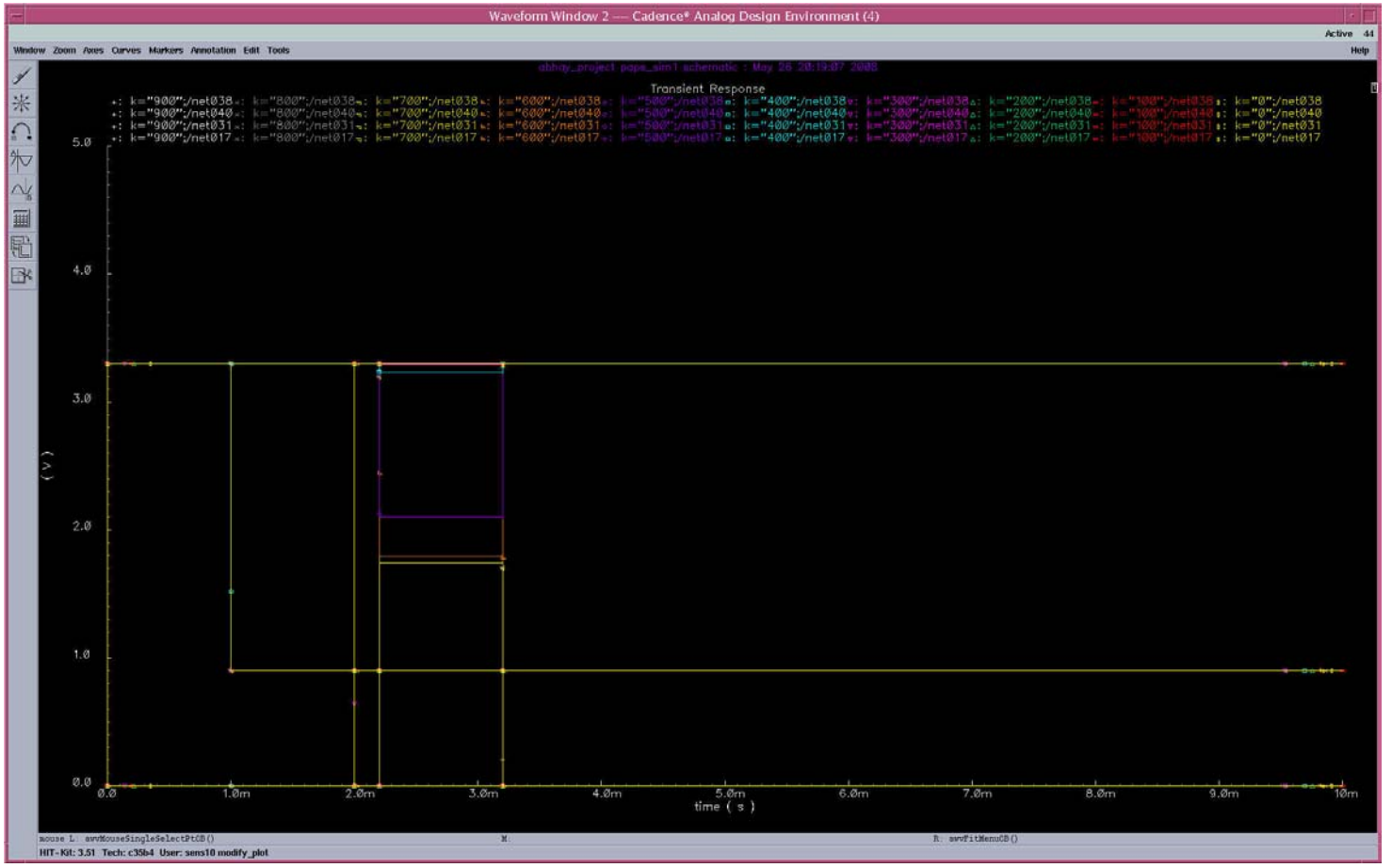
APS was then simulated with the row select and the electronic shutter. The electronic shutter is used to freeze the read-out in ´time, similar to a mechanical shutter. Row-select gives us the freedom to select one pixel at a time for a serial read-out.



APS with Shutter and Row-select



Parametric analysis

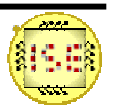


Reset Voltage

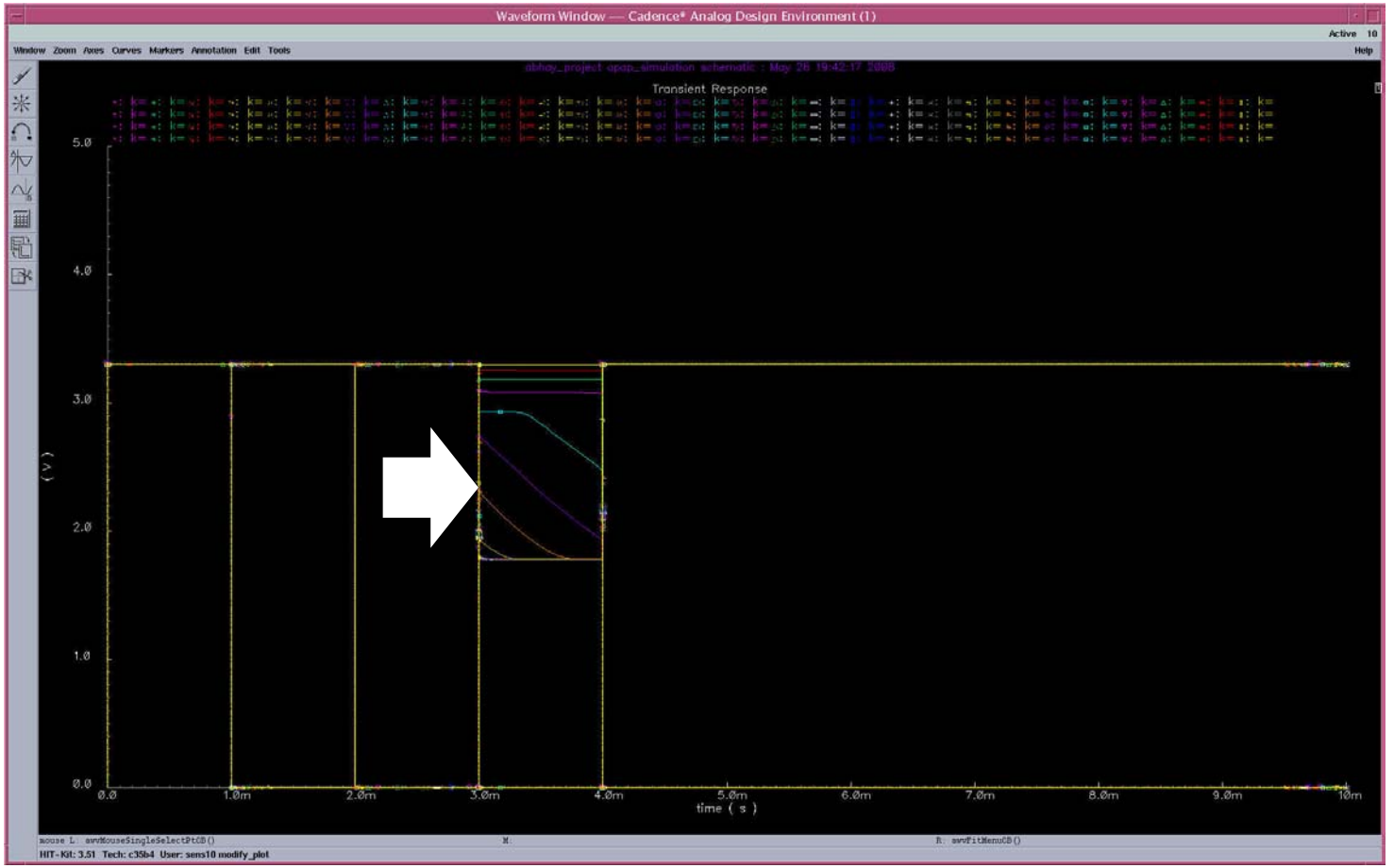
It was found that Reset voltage plays an important role when using a PMOS source follower .

If the lower voltage is set to zero the photo diode becomes forward biased because of its internal capacitance .

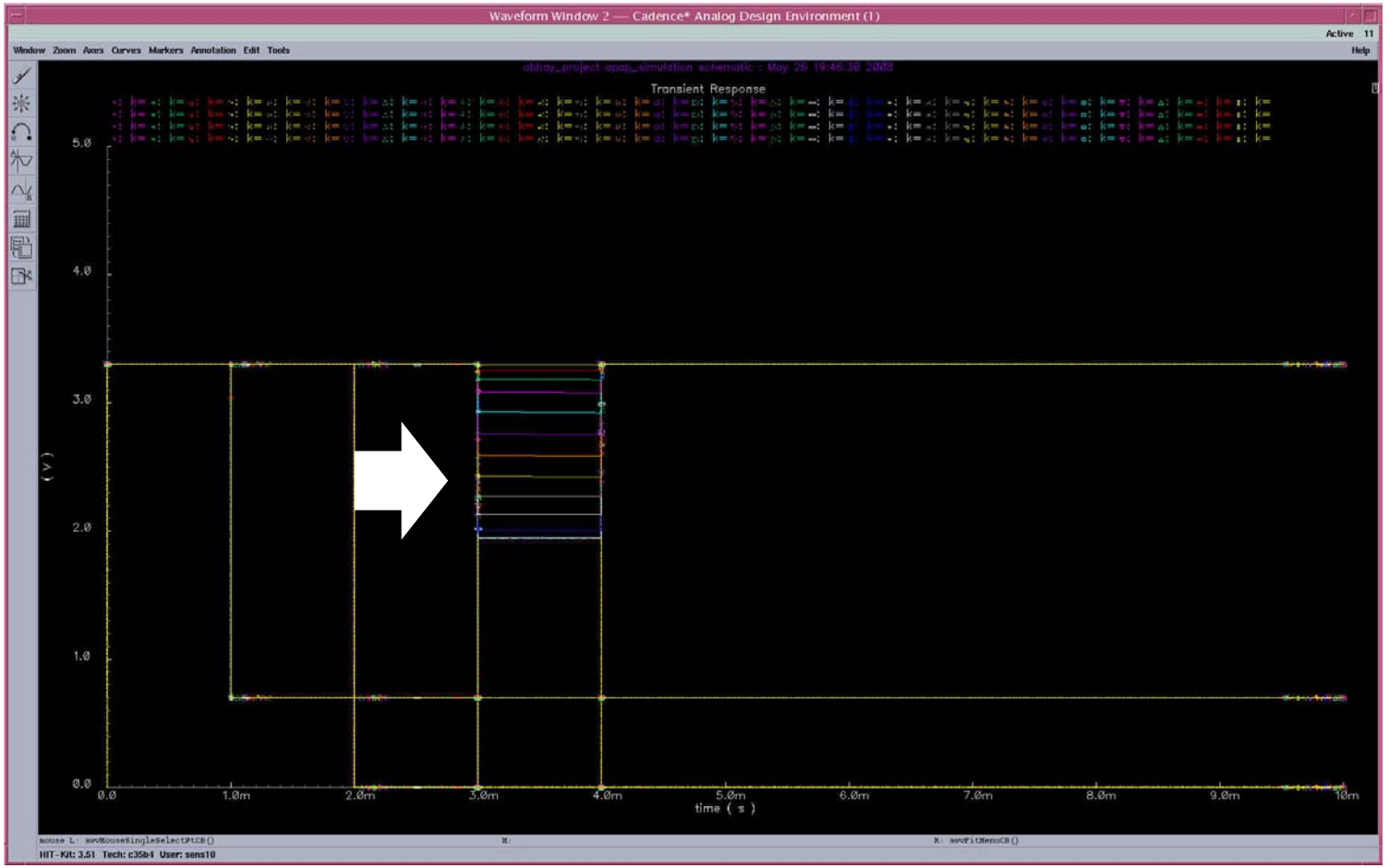
So the lower voltage should be at least set to the threshold voltage of the diode to prevent it from getting forward biased.



Reset Voltage with lower voltage as 0



Reset Voltage with lower voltage as .7V



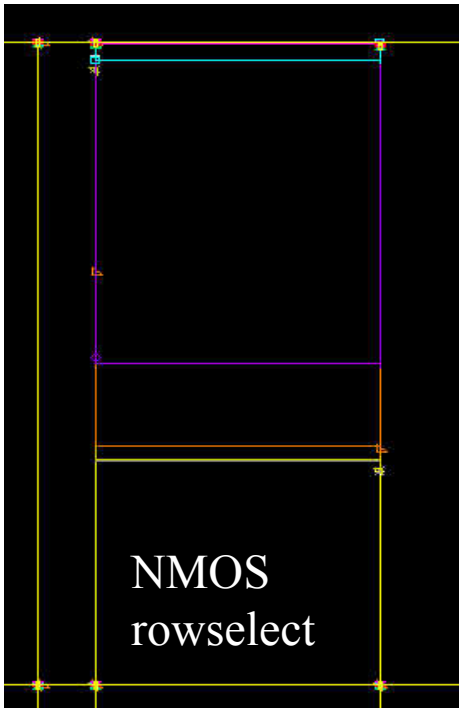
PMOS or NMOS Row-Select Switch

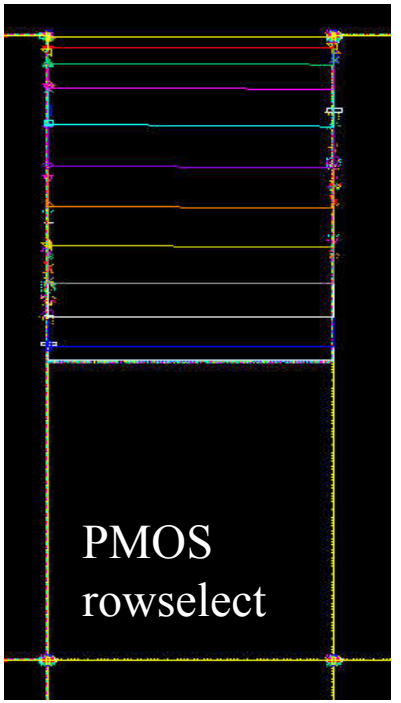
While designing , It was found that making use of an NMOS row-select switch did not give good results , While PMOS switch gives better results.

Using PMOS switch does not reduce the fill factor as it could be placed in the same n-well as the source follower, though this would reduce the advantage of the bulk effect.

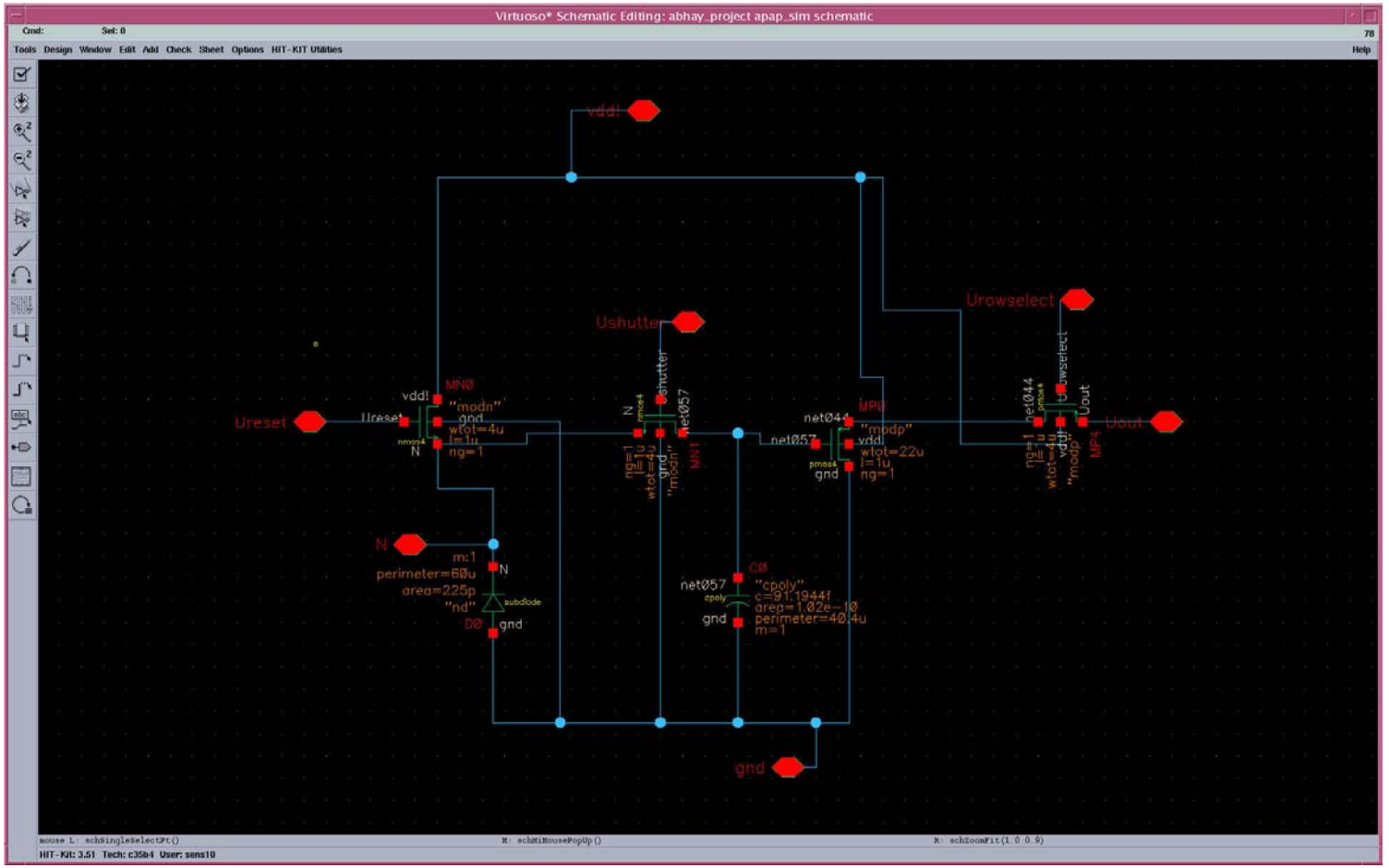
PMOS or NMOS Row-Select Switch

A parametric analysis with a sweep of current I from 100 pA to 900 pA in 10 steps is shown below for PMOS and NMOS row-select with same parameters for all devices in the circuit.





APS Schematic



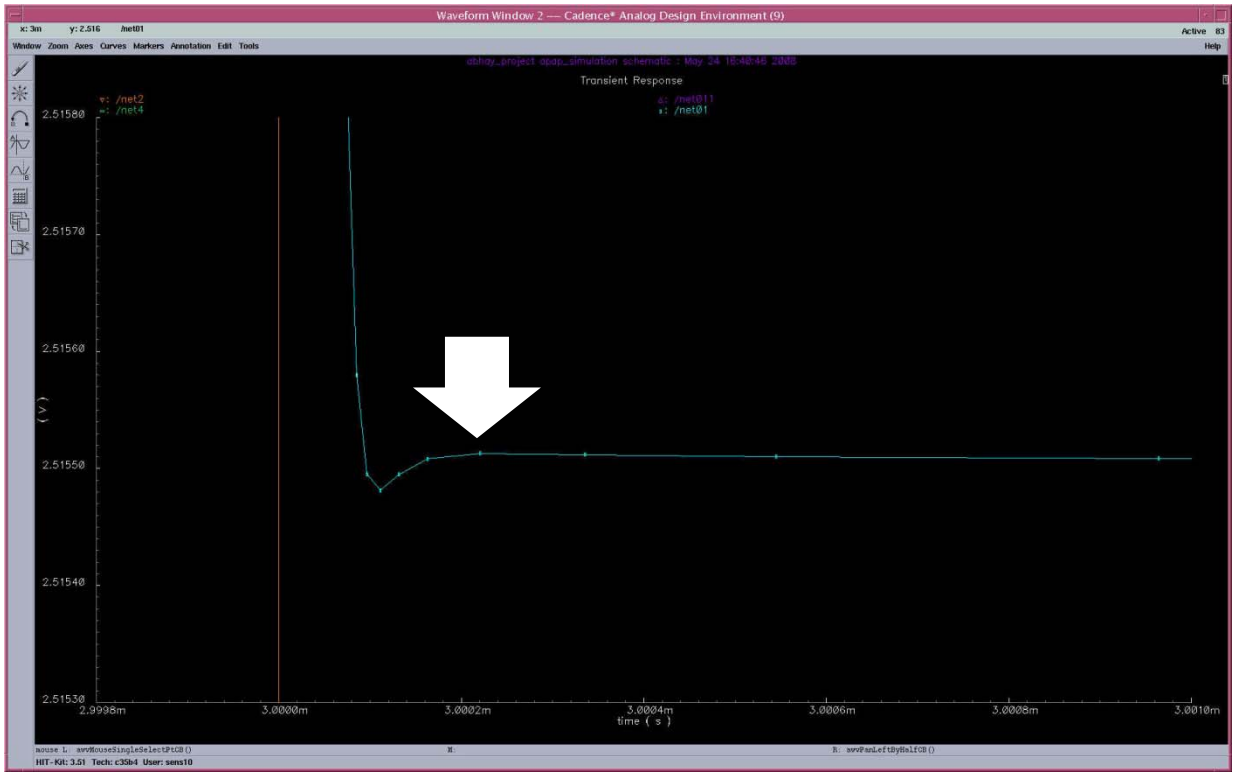
Parameter Selection

After simulating for various sizes the most effective combination of parameters was found . The parameters are listed below

Component	Width(microns)	Length(microns)
Reset Switch	4	1
Shutter switch	4	1
Row Select switch	4	1
Capacitor	Area = 93 sq micron	
Photo Diode	15	15
Source Follower	22	1
Bias Voltage	2.3 V	

Read out time

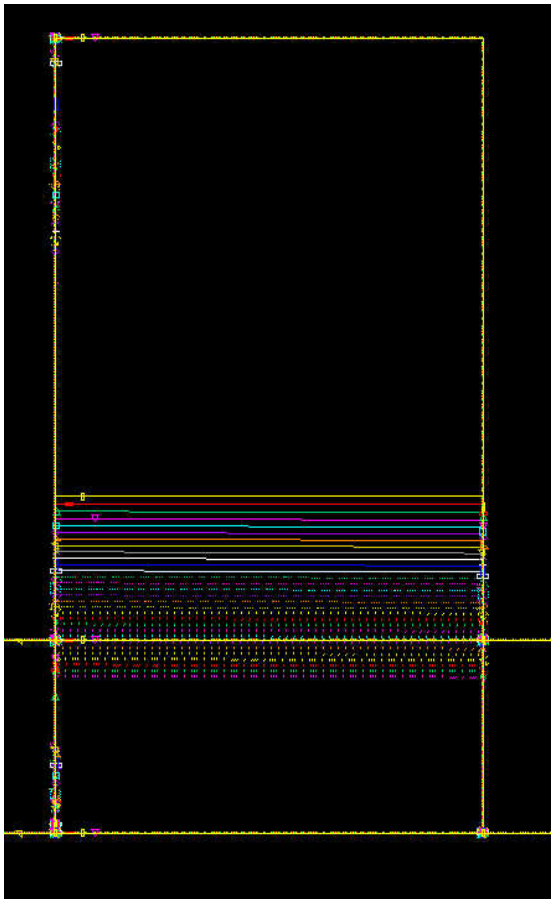
The read out time for the above parameters was found to be 100 nanoseconds



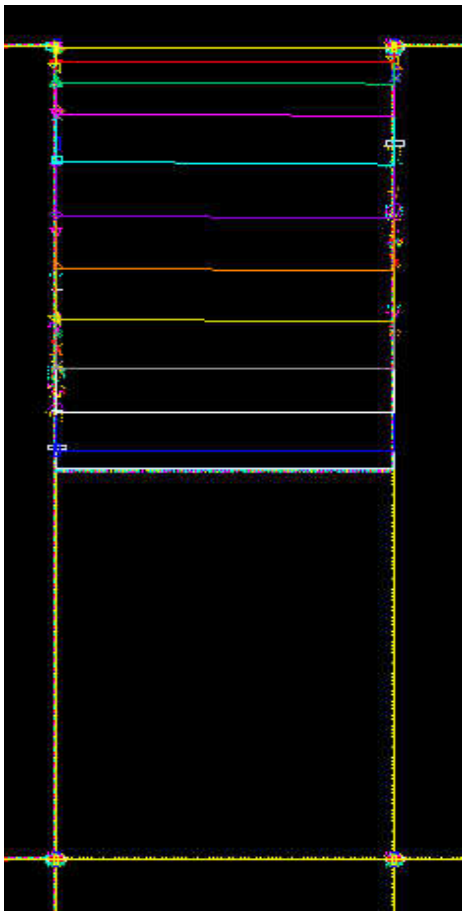
Comparison between NMOS and PMOS source follower

1) PMOS source follower has a better dynamic range than NMOS
2) PMOS occupies more area than NMOS because of the use of N-well for PMOS.
3) The body effect coefficient of PMOS is less than the NMOS , Hence PMOS has reduced bulk effect.

Dynamic Range



A parametric Analysis over a range of 0 pA current to 1800 pA was taken and We can see that the dynamic range for PMOS (right) is more than the dynamic range using an NMOD (left) source follower



LAYOUT

1)The Layout was designed in Cadence using 0.35 micrometer technology.

2) The area of the APS single cell was found to be 31 microns * 30 microns

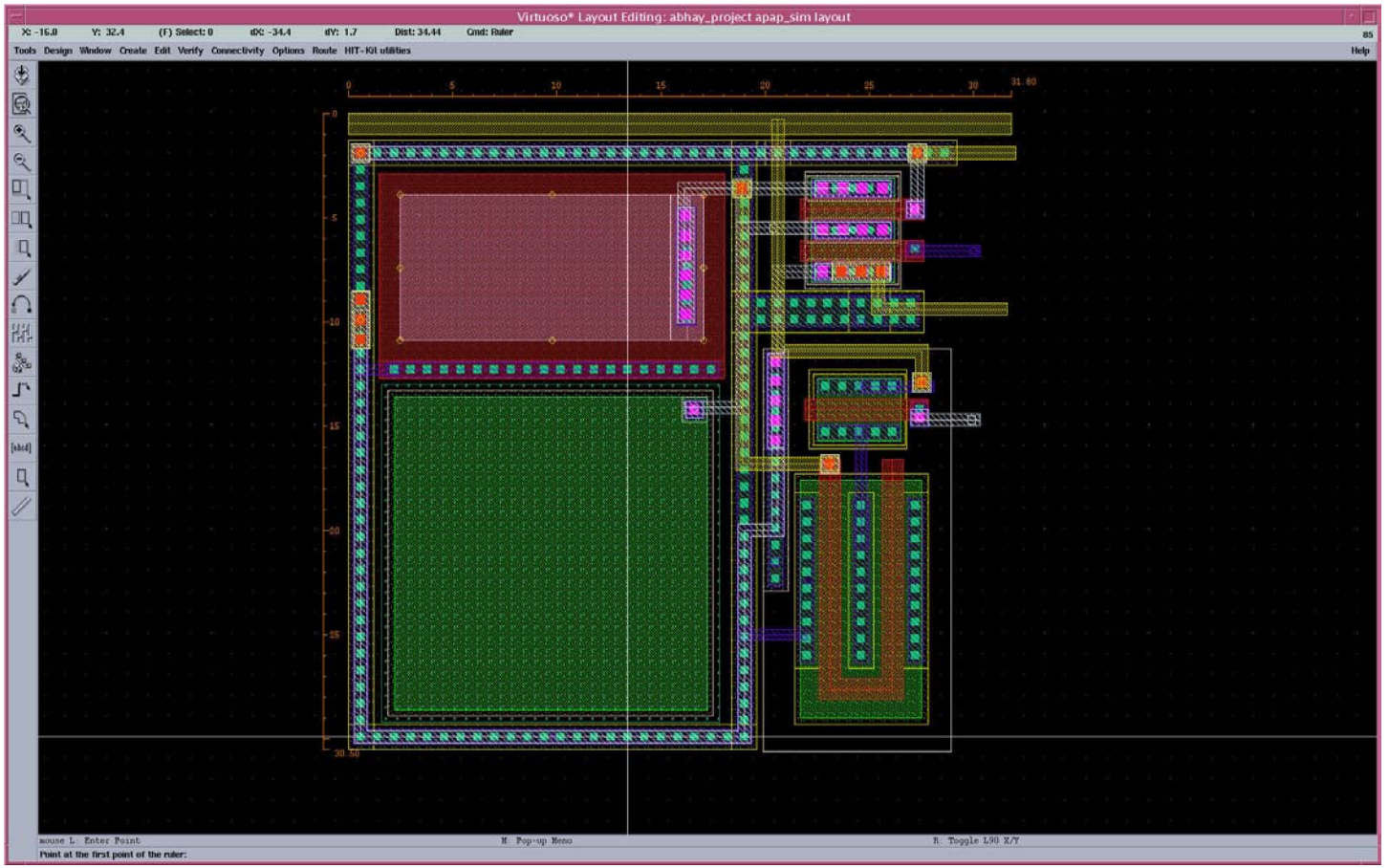
3) LVS test was successful .

4) The use of n-well might have reduced the fill factor.

5) Guard rings were used around Photo diode to prevent the "Blooming" effect .

6) The Layout was deigned to be in the shape of a square as it would help in reducing the area of the matrix.

LAYOUT


Virtuoso® Layout Editing: abhay_project apap_sim layout
Tools Design Window Create Edit Verify Connectivity Options Route HIT-Kit utilities
Help
Point at the first point of the ruler:

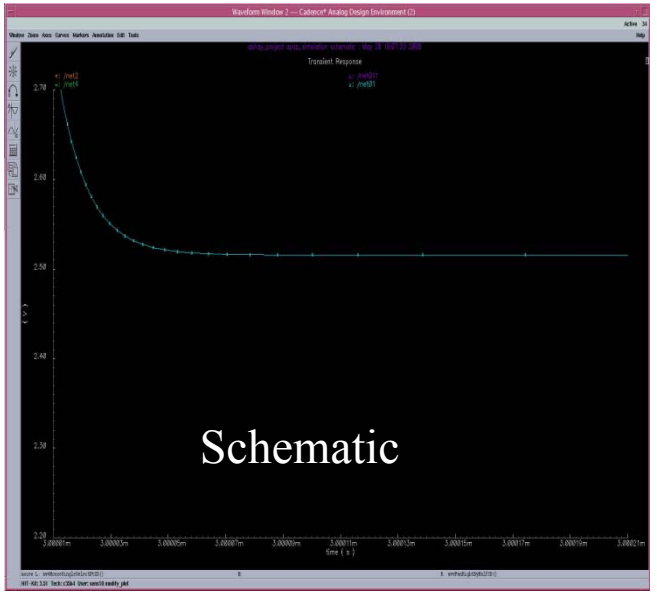
LAYOUT LVS Log

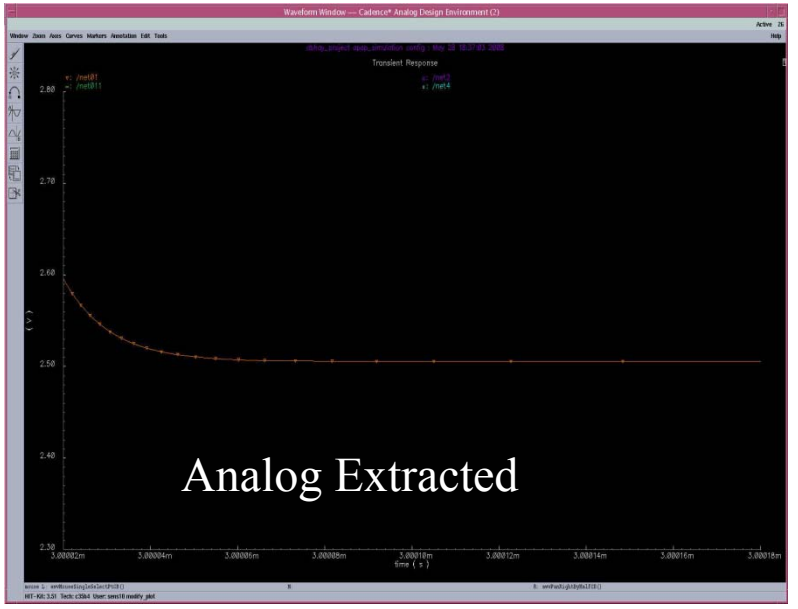
```
The net-lists match.

                          layout  schematic
                             instances
        un-matched              0       0
        rewired                 0       0
        size errors             0       0
        pruned                  0       0
        active                  6       6
        total                   6       6

                               nets
        un-matched              0       0
        merged                  0       0
        pruned                  0       0
        active                  9       9
        total                   9       9

                             terminals
        un-matched              0       0
        matched but
        different type          0       0
        total                   7       7
End comparison:      May 28 18:16:10 2008
```

The LVS check was succesful with the net-list having a complete match.

Config view

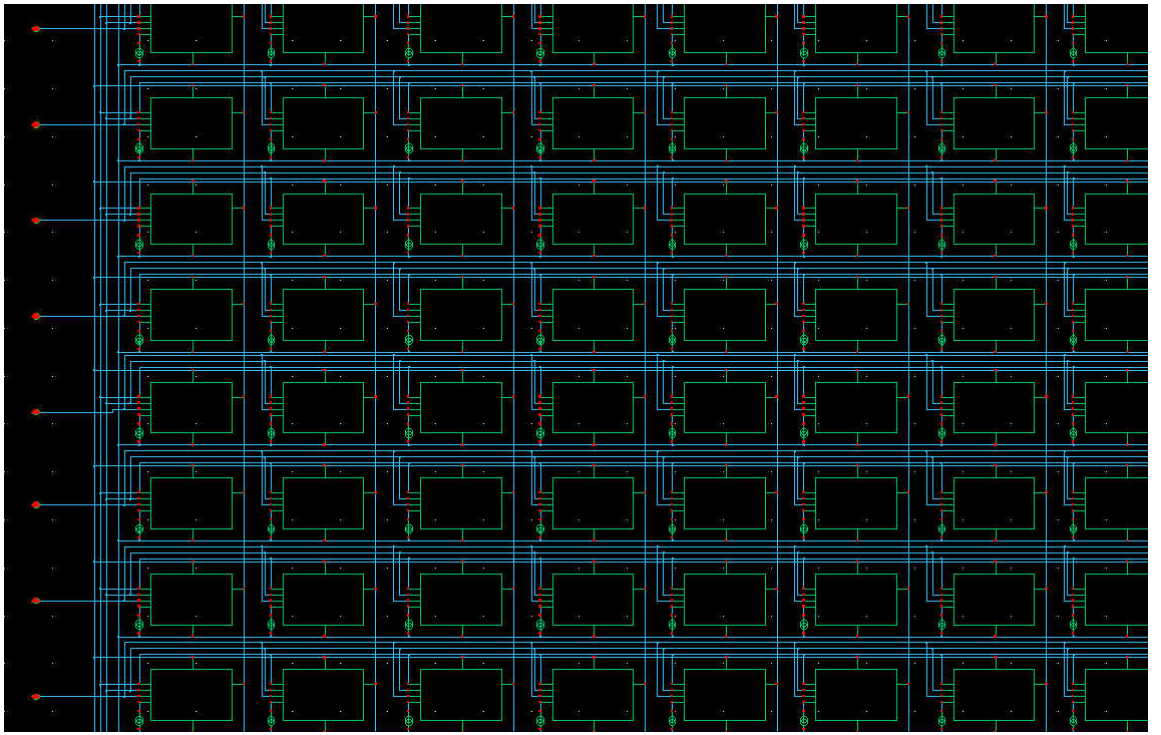
When the simulations of the Schematic view of APS and Analog Extracted View of the APS were compared using config view , Only negligible differences were found .





MATRIX SCHEMATIC(32 *16)

The Matrix was designed with 16 columns and 32 rows.

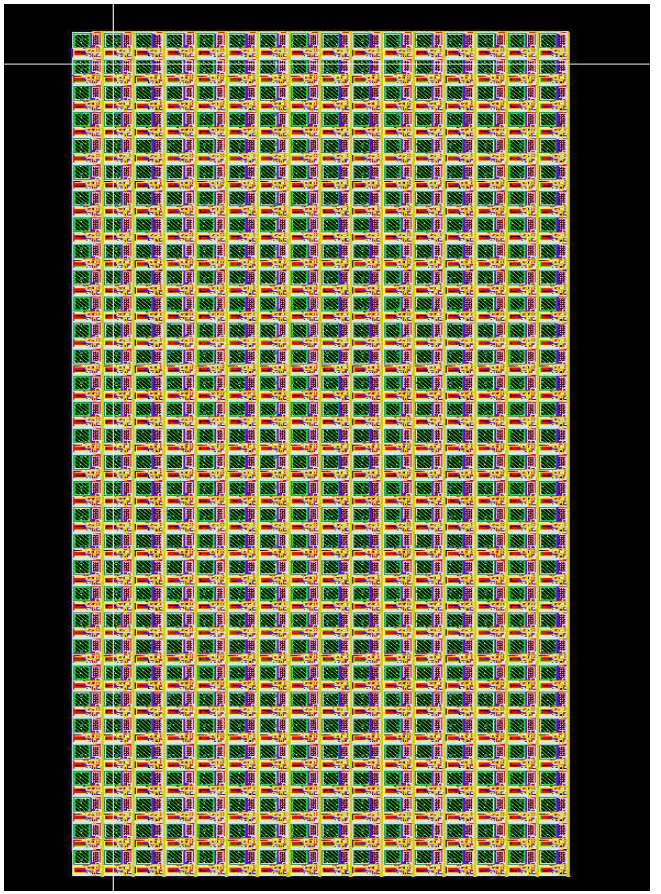


MATRIX LAYOUT (32*16)

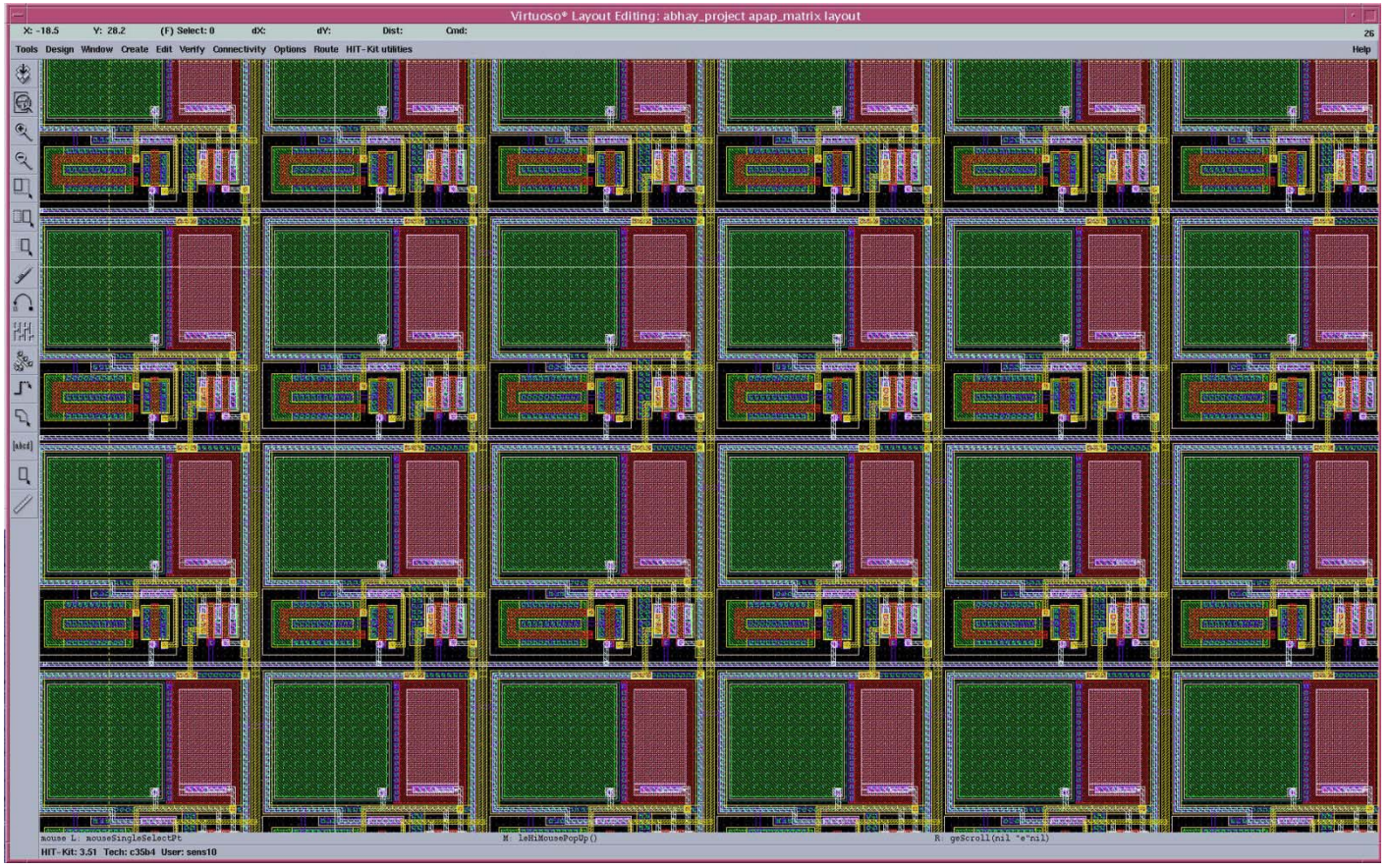
1)The Matrix layout was designed by use of the single pixel cells on a higher level .

2) Care was taken to have *equal spacing* between the diodes in all directions

3) The Area of the Matrix was found to be 1000 microns * 500 microns



MATRIX LAYOUT (16*32)



LVS Log

```
The net-lists match.

                    layout  schematic
                   instances
    un-matched          0    0
    rewired             0    0
    size errors         0    0
    pruned              0    0
    active           3072    3072
    total            3072    3072

                     nets
    un-matched          0    0
    merged              0    0
    pruned              0    0
    active           1588    1588
    total            1588    1588

                   terminals
    un-matched          0    0
    matched but
    different type      0    0
    total              52   52
End comparison:      Apr 24 17:38:35 2008
```

The LVS check was successful for the matrix, with the net lists having a complete match.

Matrix Simulation

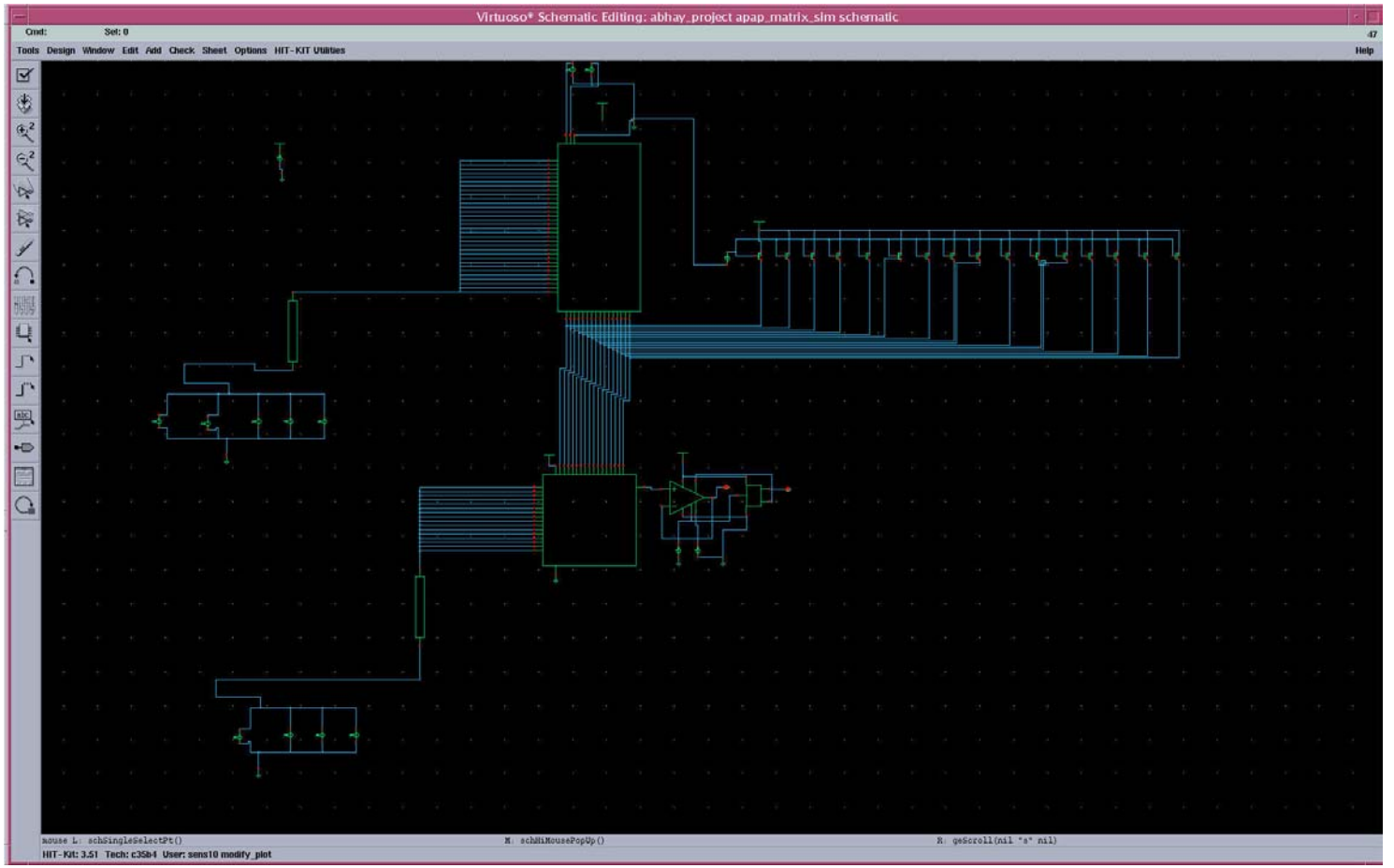
The entire Matrix was simulated with different diodes to check its functionality.

All components which were made use in this simulation were standard components ,So the values obtained were not good enough for a thorough analysis.

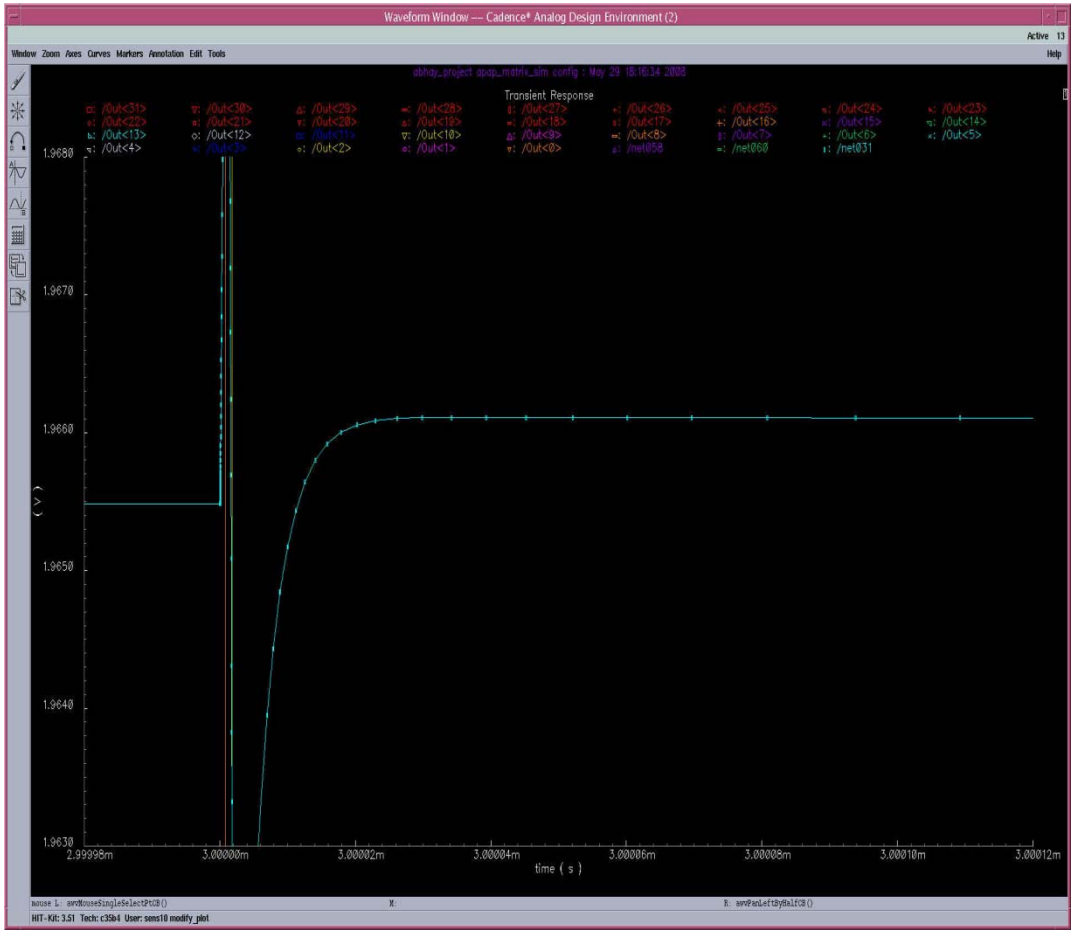
A good analysis of the matrix can be done once the global components are available.

The simulation is a mixed signal simulation, using Decoders as functional components and simulation is carried out using spectre-verilog simulator.

Matrix Simulation



Matrix Read-Out Time

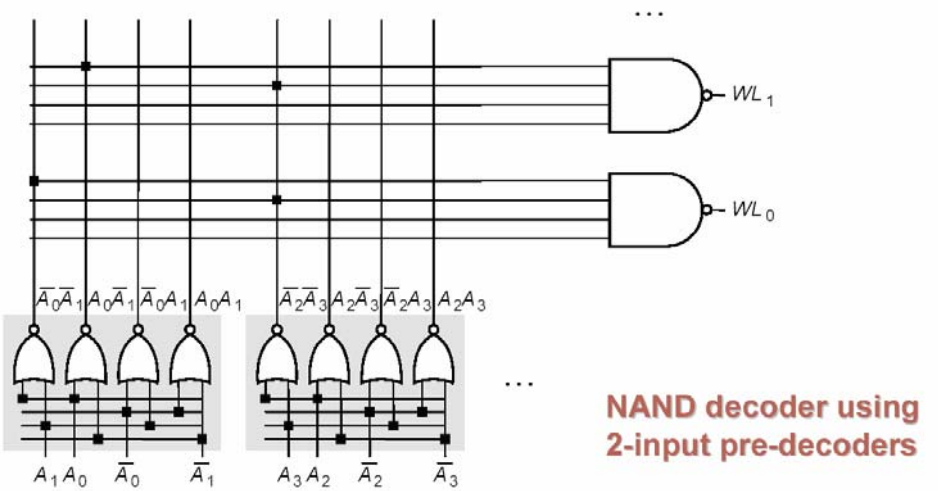


The read out time for the matrix was found to be 110 nano seconds.

An APS cell in the fourth row and 4 column was selected for this readout.

Global Task

The global task is to create a 4 to 16 bit decoder . This can be realized using a combination of NAND gates using CMOS techniques.



Picture taken from http://bwrc.eecs.berkeley.edu/classes/icdesign/ee141_s07/Lectures/Lecture14-SRAM-Decoder-Project_6up.pdf

Conclusion

The differences between PMOS and NMOS source follower was discussed before and it was found that both PMOS and NMOS have their advantages and disadvantages, So a PMOS source follower cannot be totally neglected during design and use of PMOS or NMOS source follower is dependent on the application.

Thank You for your attention!