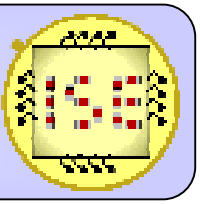

Image Sensor Design

Project4

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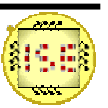
May, 2008

Prof. Dr.-Ing. Andreas König



Overview

1. Introduction
    - *Task*
2. Parts of the Project
    - *Normal Diode and Meander Shape Diode*
    - *APS Design*
    - *Test Result*
    - *Global Task*
3. Conclusion

Task

- The individual project is to design an 32 x 16 APS cell with shutter arrangement. Use a meander shaped photodiode. The photodiode could be implemented as a diffusion type.

- The global task is to place the I/O pads and global pads.

1.Normal Diode and Meander Shape Diode

- Assume that
- Normal Diode:

  The area A is: A=225μm^2

  The perimeter P is: P=60μm
- Meander Shape Diode

  The area A is: A=225μm2

  The perimeter P is: P=452μm

Photo Current

- Normal Diode
- The area A will be: $A = 15\mu m \cdot 15\mu m = 225 \cdot 10^{-12} m^2 = 225\mu m^2$
- The perimeter P will be: $P = 4 \cdot 15\mu m = 60\mu m$
- The area A related contribution will be:

$$C_{d0}^{A} = A \cdot 0.84 \frac{fF}{\mu m^2} = 225\mu m^2 \cdot 0.84 \frac{fF}{\mu m^2} = 189\,fF = 0.189\,pF$$

- The perimeter P related contribution will be:

$$C_{d0}^{SW} = P \cdot 0.25 \frac{fF}{\mu m} = 60\mu m \cdot 0.25 \frac{fF}{\mu m} = 15\,fF = 0.015\,pF$$

$$C_d^A = C_j^A = \frac{C_{d0}^A}{(1 - U/U_D)^{MJN}} = \frac{0.189\,pF}{(1 - (-3.3V)/0.69V)^{0.34}} \approx 0.104\,pF$$

$$C_d^{SW} = C_j^{SW} = \frac{C_{d0}^{SW}}{(1 - U/U_D)^{MJSWN}} = \frac{0.015\,pF}{(1 - (-3.3V)/0.69V)^{0.23}} \approx 0.01\,pF$$

$$C_d^{@-3.3V} = C_j^{@-3.3V} = 0.104\,pF + 0.01\,pF = 0.114\,pF \cong 0.104\,pF$$

Photo Current

- Meander shape
- The area A is: A=225μm^2 , The perimeter P is: P=452μm
- The area A related contribution will be:
- $C_{d0}^{A} = A \cdot 0.84 \frac{fF}{\mu m^2} = 225 \mu m^2 \cdot 0.84 \frac{fF}{\mu m^2}$ =0.189pF
- $C_d^A = C_j^A = \frac{C_{d0}^A}{(1 - U/U_D)^{MJN}} = 0.189 / (1 - (-3.3V)/0.69V)^{0.34} =$ 0.104pF
- The perimeter P related contribution will be:
- $C_{d0}^{SW} = P \cdot 0.25 \frac{fF}{\mu m} = 452 \cdot 0.25 \frac{fF}{\mu m}$ =0.113pF
- $C_d^{SW} = C_j^{SW} = \frac{C_{d0}^{SW}}{(1 - U/U_D)^{MJSWN}} = 0.113 / (1 - (-3.3V)/0.69V)^{0.23}$ =0.075pF
- $C_d^{@-3.3V} = C_j^{@-3.3V}$ = 0.104pF+0.075pF=0.179pF

Photo Current

- As $Q = \frac{C_d^{@-3.3V}}{U_{Bias}}$ so maximum collectable charge
- Normal Diode

  Q =0.114pF/3.3V=3.455*10^{-14} C

  Q/q= 3.455*10^{-14} C/1.609*10^{-19} C=2.147*10^{5} carries
- Meander shape diode

  Q =0.1851pF/3.3V=5.42*10^{-14} C

  Q/q=5.42*10^{-14} C/1.609*10^{-19} C=3.36*10^{5} carries

Integration Time

- According to the simulation result, the integration of the meander shape diode is longer.

	V1	V2	Time	slop
normal diode	2.6149V	575.78mV	9.09ms	0.224
meander shape diode	2.6137	575.78mV	11ms	0.1853

Dark Current

- Normal Diode

$$I_S = 225\mu m^2 * 0.51 \cdot 10^{-18} \frac{A}{\mu m^2} + 60\mu m * 0.61 \cdot 10^{-18} \frac{A}{\mu m}$$

$$I_S \cong 0.15 \cdot 10^{-15} A = 0.15 \cdot fA$$

$$\frac{I_S}{q} = \frac{0.15 \cdot 10^{-15} A}{1.602 \cdot 10^{-19} C} \cong 936 \frac{electrons}{s}$$

$$t_{\text{int}}^{\max} = \frac{reset\ charge}{dark\ current} = 2.147*10^5 / 936\ \text{s} = 229.38\text{s}$$

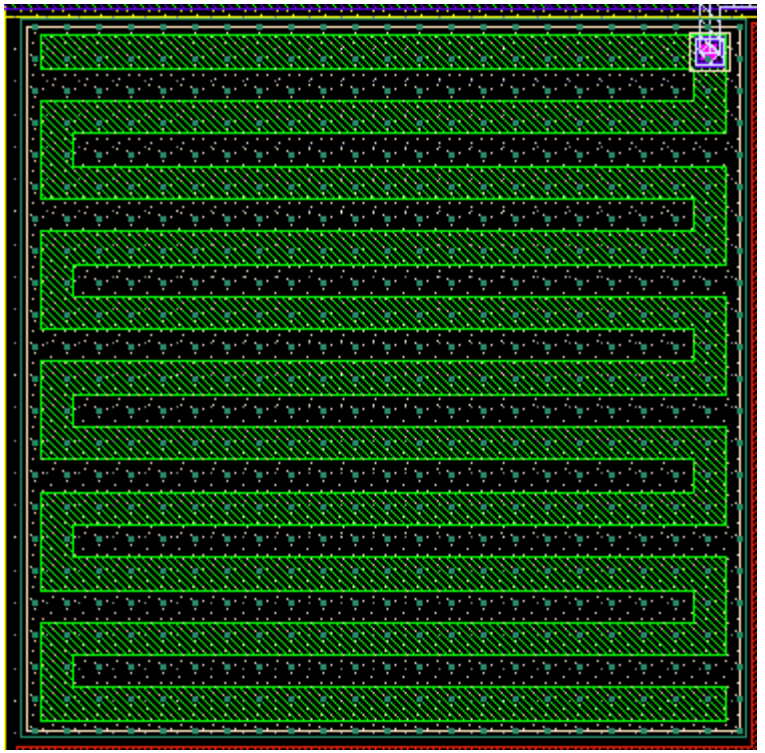
Dark Current

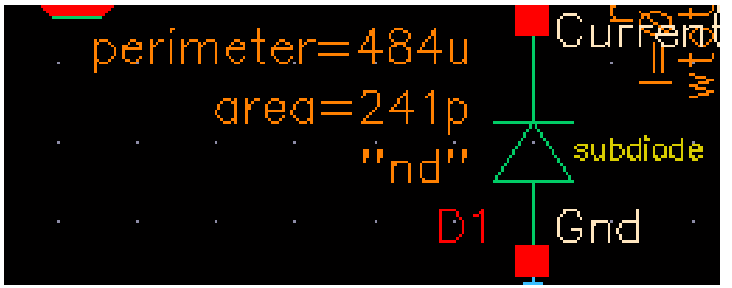
- Meander Shape Diode
- $I_S = 225\mu m^2 * 0.51 \cdot 10^{-18} \frac{A}{\mu m^2} + \quad 452\,\mu m * 0.61 \cdot 10^{-18} \frac{A}{\mu m}$
- Is=0.39*10^{-15}A=0.39fA
- Is/q=0.39*10^{-15}A /1.609*10^{-19} C=2424 $\frac{electrons}{s}$
- $t_{\text{int}}^{\max} = \frac{reset\ charge}{dark\ current} =$ 3.36*10^5 /2424s=138.6s

Others

- The increase in the quantity of collected photo carriers in meander diode is sheer.
- As a result of lateral diffusion, lateral crosstalk is also large, which have diffused out of the pixel site in which it was generated to be collected by a “wrong” pixel.
- It degrades the contrast of the sampled image and presents a lower boundary on the size of the pixel.

Meander Shape Diode





2.APS Design

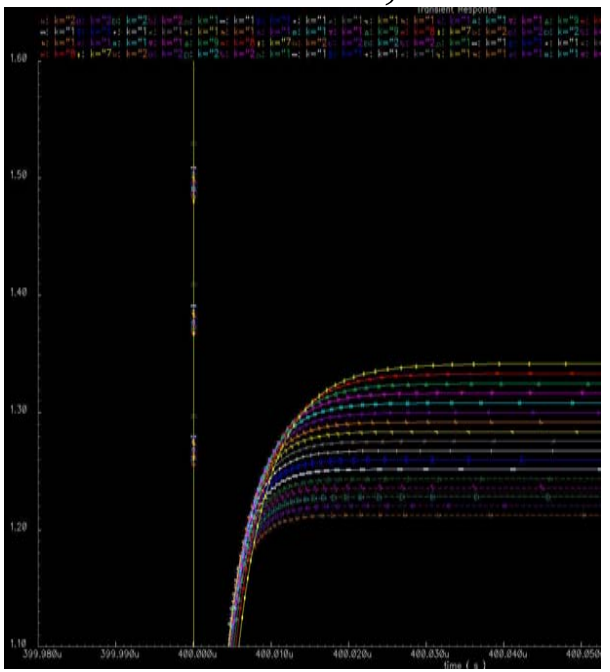
- NMOS realization has two advantages
- Due to higher electron mobility, identical channel dimensions return lower on-resistance
- In an n-well technology, the required area is considerably less.
- In order to hold for values of $U_{GS} > U_{THN}$, thus, the reset voltage on the photo diode can only achieve a value of $U_{reset} - U_{THN}$.

APS Design

- The photodiode goes on integrating, even when the shutter switch is opened
- Potentially, the photodiode voltage can reach zero or even be negative
- Depending on matching properties, this could turn on the shutter switch again, compromising the stored pixel value !
- Application of a slightly increased low voltage level at the reset transistor, to limit the photodiode voltage range.

Source Follower Transistor

- Source Follower Transistor allows the non-destructive read-out of the photo-voltage.
- The length of the Follower Transistor, at least is 1.
- Change the width.
- Width is larger the readout time is smaller.
- Consider the area, I set width=23u



Components Determine

- Increasing C, Readout Time is decreased.
- Increasing Bias Voltage, Readout Time is decreased, Output Voltage is decreased.
- Consider all constrains, I set C=213.4f, Bias Voltage=850mV

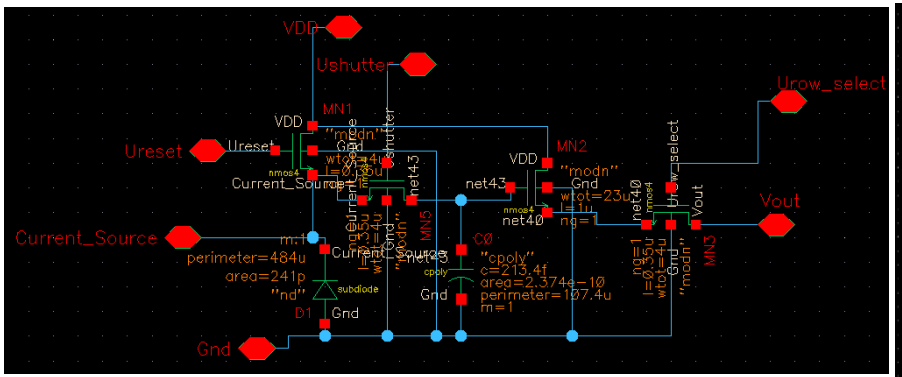
Components Parameter

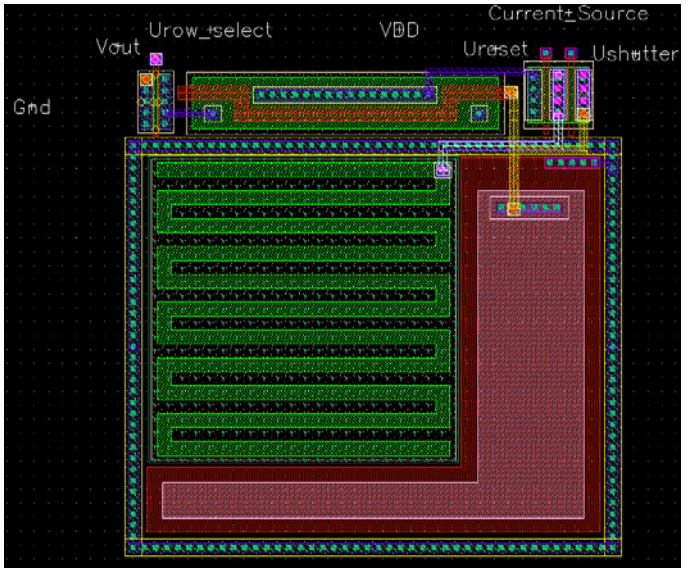
- Poly-Poly Sandwich Capacitor
  C=213.4 f
  Area=2.274e^{-10}
  Perimeter=107.4µ
- Diode
  Area=241µm^2
  Perimeter=484µm
- Transistor
  Source Follower Transistor: W/L=23/1
  Switch Transistor: W/L=4/0.35
- Load Capacitor
  C=1.29998 pF
- Current Source=100pA

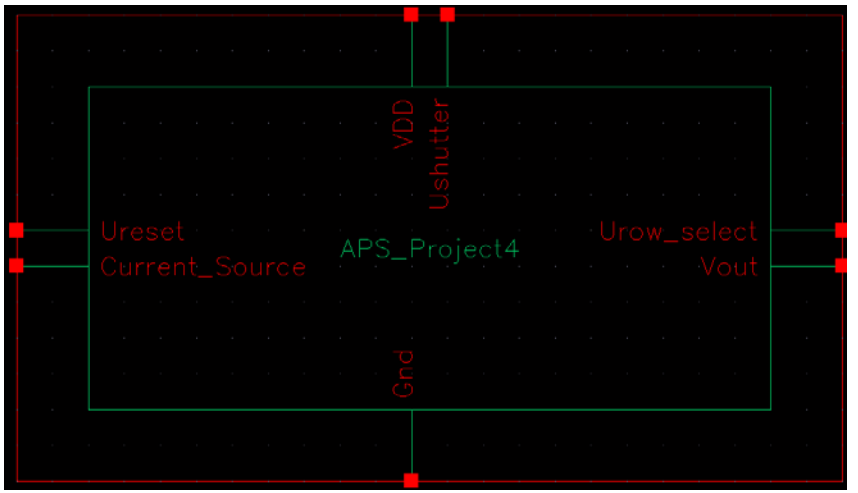
Voltage Set

	Ureset	Ushutter	Urow_select	Ubiase
V1	900mV	0	0	850mV
V2	3.3V	3.3V	3.3V	850mV
rise time	50ps	50ps	50ps	
fall time	50ps	50ps	50ps	
Pulse width	200us	300us	100us	
Delay Time			400us	

Schematic & layout & symbol—APS Cell





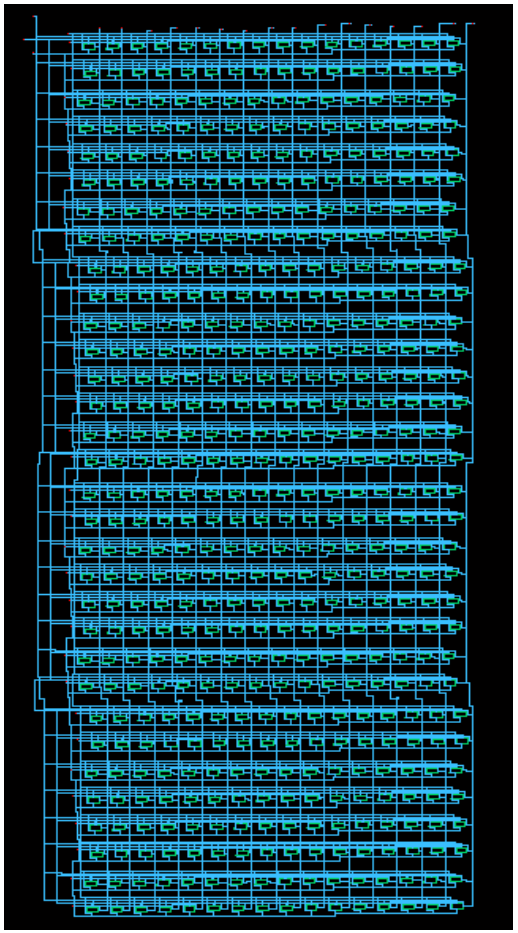


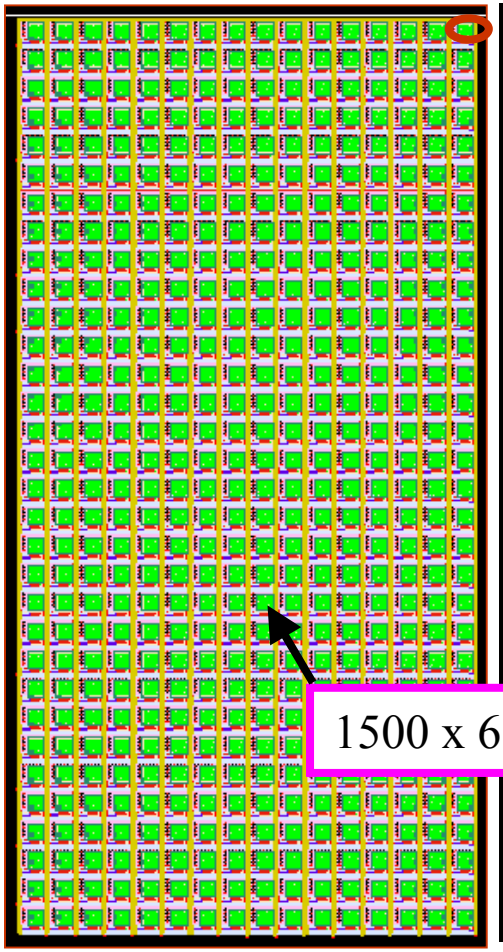
36 x 36 μm

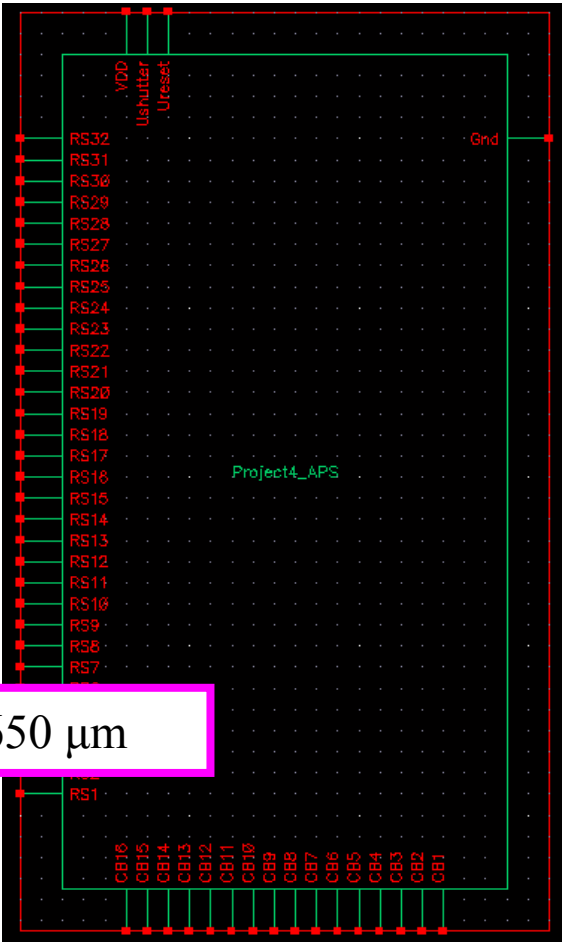
LVS Result

```
The net-lists match.

                              layout  schematic
                                 instances
        un-matched                  0       0
        rewired                     0       0
        size errors                 0       0
        pruned                      0       0
        active                      6       6
        total                       6       6

                                   nets
        un-matched                  0       0
        merged                      0       0
        pruned                      0       0
        active                      9       9
        total                       9       9

                                 terminals
        un-matched                  0       0
        matched but
        different type              0       0
        total                       7       7
End comparison:      May 29 17:35:05 2008
```

Schematic & layout & symbol—APS Matrix



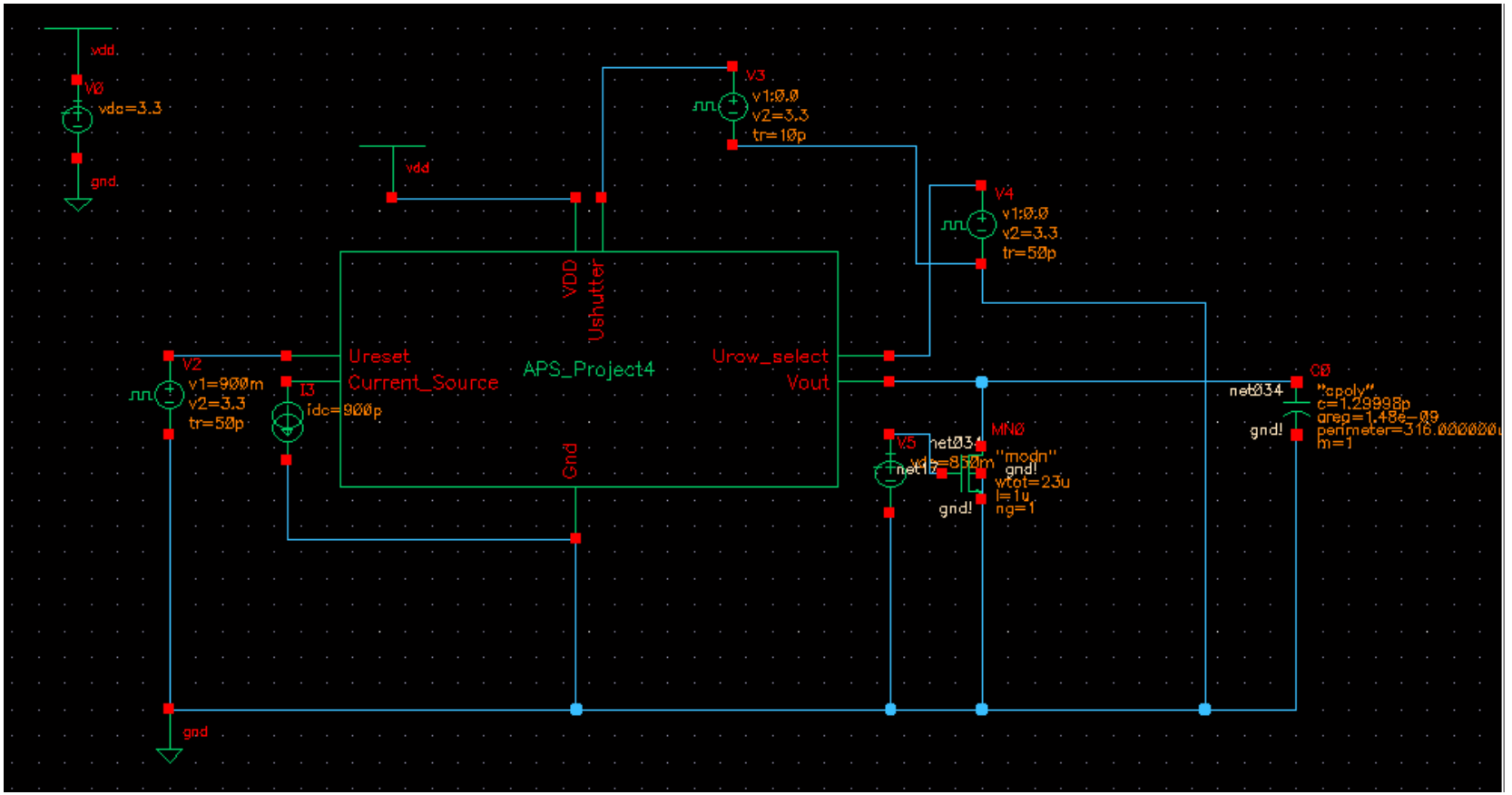




LVS Result

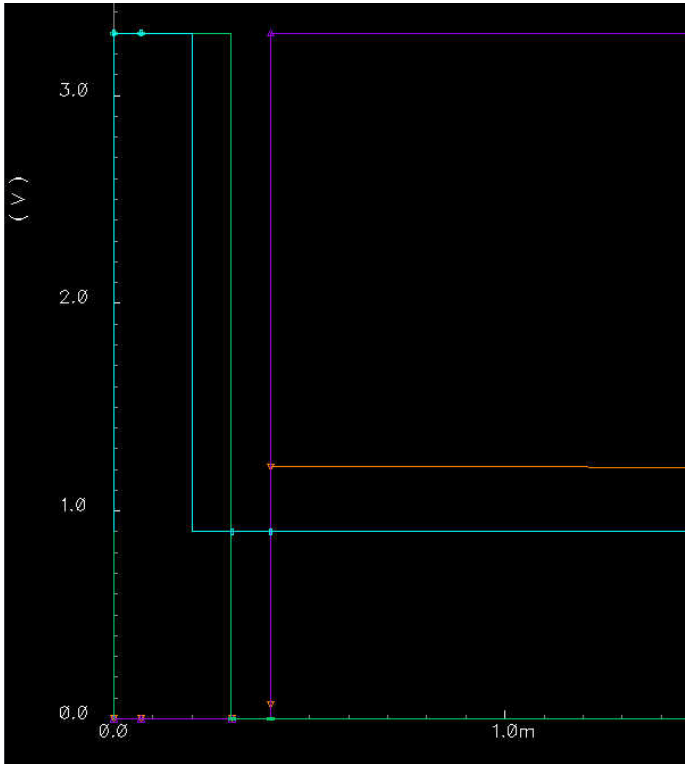
```
The net-lists match.

                                 layout  schematic
                                    instances
        un-matched                  0       0
        rewired                     0       0
        size errors                 0       0
        pruned                      0       0
        active                      3072    3072
        total                       3072    3072

                                      nets
        un-matched                  0       0
        merged                      0       0
        pruned                      0       0
        active                      1588    1588
        total                       1588    1588

                                    terminals
        un-matched                  0       0
        matched but
        different type              0       0
        total                       52      52
End comparison:      May 29 17:51:38 2008
```

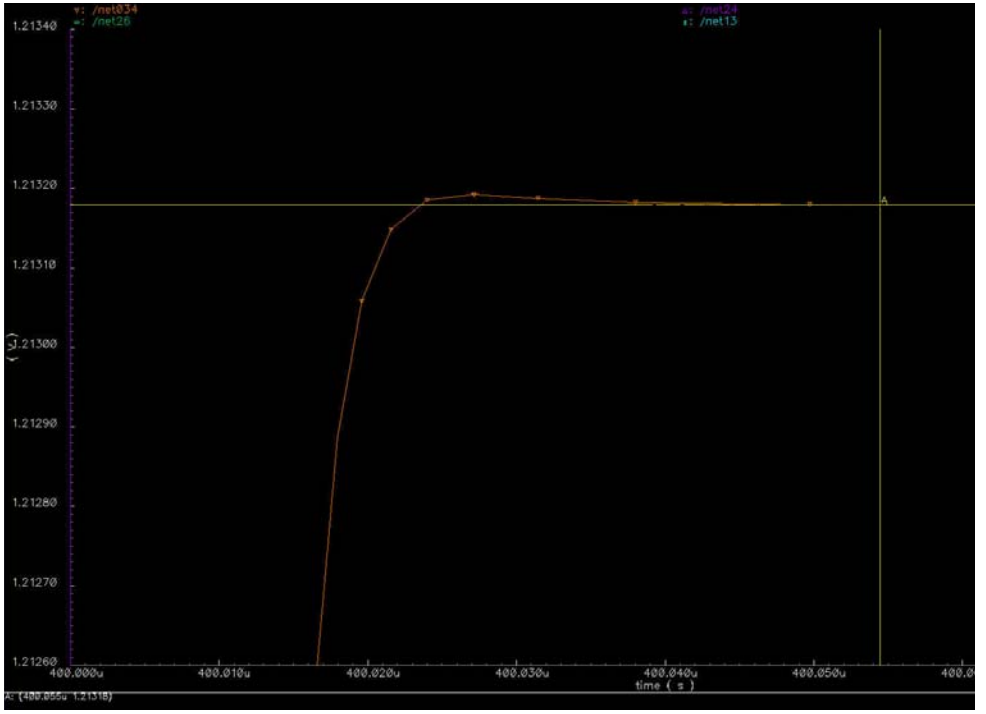
3.Test Result—APS Cell



Readout Time

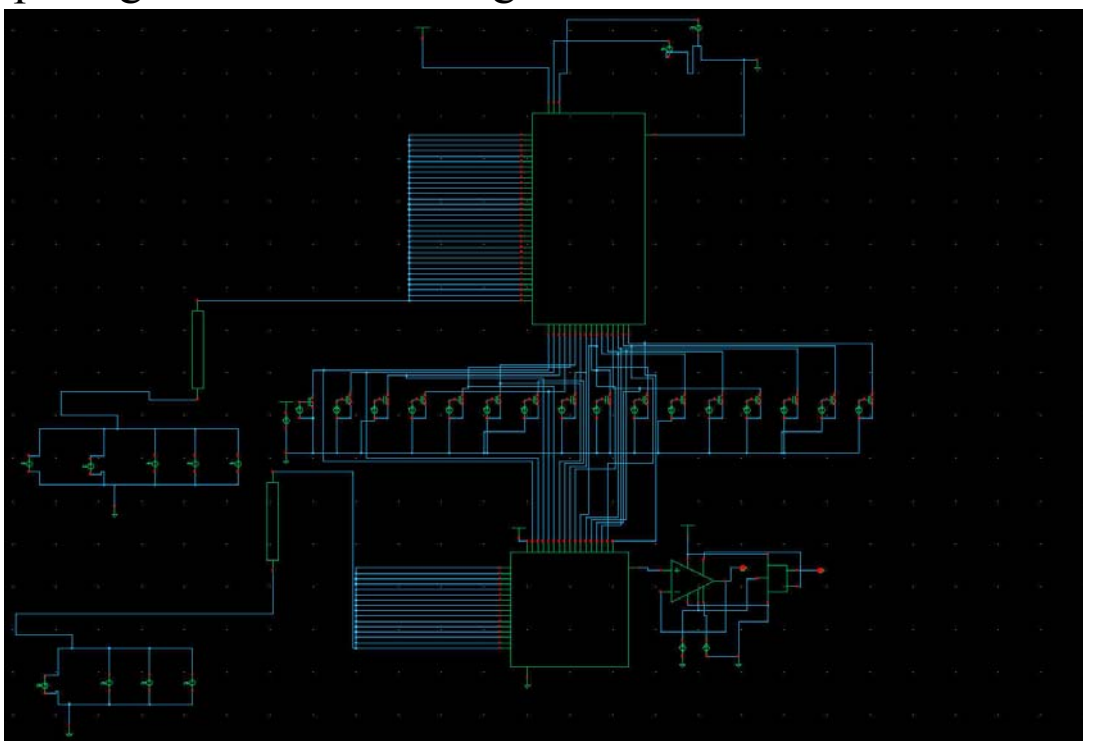
- Readout Time: 55ns
- Output Voltage: 1.2V





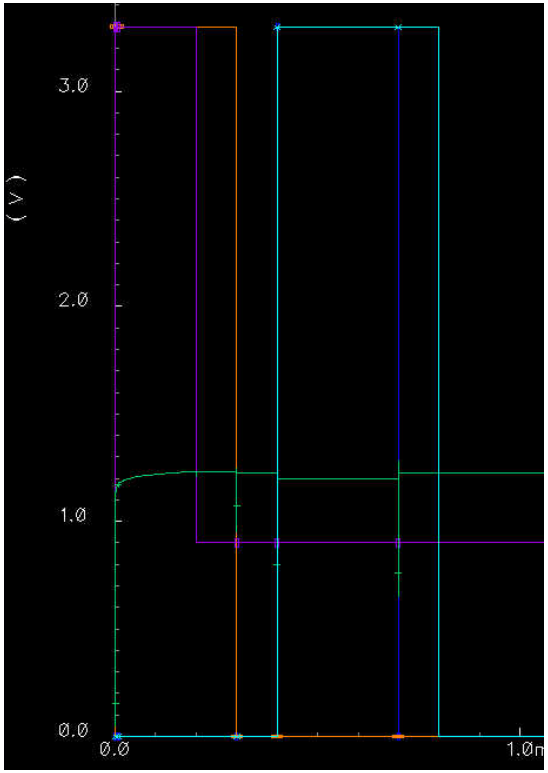
Test Result—APS Matrix

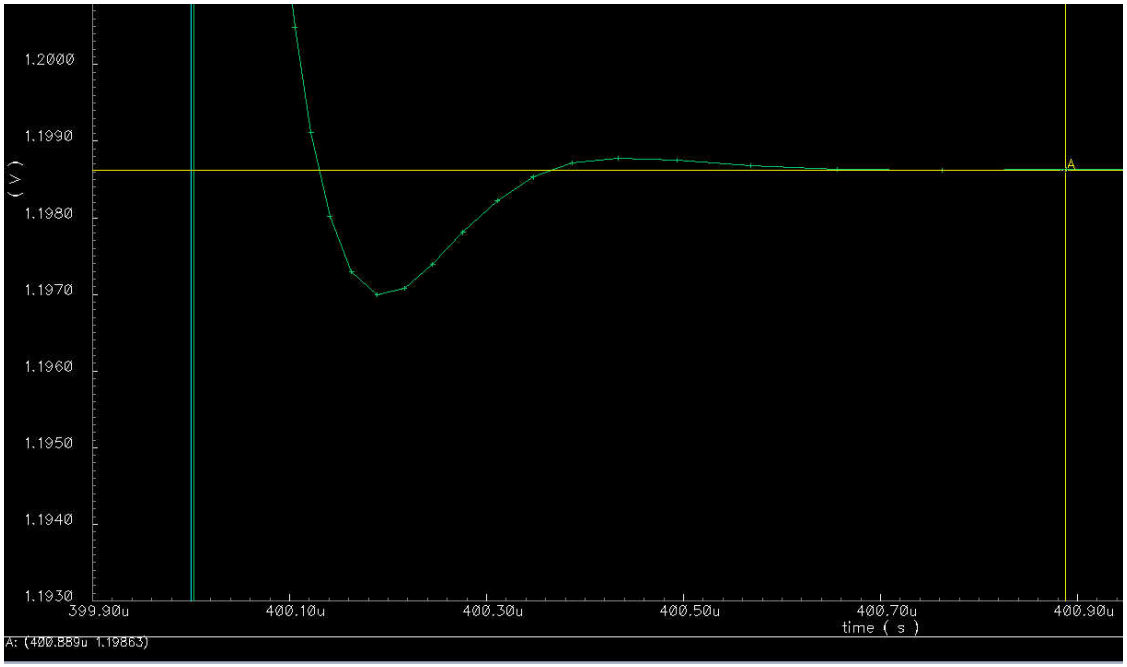
- I use two Decode, 16 bits and 32 bits, an analog multiplexer and an inverter to amplify the output signal.
- The output signal is the mixed signal.



Readout Time

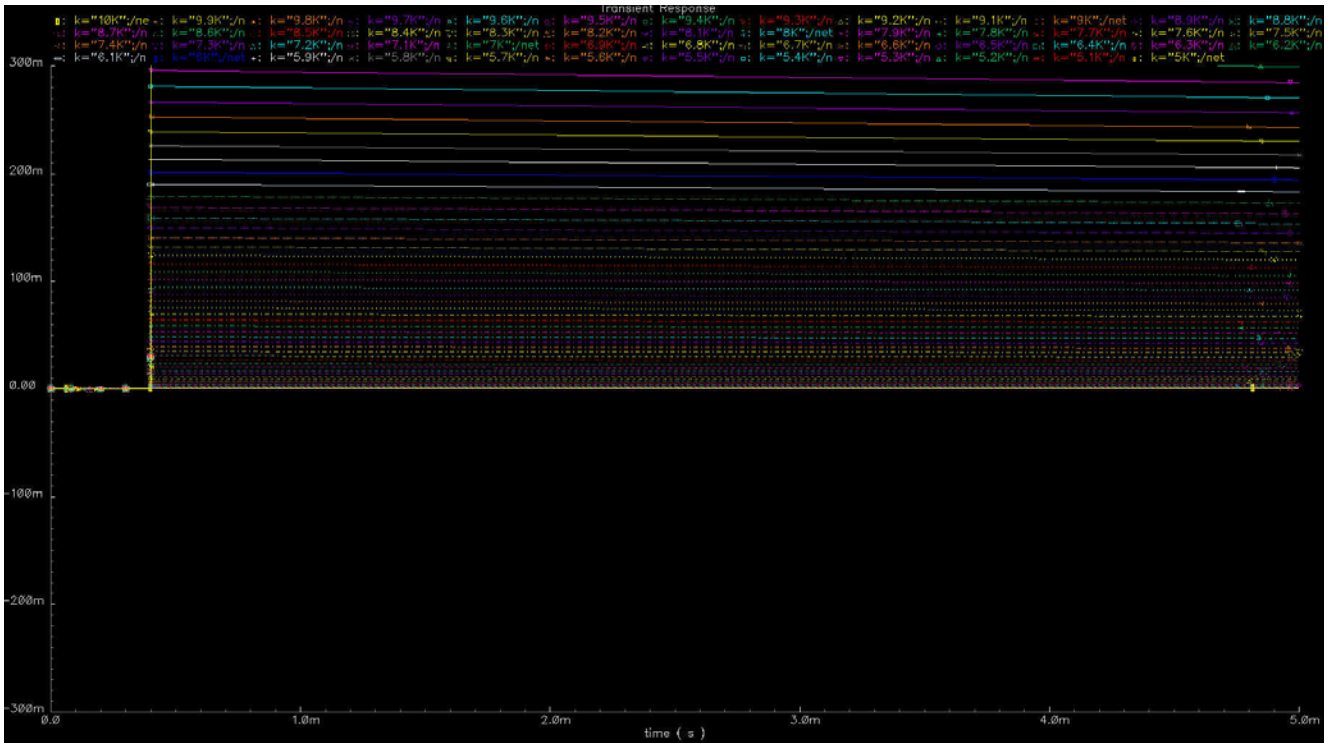
- Readout Time: 900ns
- Output Voltage: 1.2V





Dynamic Range

- 72.26uV(Current Source 10000pA) < Vout <1.24 V (Current Source 0)



4.Global Task

- Place the I/O pads and global pads
- 5-bit Row Address
- 4-bit Column Address
- 1-bit Reset
- 1-bit exposure
- 2-bit VDD/GND
- 1-bit Reference Voltage
- 8-bit Digital

Signal pad

- Signal pad die placement considerations:
- The logic located on the die that will connect to the pad.
- Bonding wire angles.
- Switching frequency of pads and proximity to VDD/VSS pads
- Cross-talk between pads.
- ESD considerations – charge concentrates at points, like in comers of the die – pads placed in the corners of the die may be more susceptible to ESD, so use VSS pads in the die corners.

Power pad

- Power pad die placement considerations:
- Don't place different power rails next to each other (e.g. 3.3V I/O power pad butted up against a 1.8V core power pad).
- Power pads should be close to fast switching outputs with high slew rates, particularly if those output pads drive large loads.
- Assist in power grid routing.
- Connect to power rings vs. directly to package balls/pins.

Conclusion

- The project is to design an 32 x 16 APS cell with shutter arrangement, using a meander shaped photodiode.
- Compared with the normal diode, as the meander shape diode (large perimeter diode) .
- The maximum collectable charge is larger.
- The integration time is increased, but the maximum integration time which is limited by the dark current is decreased.
- The lateral diffusion is larger, so the edge-effect is stronger, however, the followed lateral crosstalk is increased.
- The I/O pad should be placed in appropriate position, considering the whole circuit structure and path delay, in order to reduce the interconnection length and circuit delay, minimum core/chip area consumption.

Thank You for your attention!