Rheinland-Pfälzische Technische Universität Kaiserslautern Landau

Institute of
Cognitive Integrated Sensor Systems
Department of Electrical and Computer Engineering

Design of a 192x32 Active Pixel Sensor in 0.35um CMOS Technology

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'Semester Project HEIS', 2023

Supervisor: Prof. Dr.-Ing. Andreas König

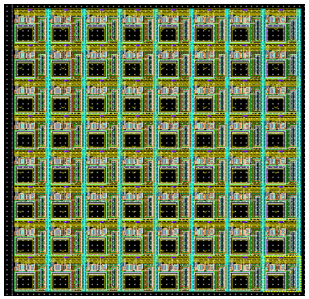
Overview

1. Motivation
2. Design Requirements
3. Design of the Pixel Matrix (Amira Ghezal)
4. Design of the Logic (Luis Pena)
5. Design of the Readout Circuit and ADC (Lukas Birkenmeier)
6. Top-Level Hierarchical Layout and Post Layout Simulations (Lukas Birkenmeier)
7. Conclusion

Motivation

- In the 19th and 20th centuries, film cameras were very popular. However, taking a picture using those cameras was expensive and complicated.
- As the photographic market expanded, companies began to invest in new technologies such as Active Pixel Sensors (APS), which are used in digital cameras.
- In this project, we designed and simulated a matrix of APS.

Taking a picture



Active pixel sensors

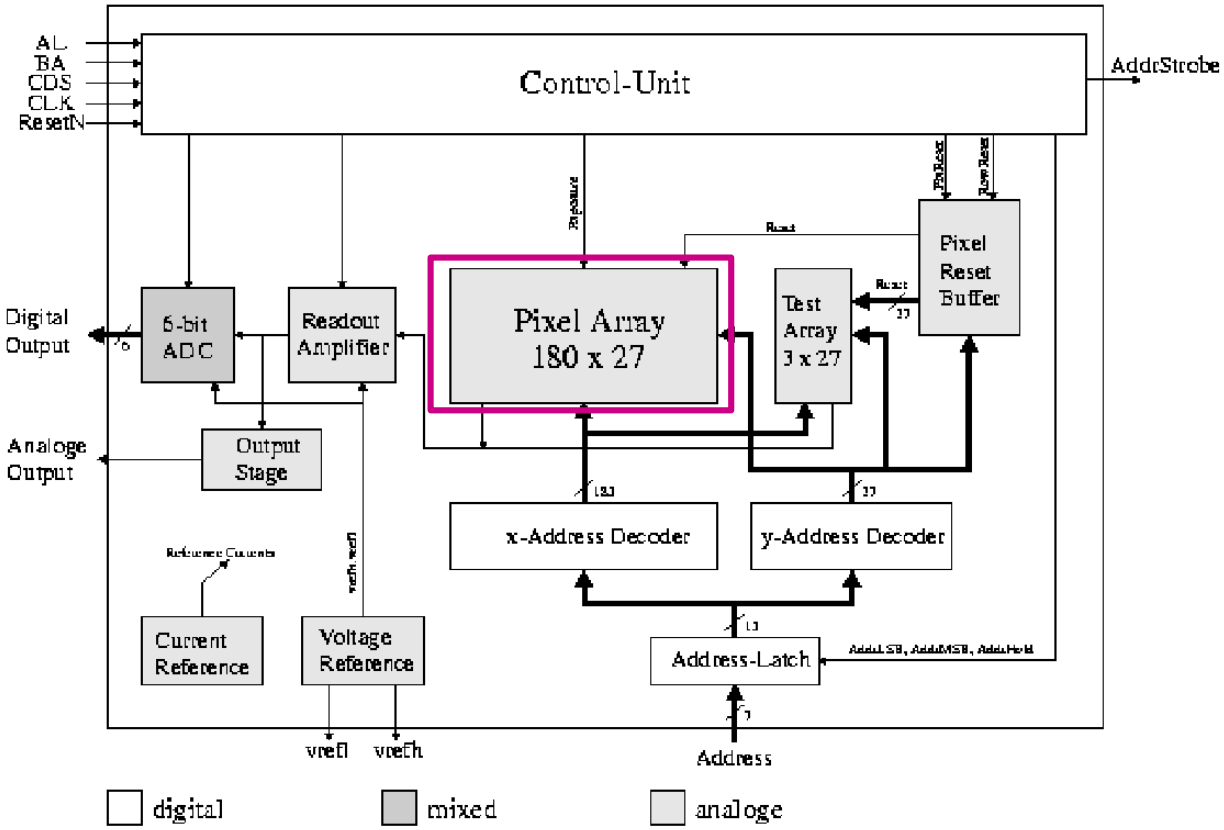
Digital picture

Design Requirements

Sensor Constituents	Design parameters
Pixel photodetector size	15umx15um
Matrix size- row	180
Matrix size -column	27
ADC	6 bits
Frames/sec	20
Column select transistor speed	<=10.29us
Row select transistor speed	<=1.85ms
Read out amplifier	>=200 KHz (-3db), SC and AZ
Output stage	buffer

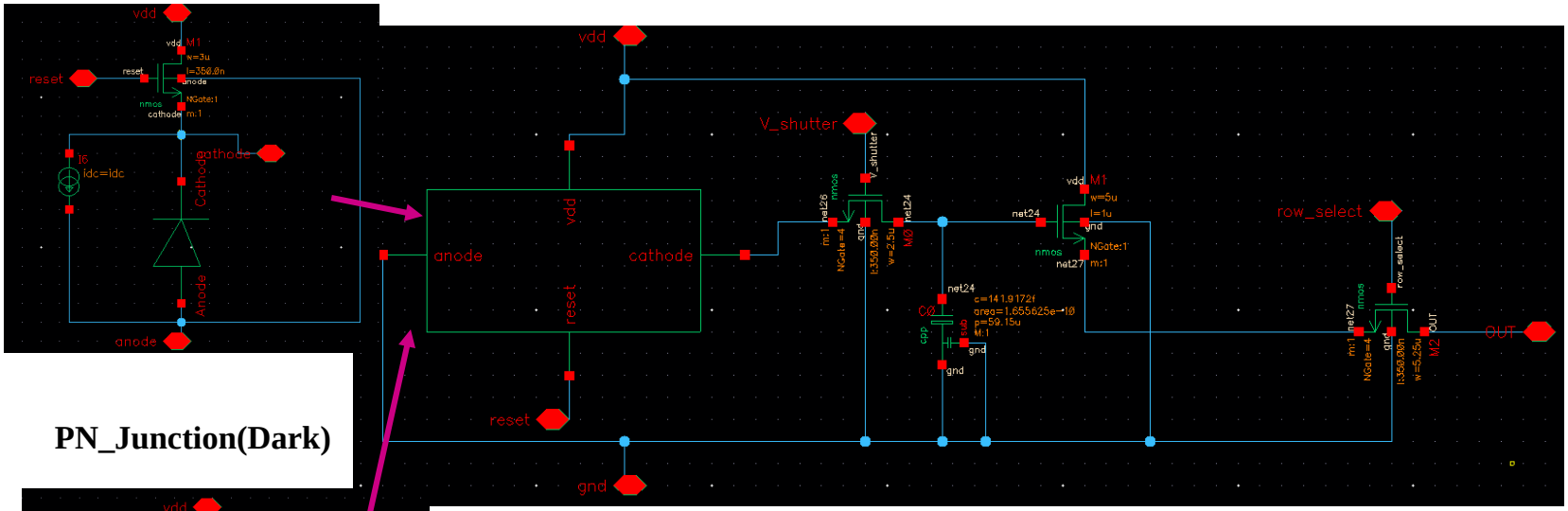
Design of the Pixel Matrix

Overview

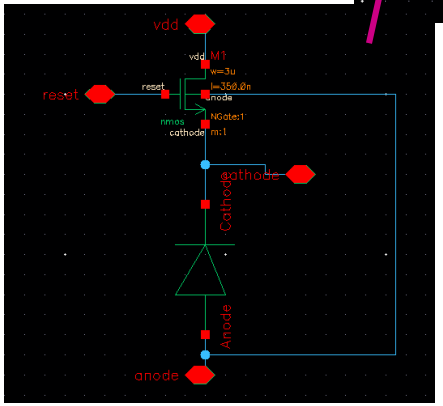


Active Pixel Cell (APS)
Schematic

PN_Junction(Light source)

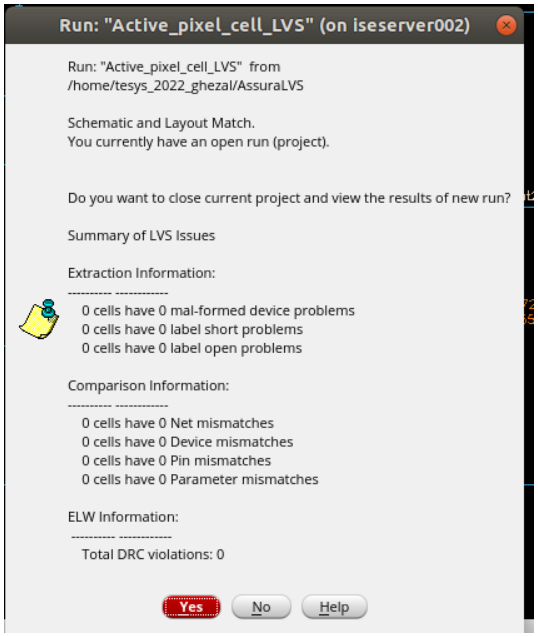


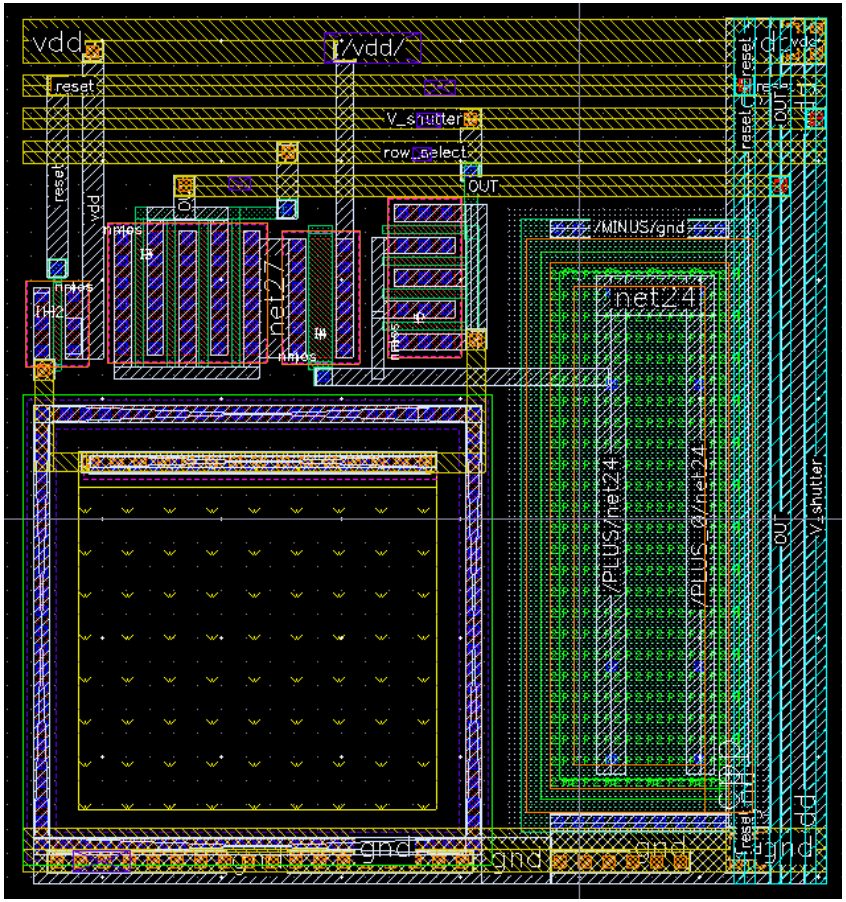
PN_Junction(Dark)



Active Pixel Cell (APS)
Layout

- Fill Factor: 18.5 %
- 

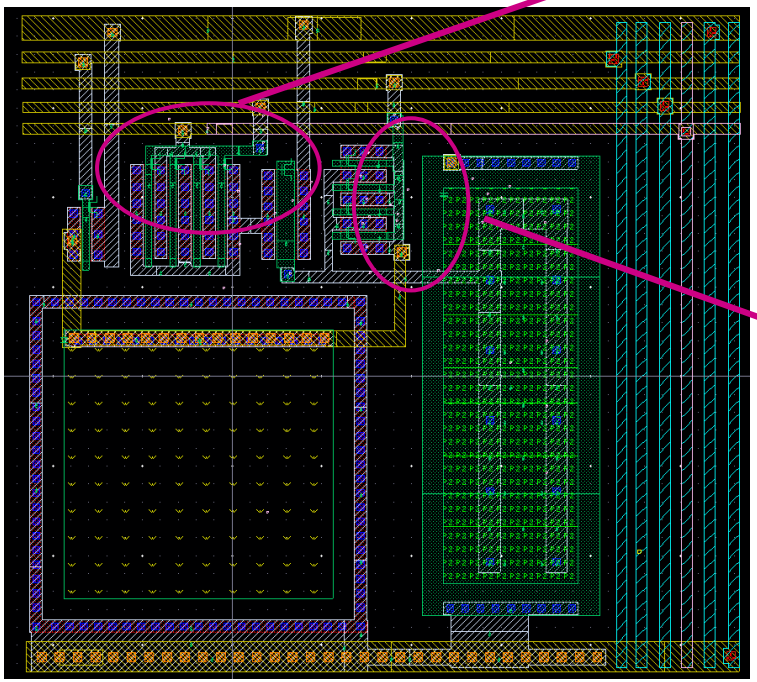


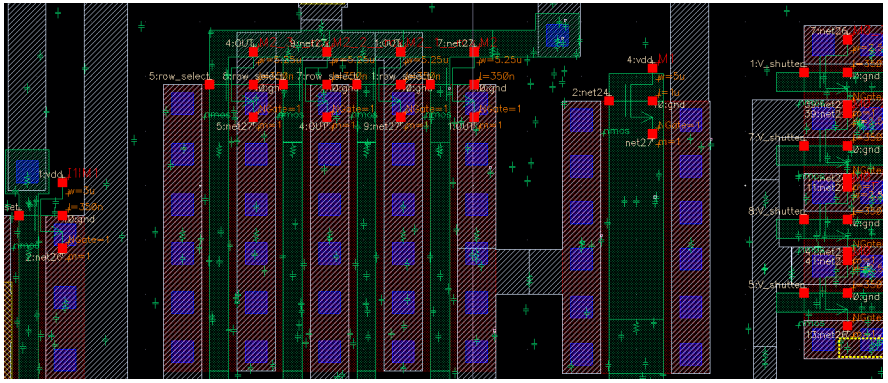


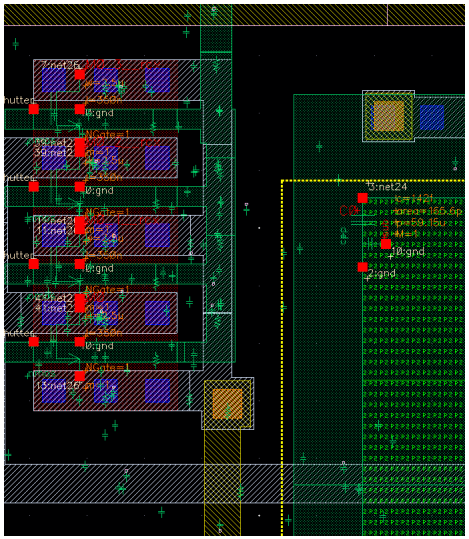
The layout has been designed in such a way that an arrangement in a matrix is possible by simply placing the cells next to each other.

Active Pixel Cell
Post Layout

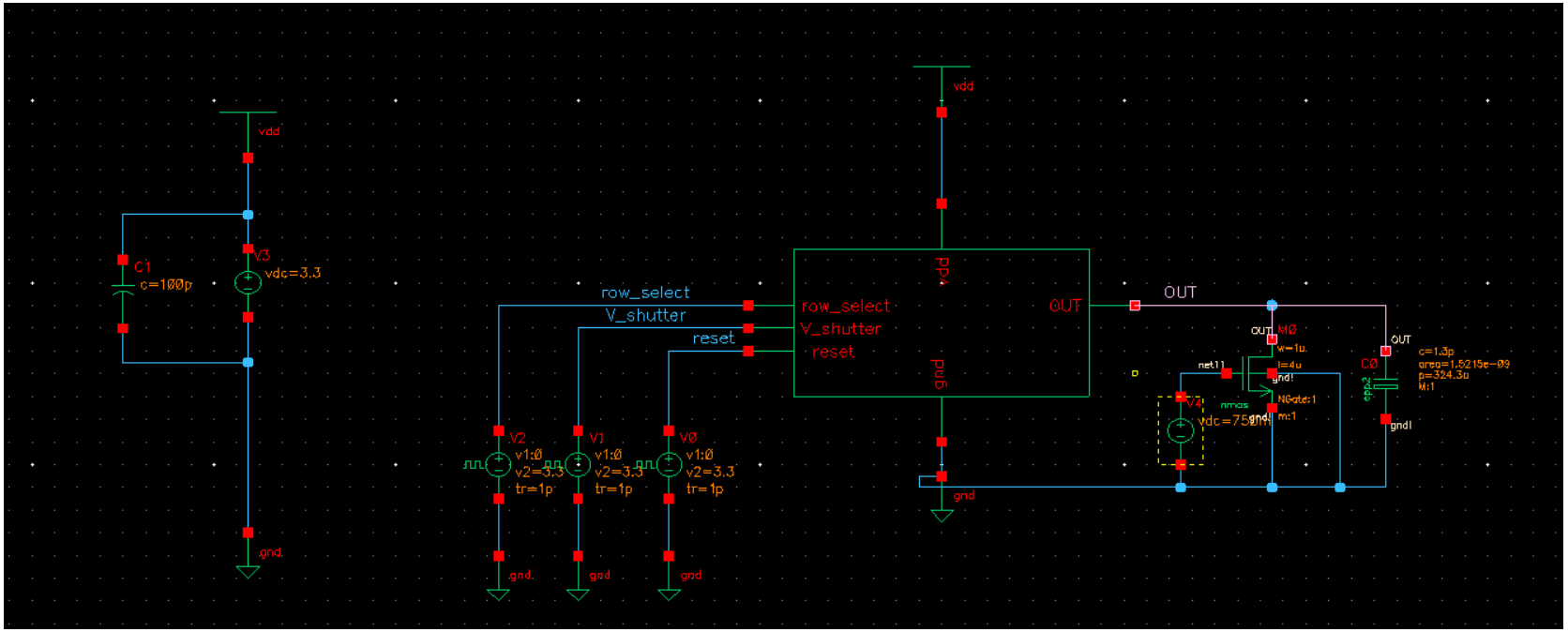
Parasites



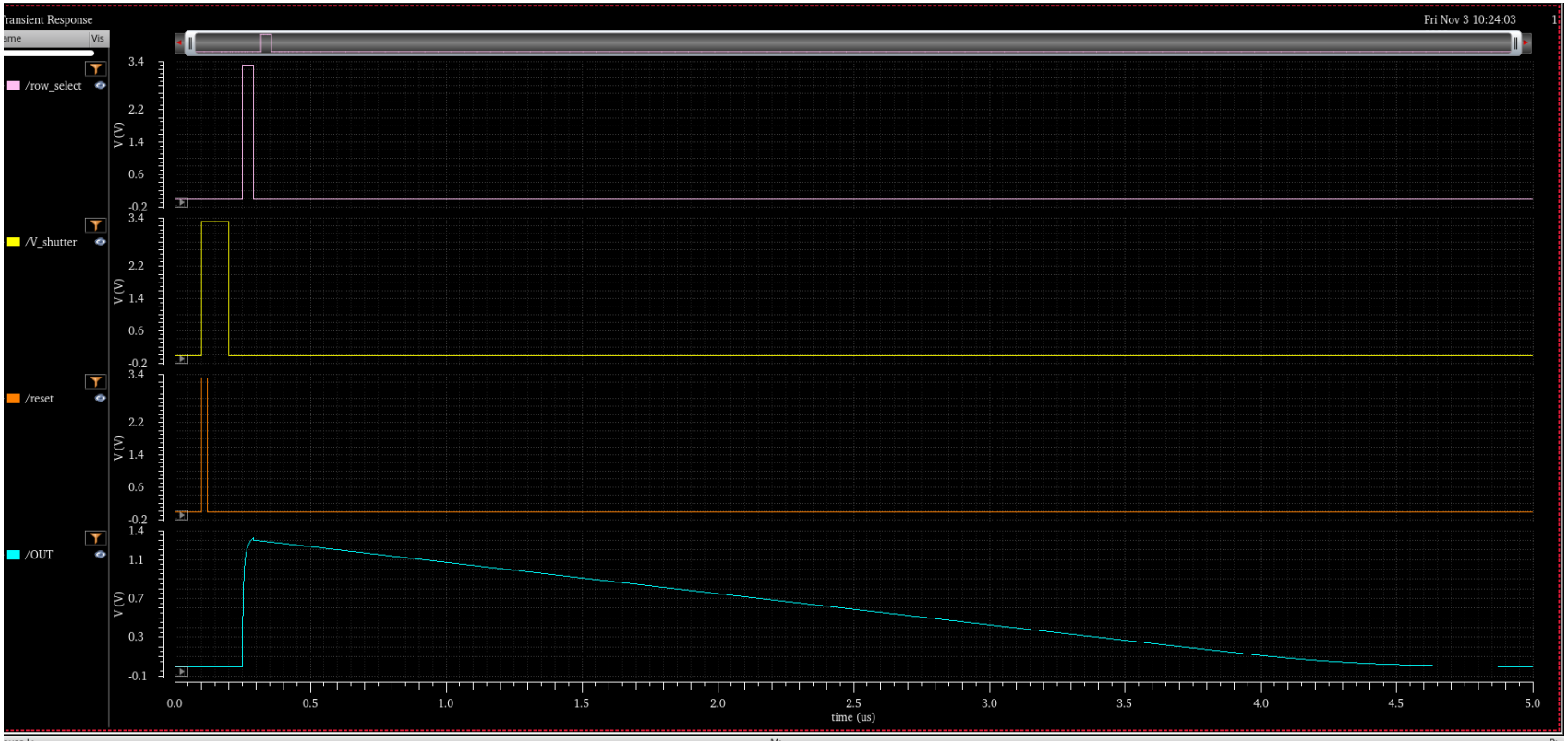




Active Pixel Cell (APS)
Test Bench

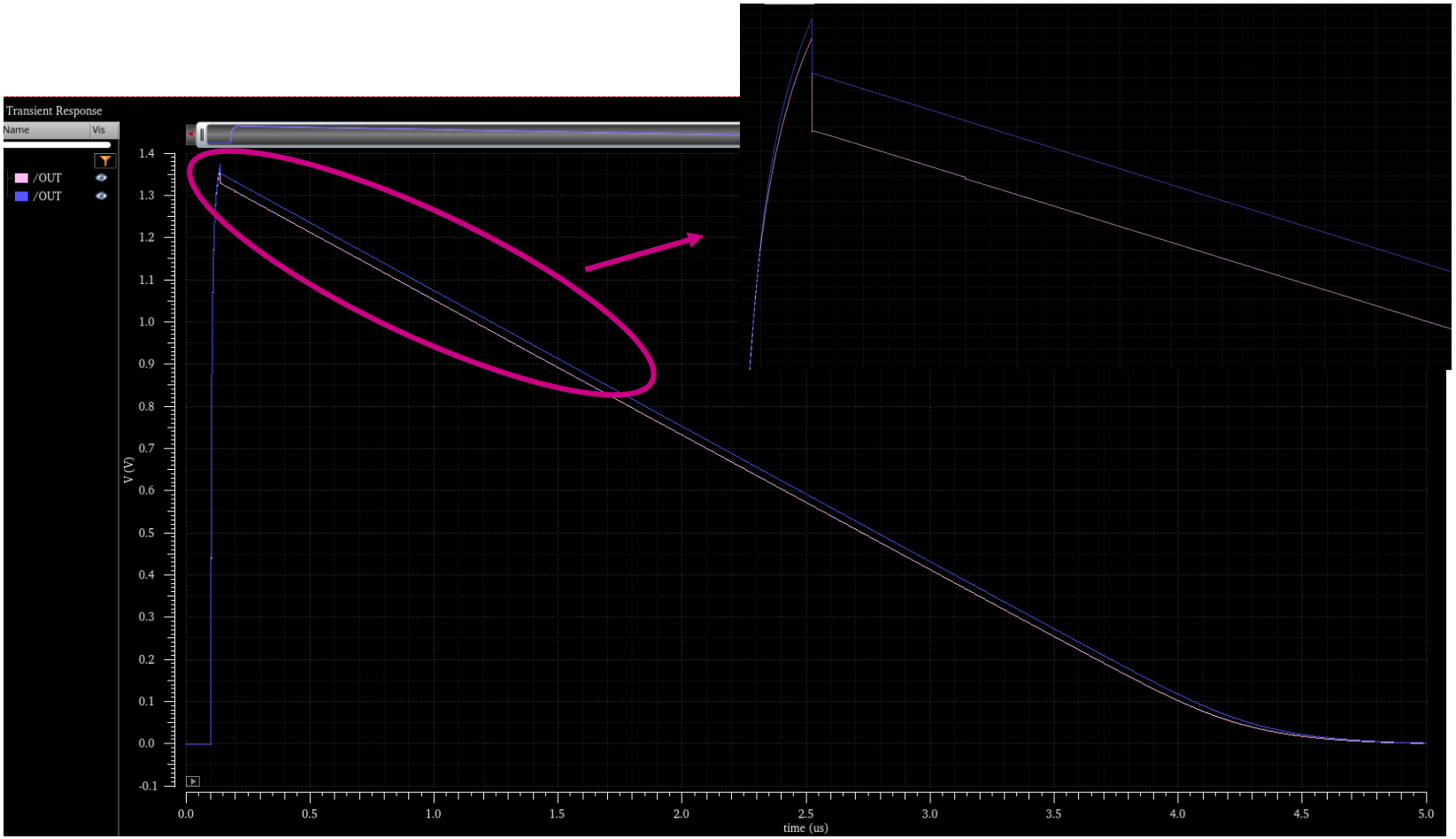


Active Pixel Cell (APS)
Simulation



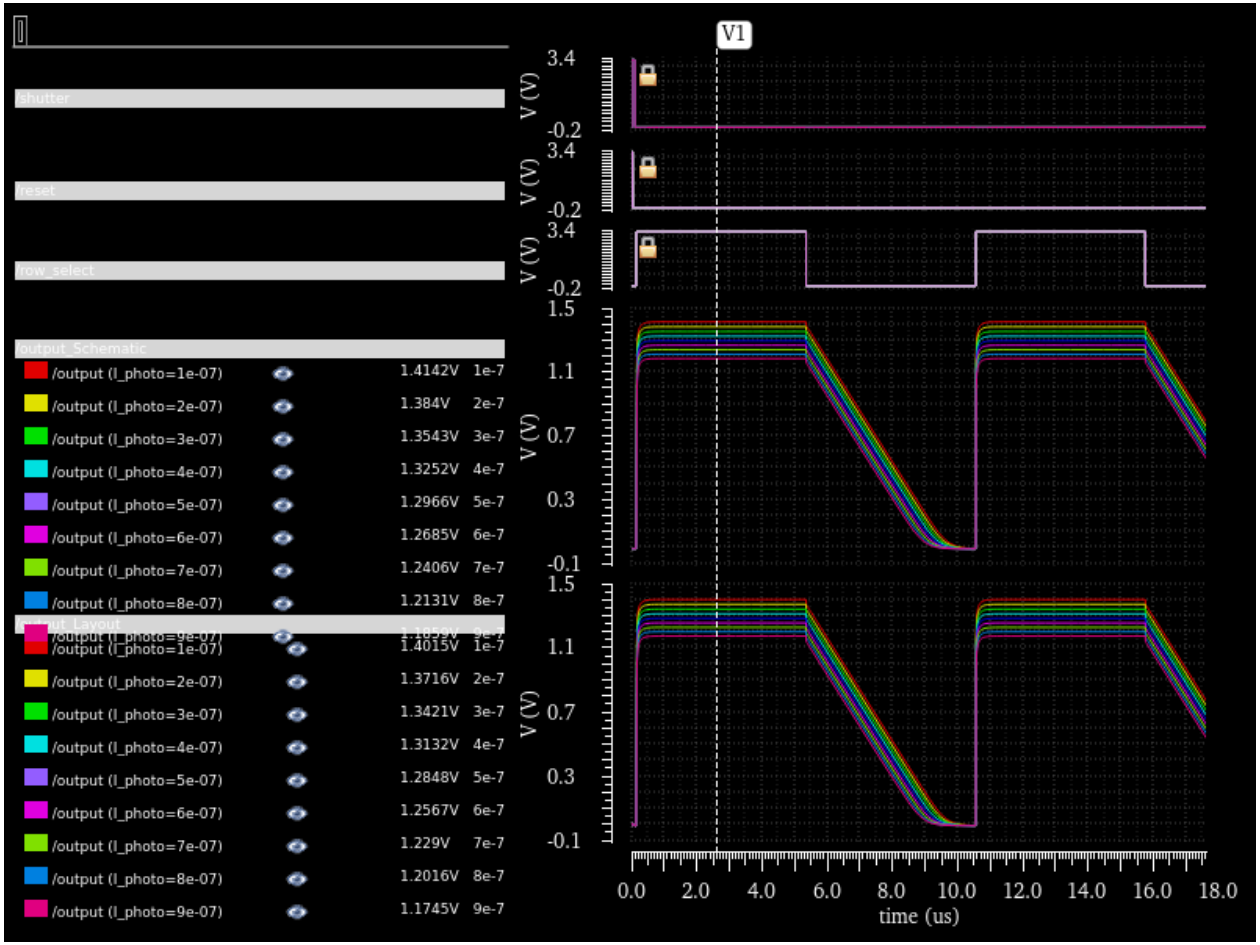
Active Pixel Cell (APS)

Schematic and Post Layout Simulation (Dark)

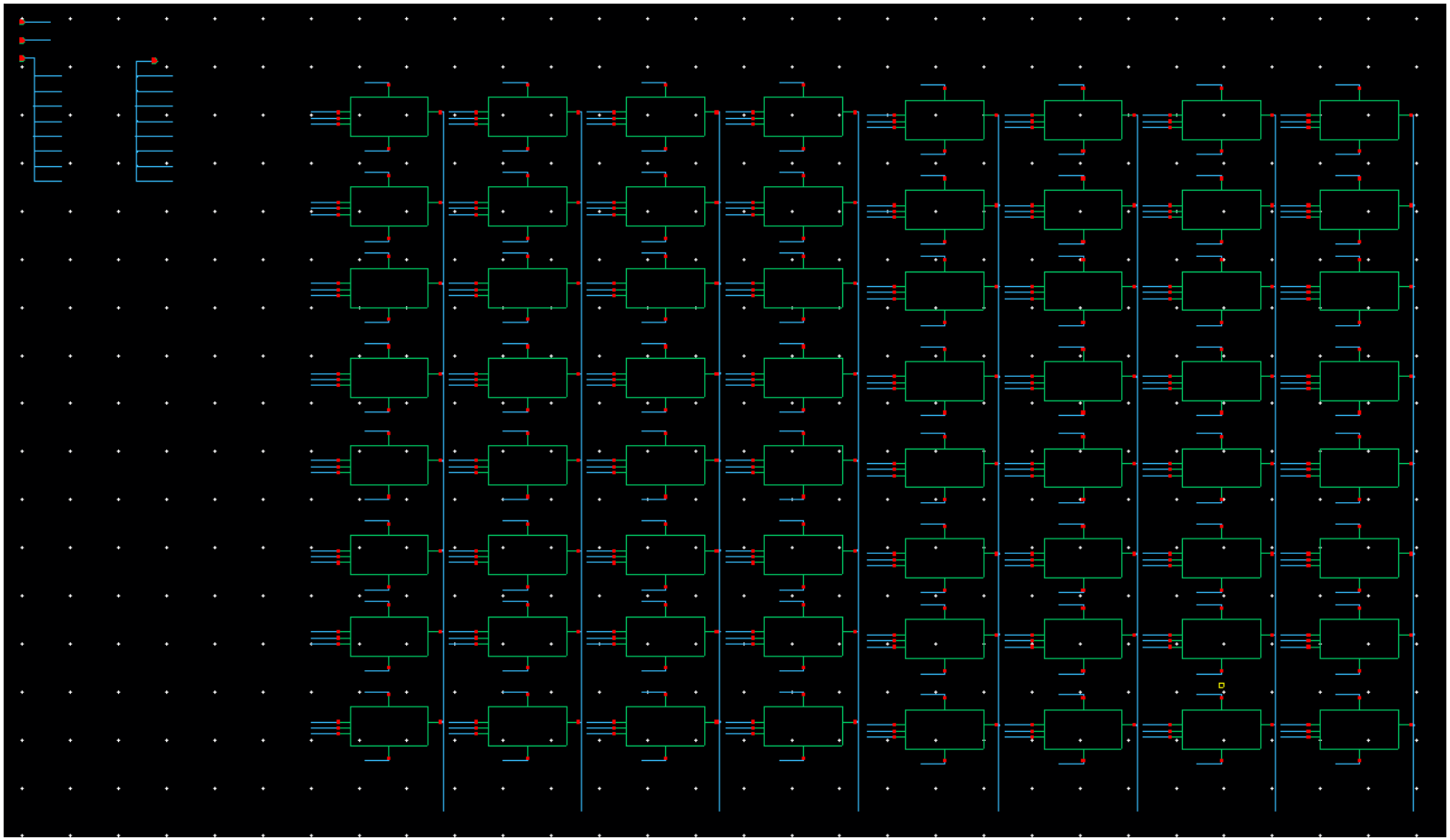


Active Pixel Cell (APS)

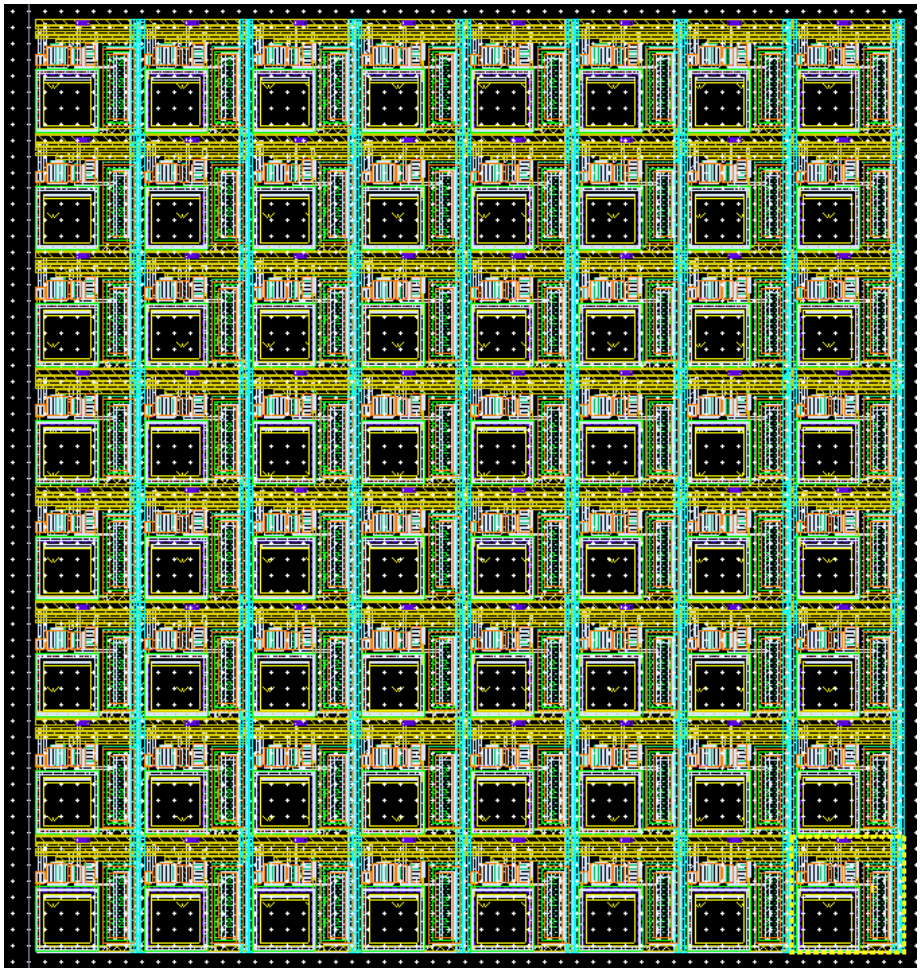
Schematic and Post Layout Simulation (Light)

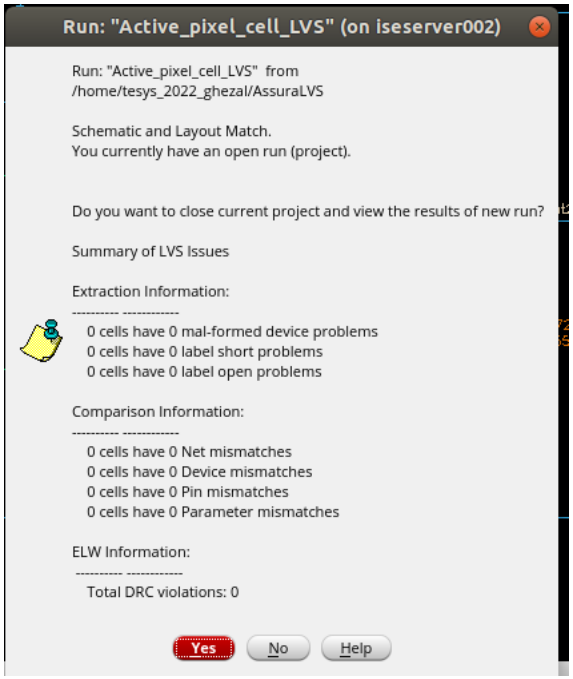


Active Pixel 8x8 Matrix
Schematic



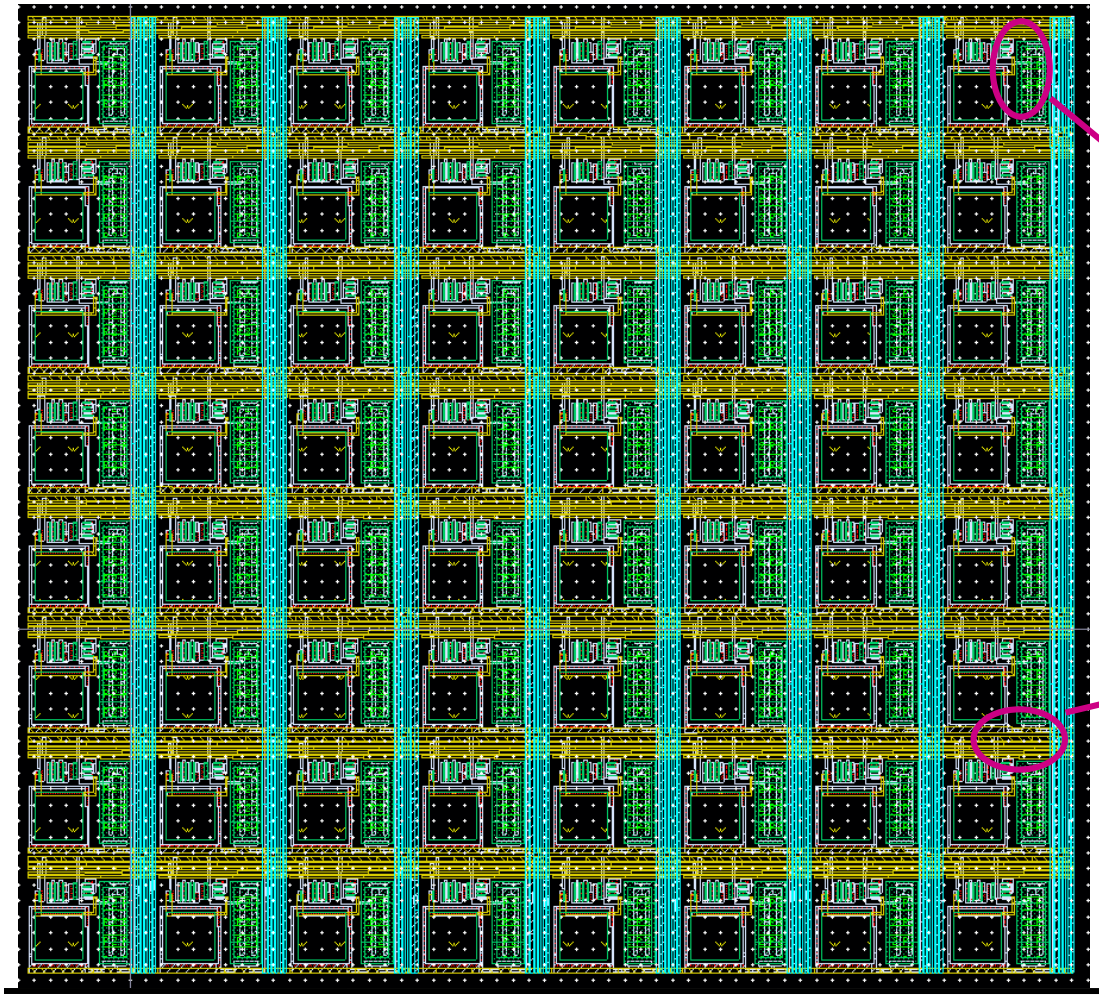
Active Pixel 8x8 Matrix
Layout

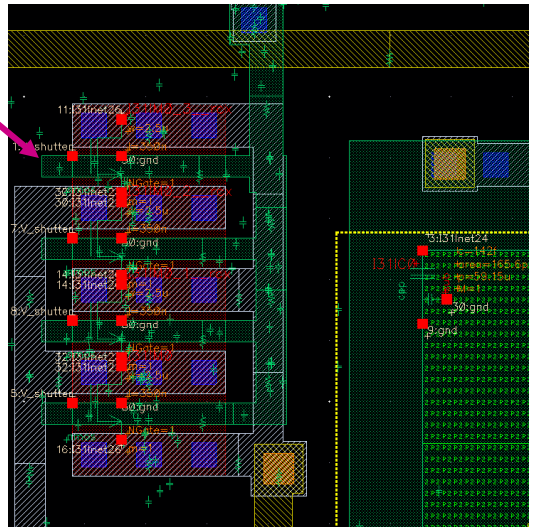


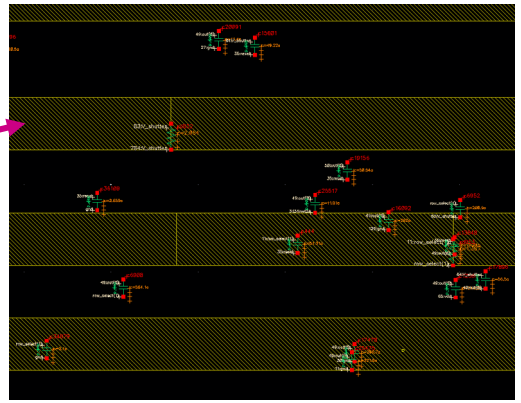


Active Pixel 8x8 Matrix

Post Layout

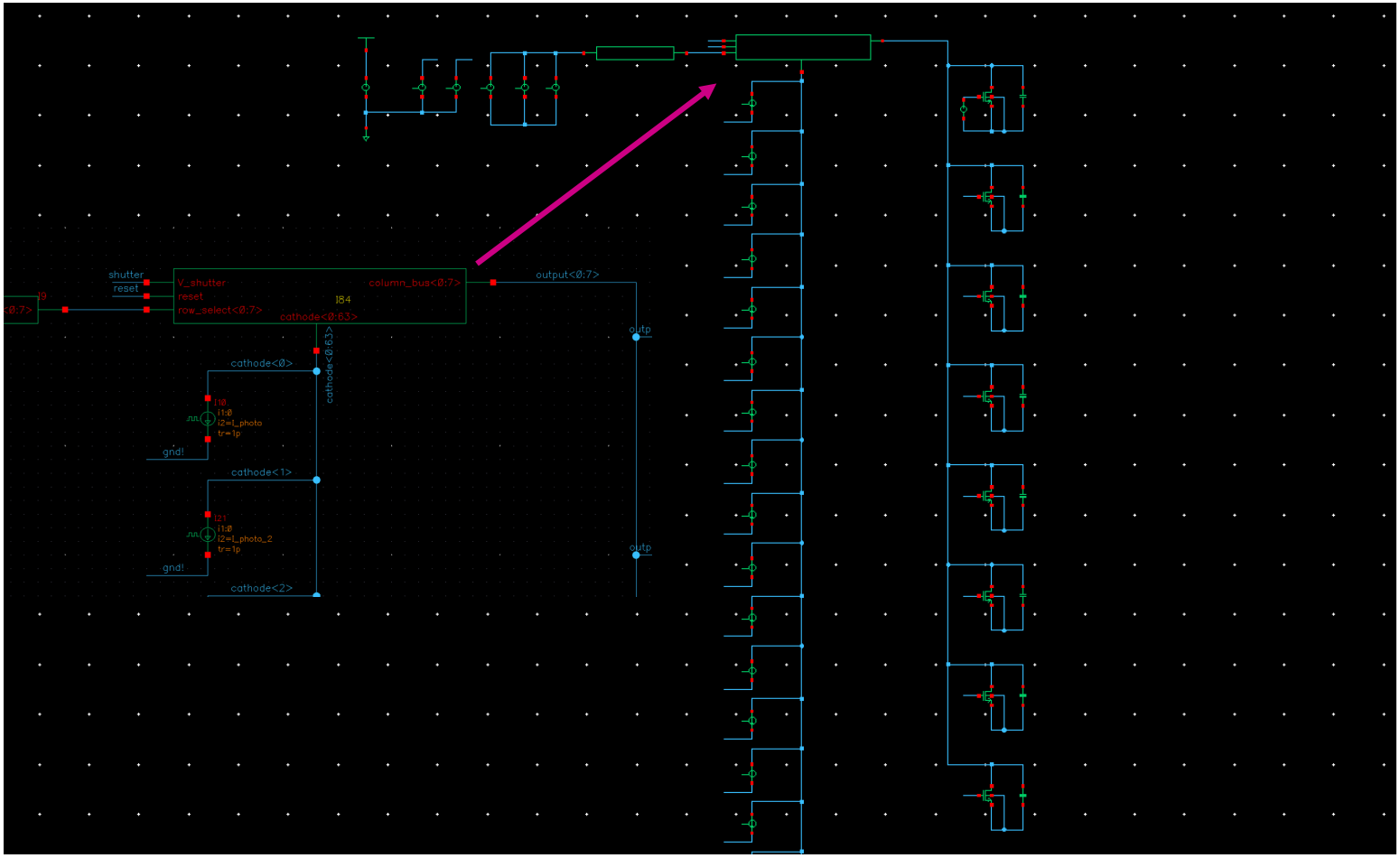




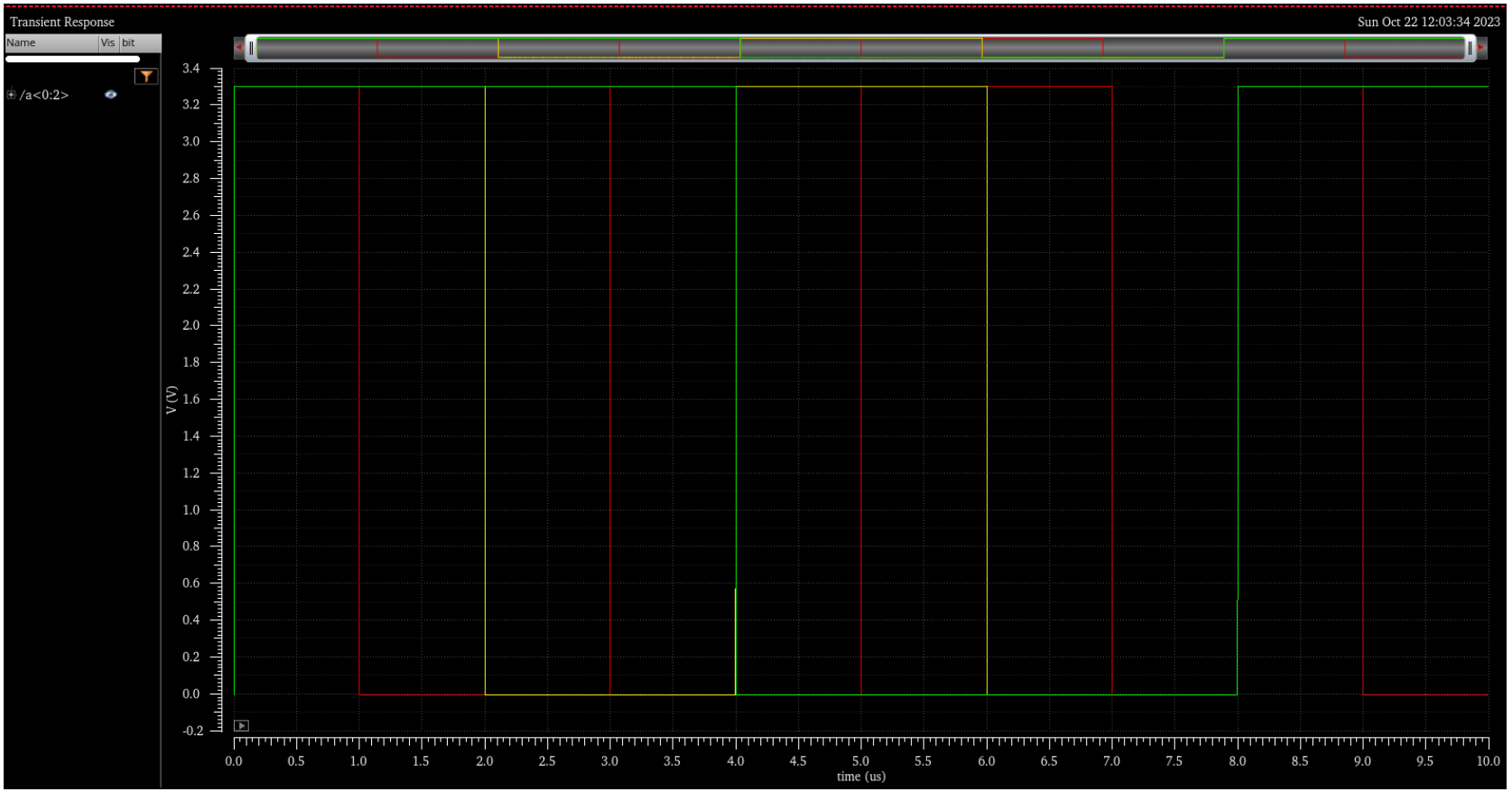


Active Pixel 8x8 Matrix

Test Bench

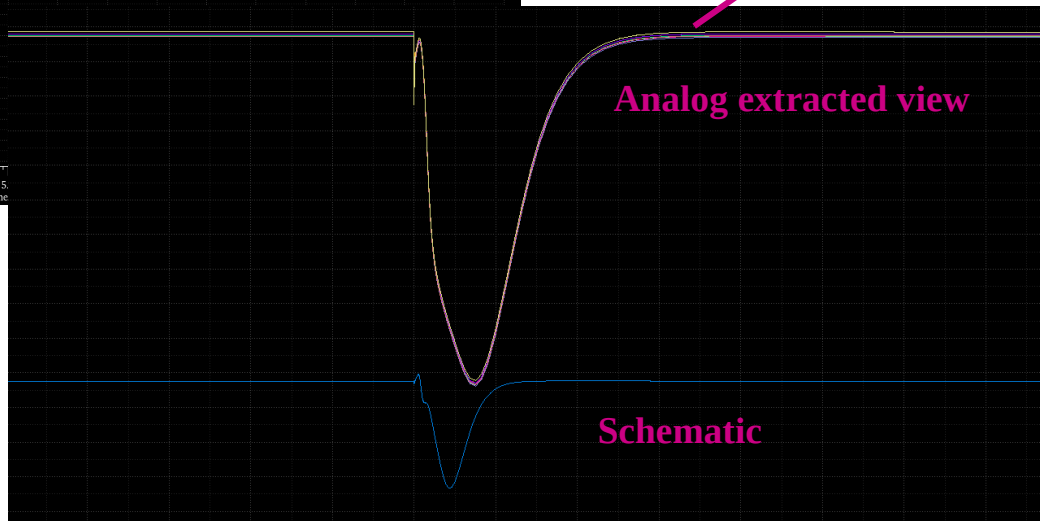


Active Pixel 8x8 Matrix
Simulation (Inputs)



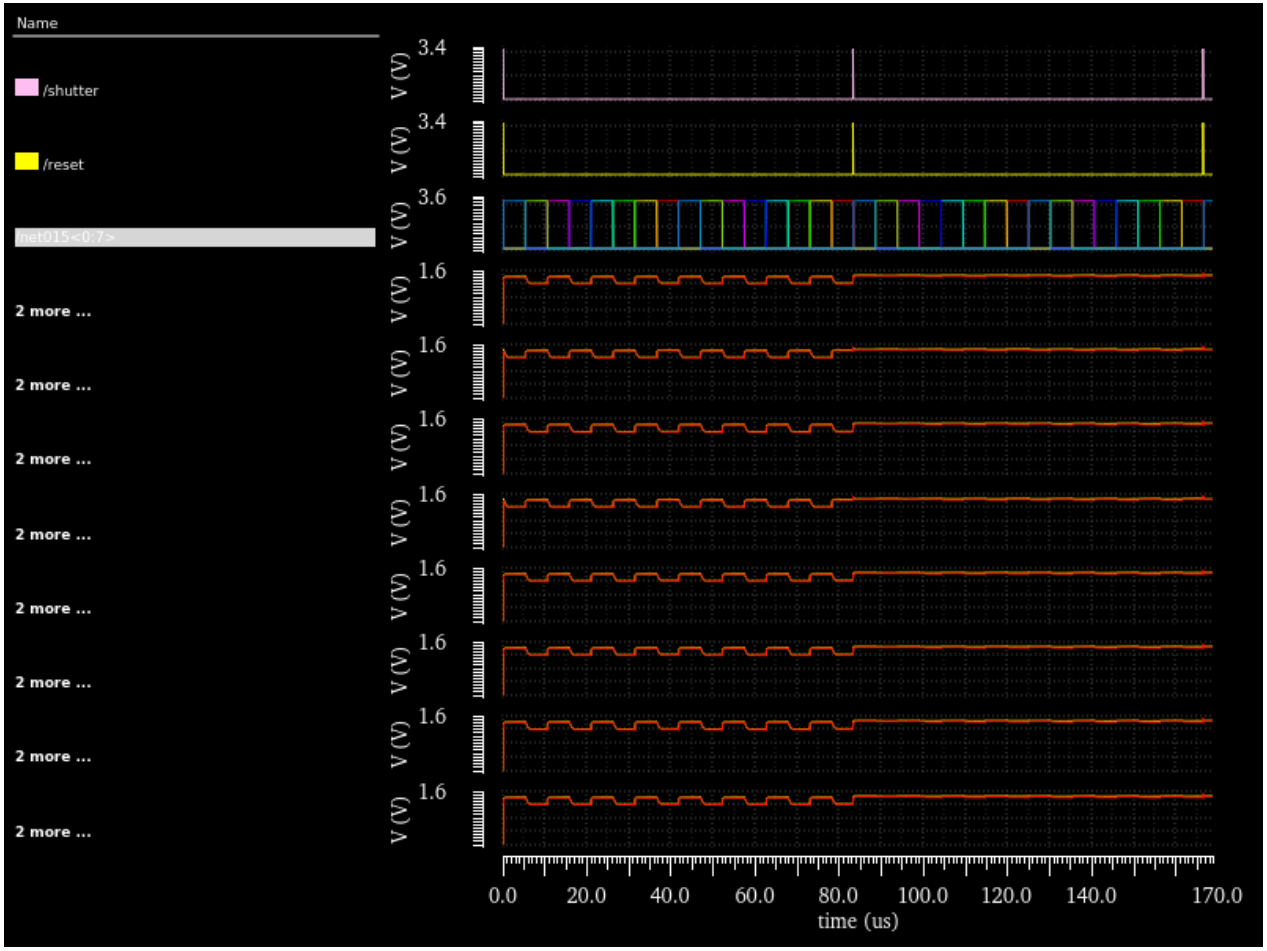
Active Pixel 8x8 Matrix

Schematic and Post Layout Simulation (Dark)



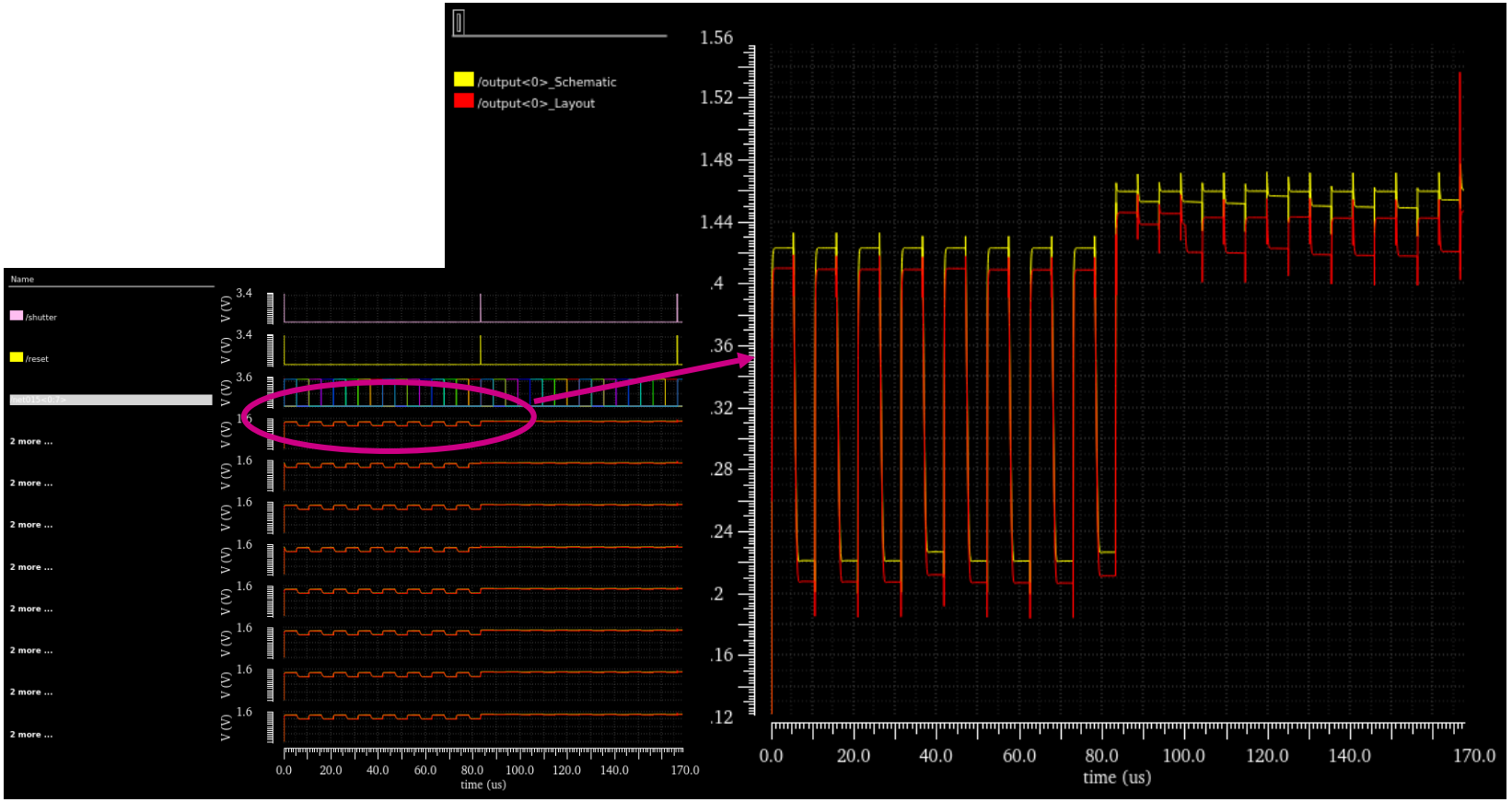
Active Pixel 8x8 Matrix

Schematic and Post Layout Simulation (Light)

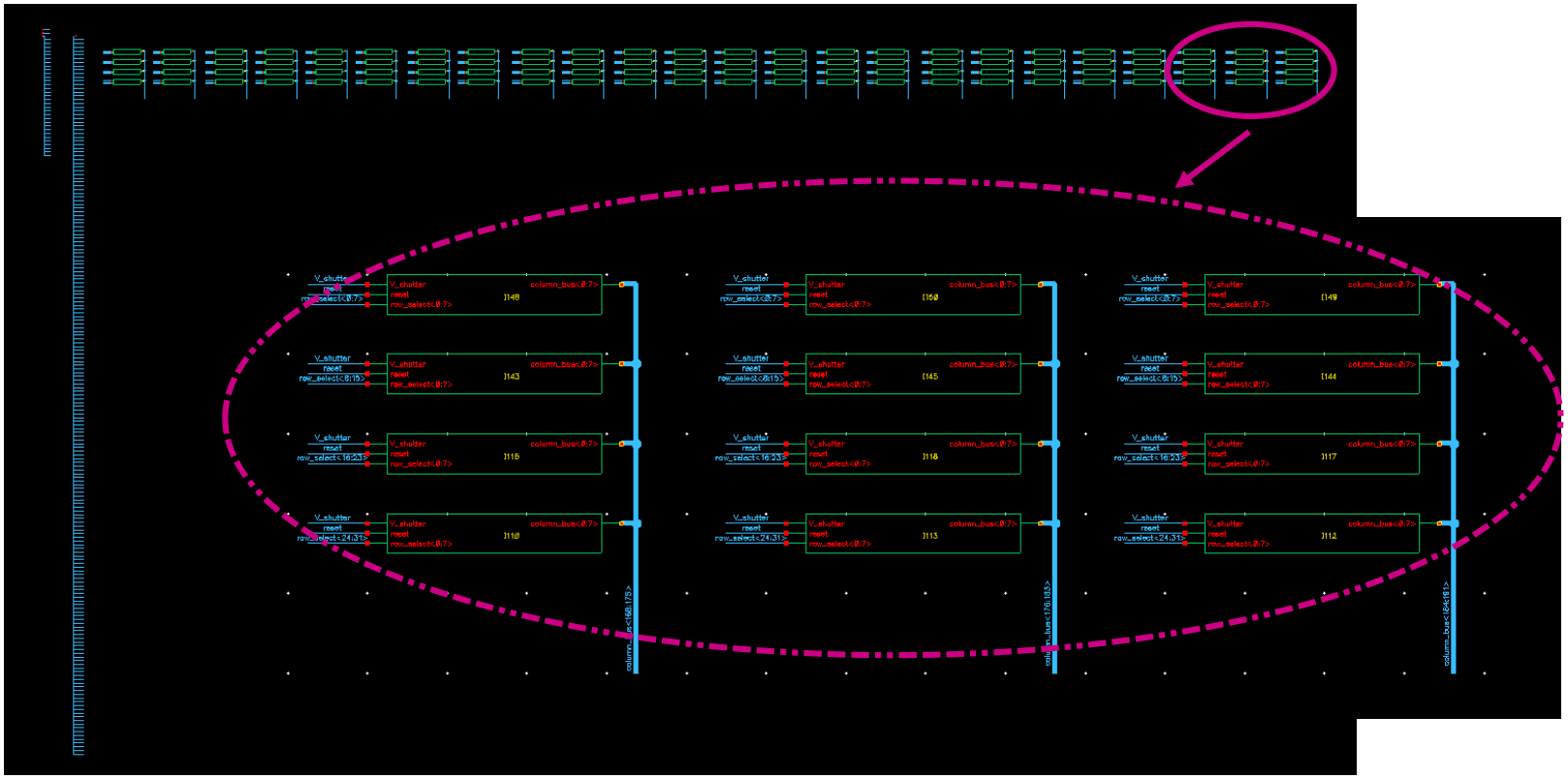


Active Pixel 8x8 Matrix

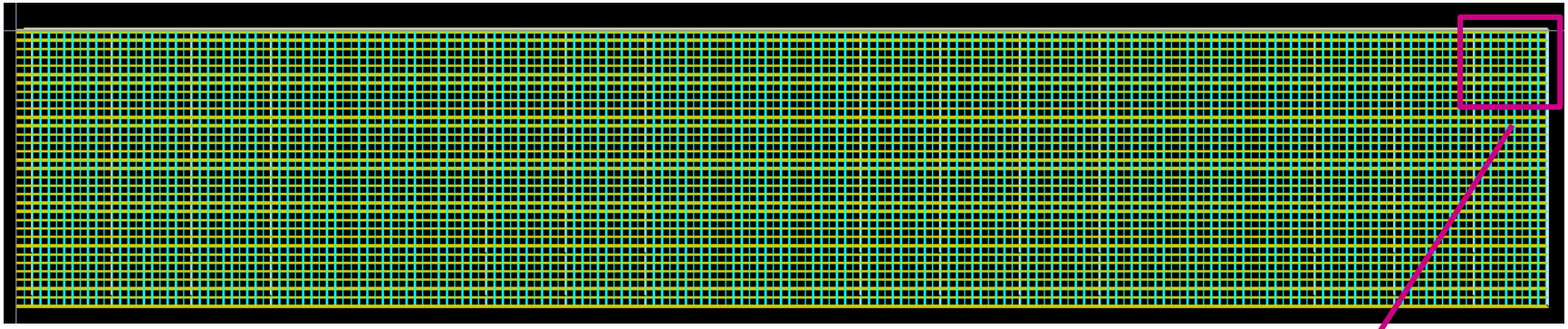
Schematic and Post Layout Simulation (Light)

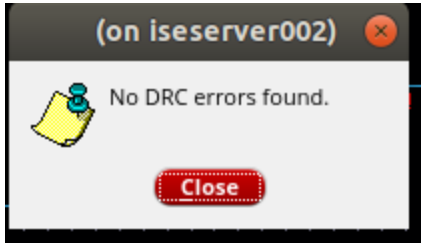


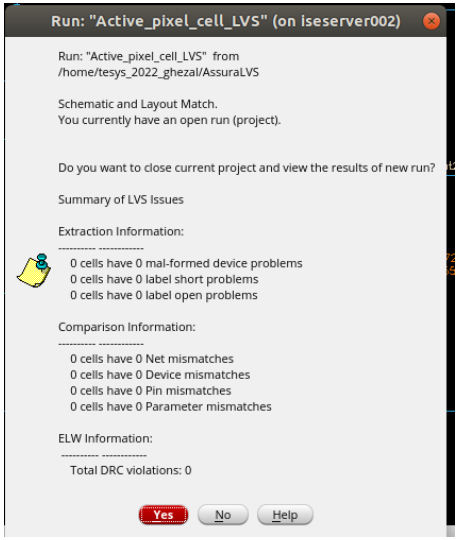
Active Pixel 192x32 Matrix
Schematic

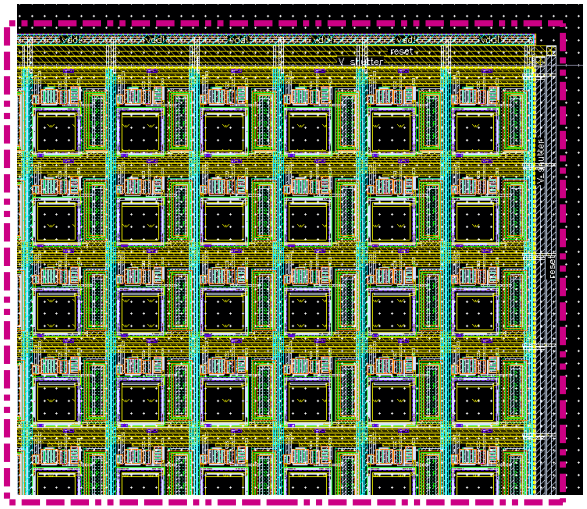


Active Pixel 192x32 Matrix
Layout

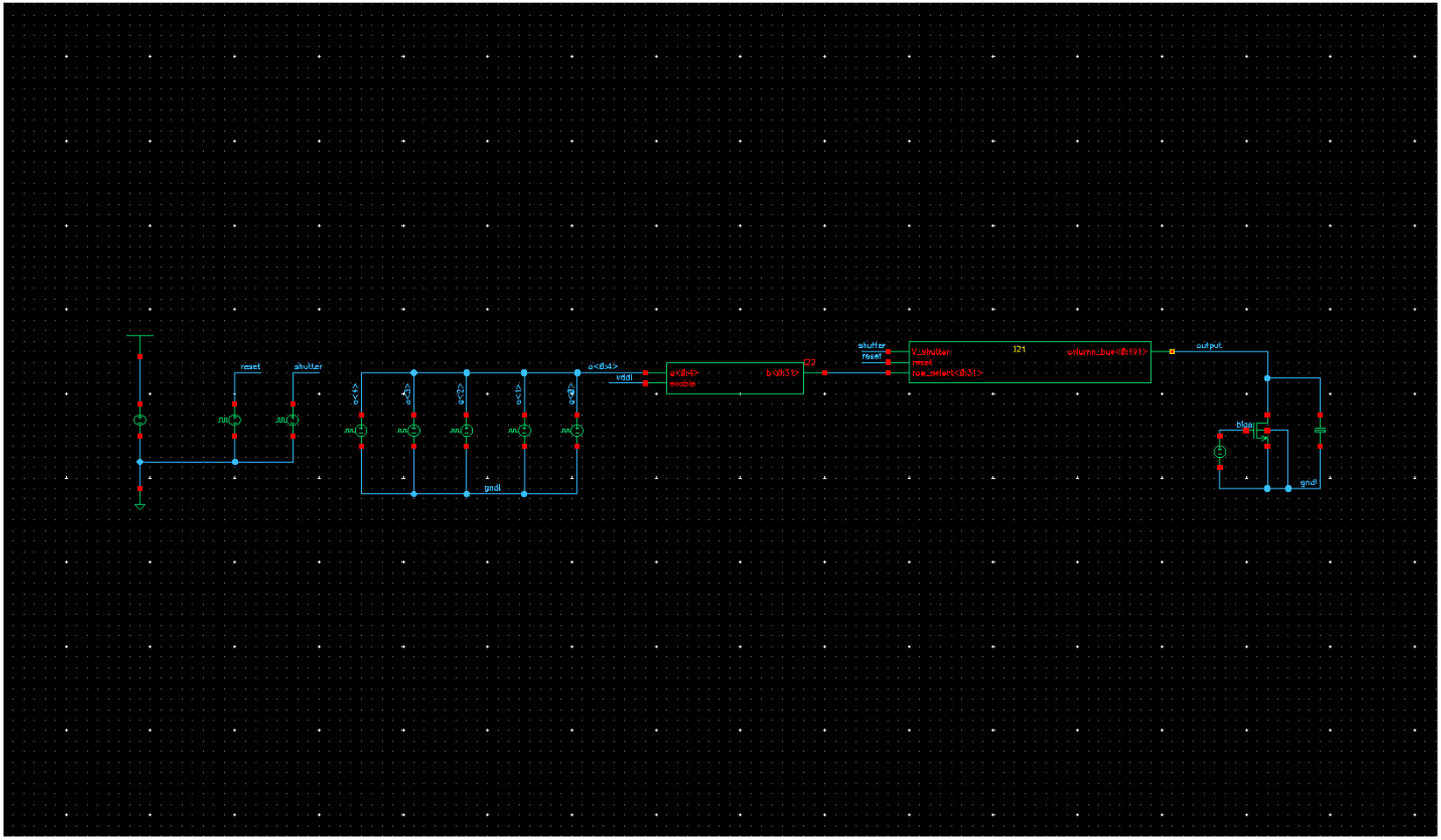






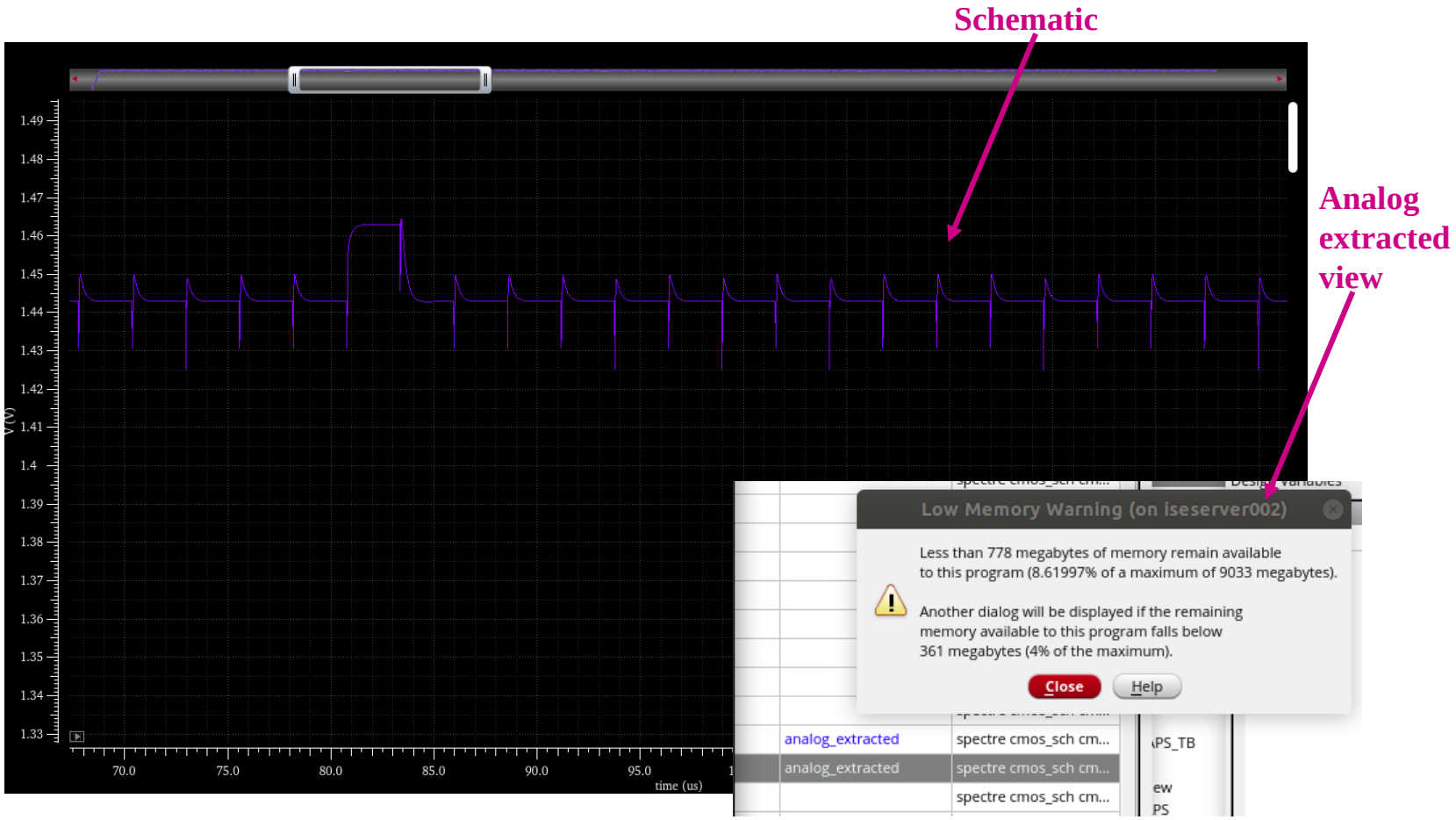


Active Pixel 192x32 Matrix
Test Bench

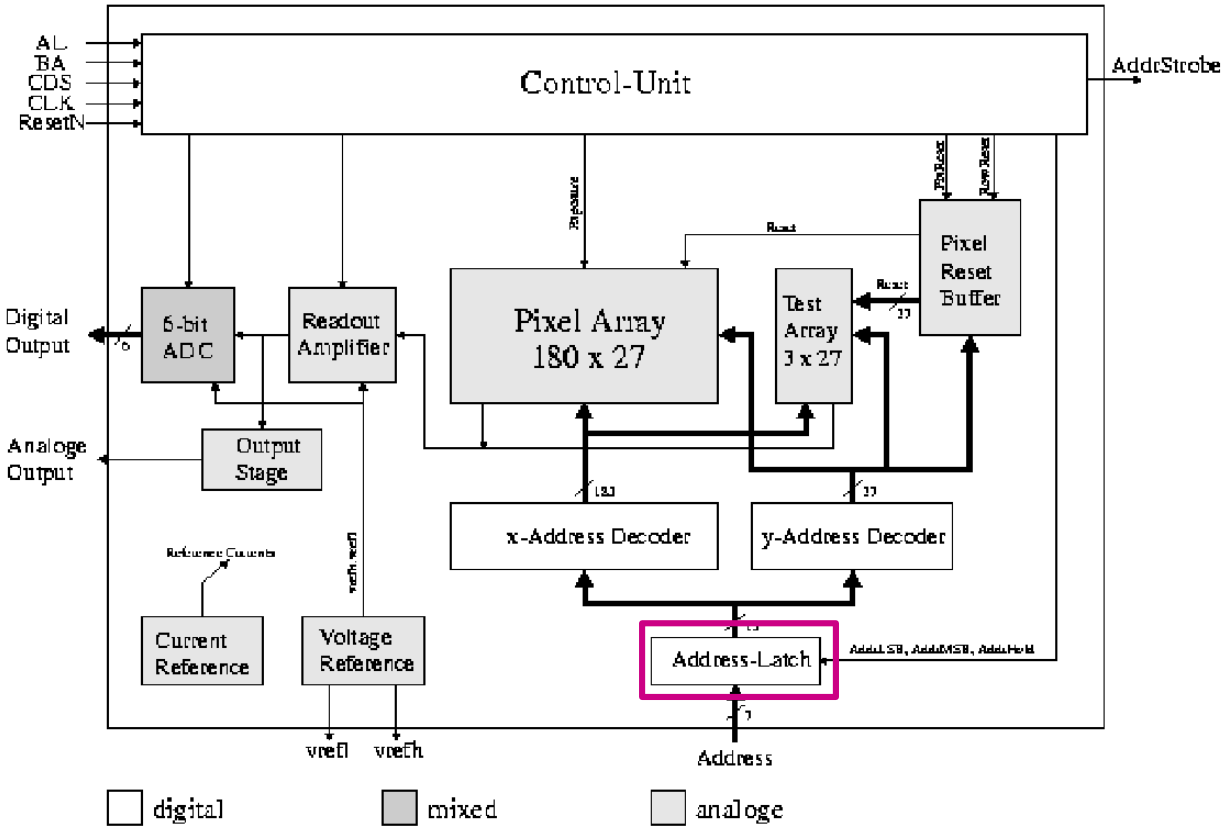


Active Pixel 192x32 Matrix

Schematic and Post Layout Simulation

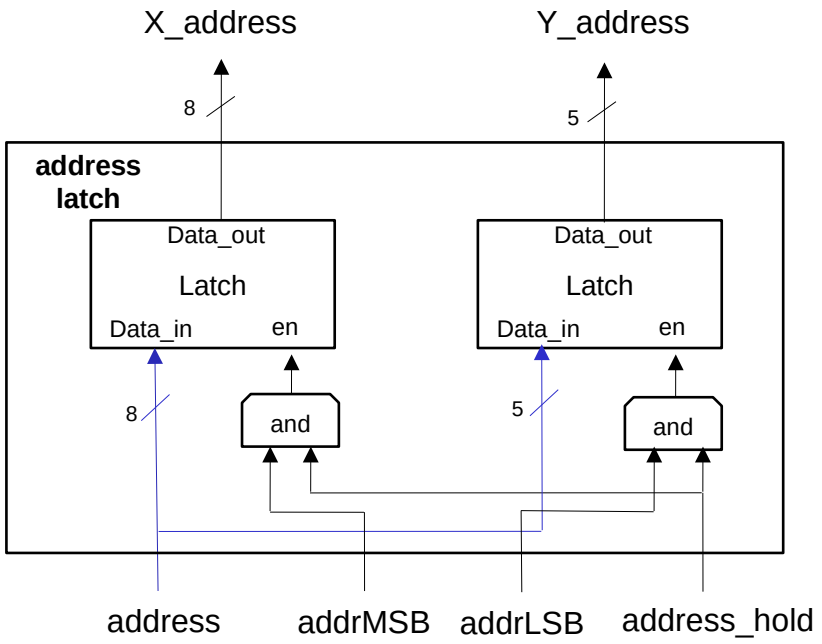


Address latch
Overview



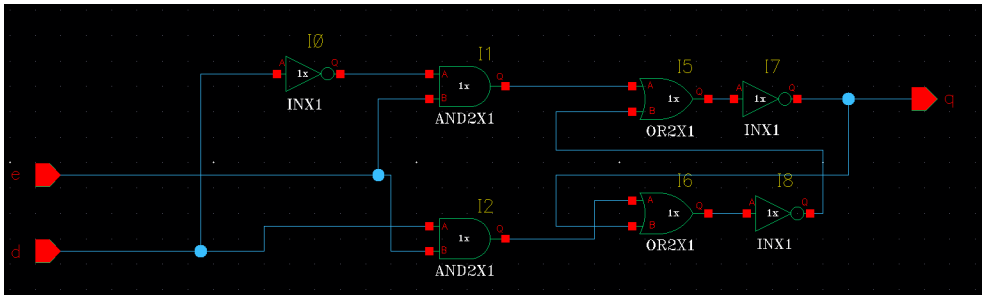
Address latch

- The goal of this part of the circuit is to retain the values of the column and row.
- This section is divided into two subsections: 1-bit latch and Address latch.

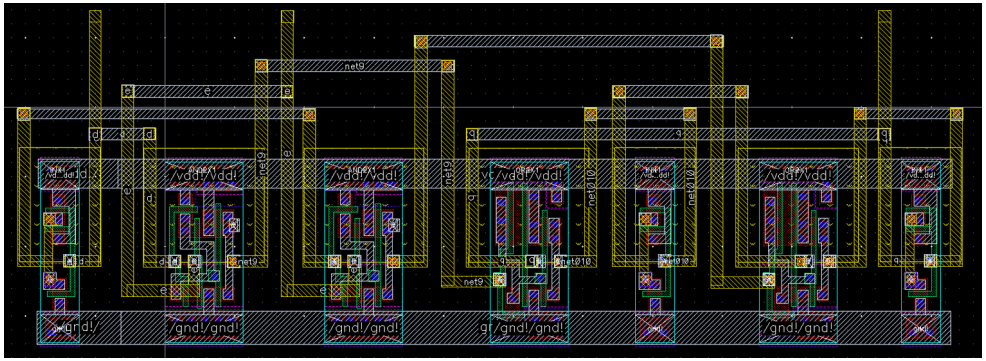


Address latch
1 bit latch

Schematic

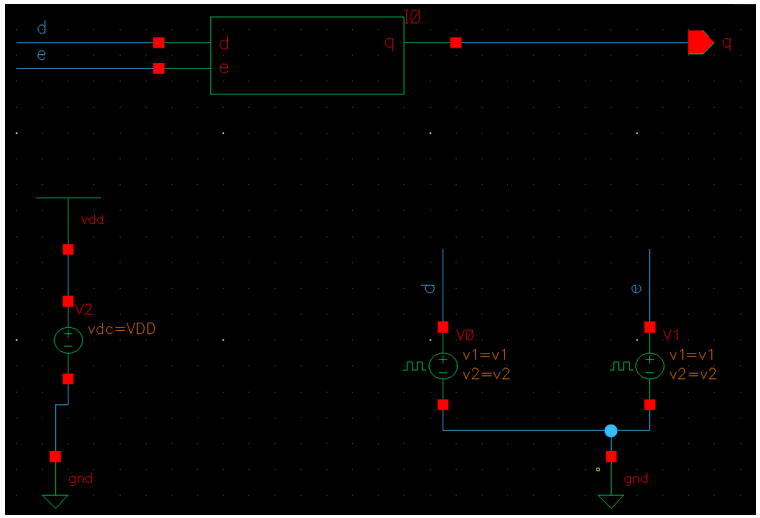


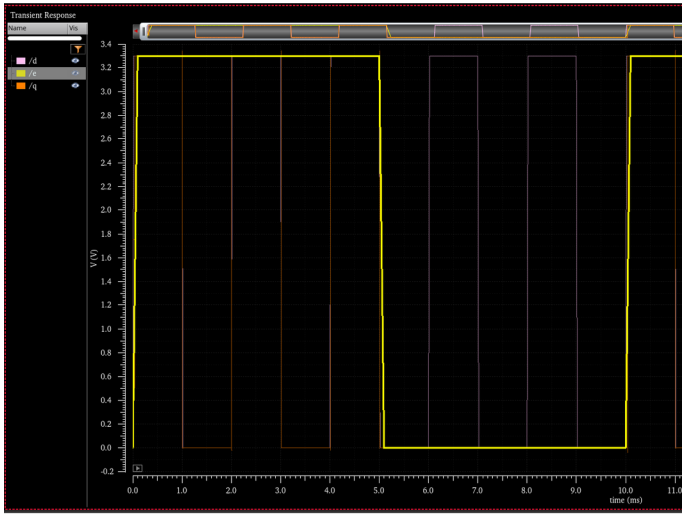
Layout



Address latch
1 bit latch

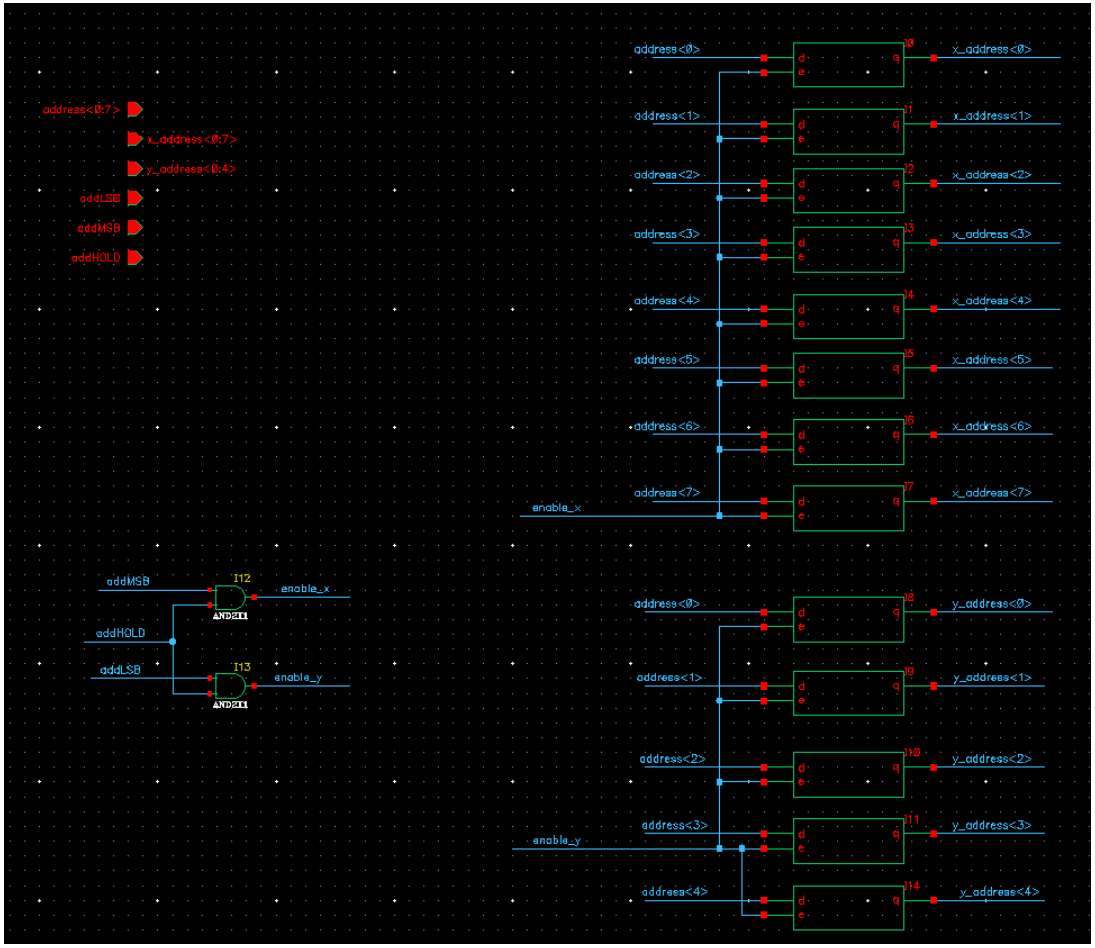
- The simulation shows that if 'e' is '1', the value ‘d’ is stored in 'q'. However, if 'e' is '0', the value 'q' is kept.





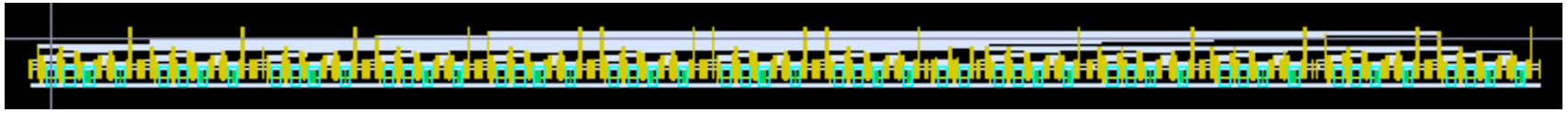
Address latch

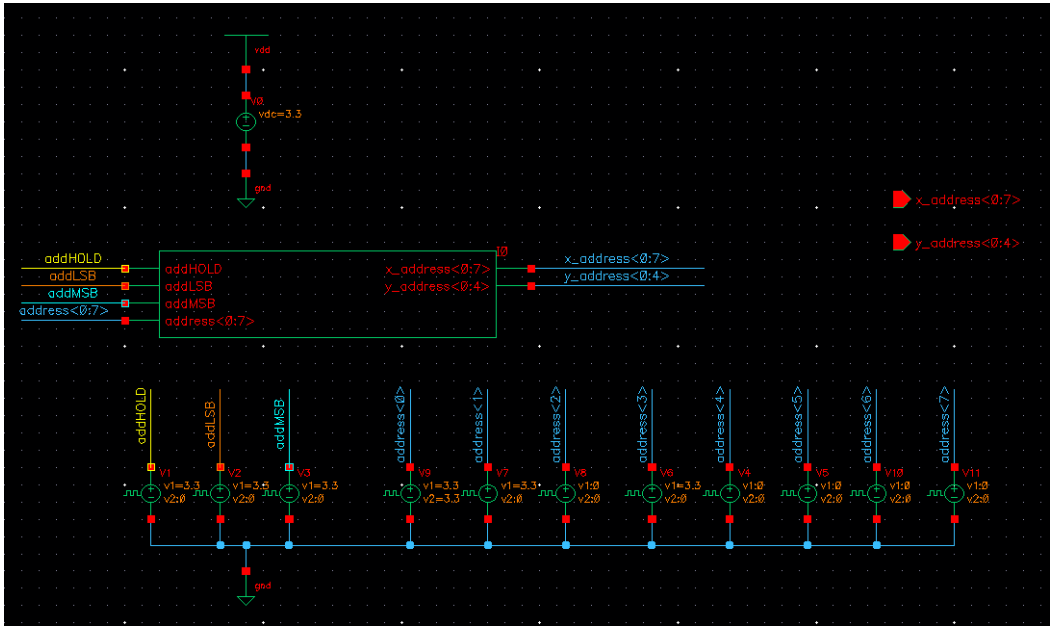
Address latch - Schematic



Address latch

Address latch – Layout and test bench

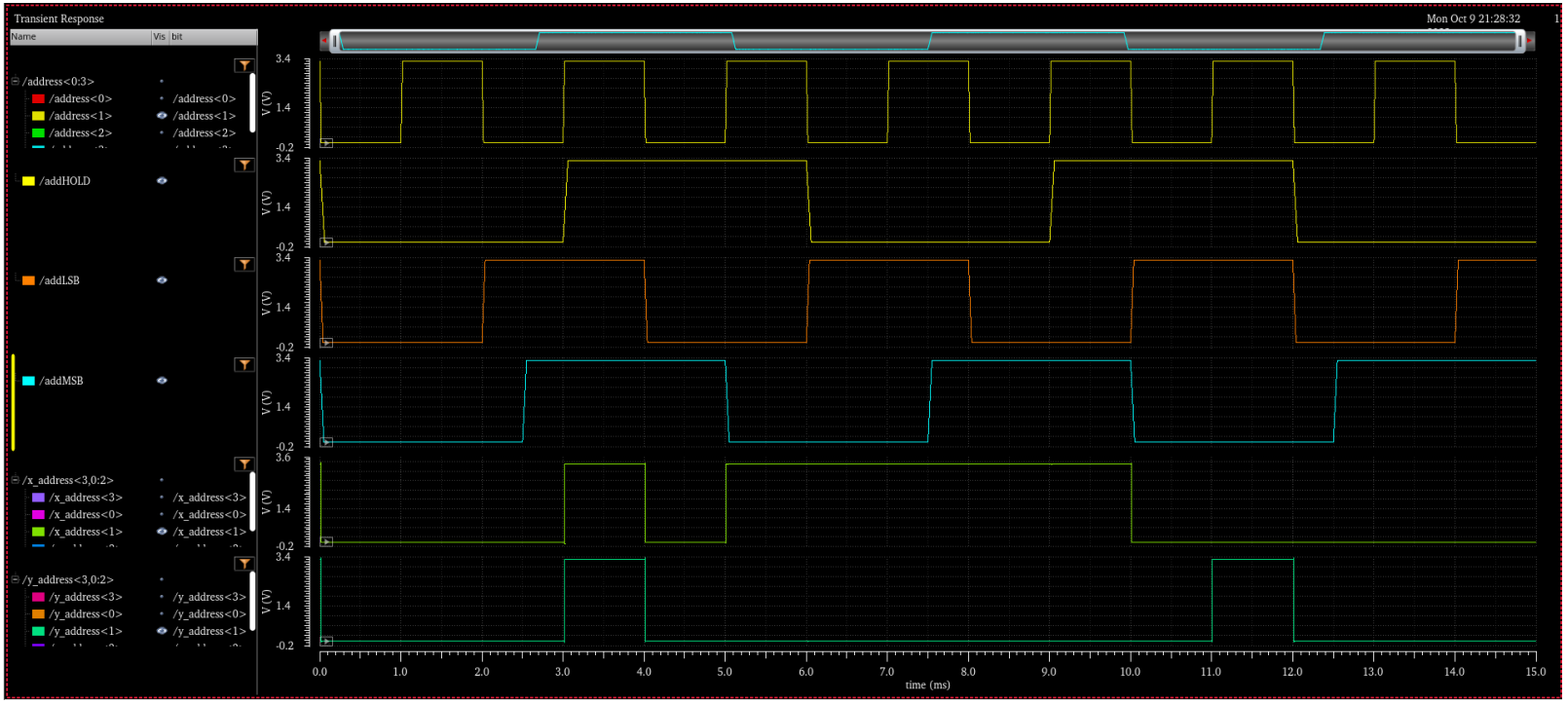




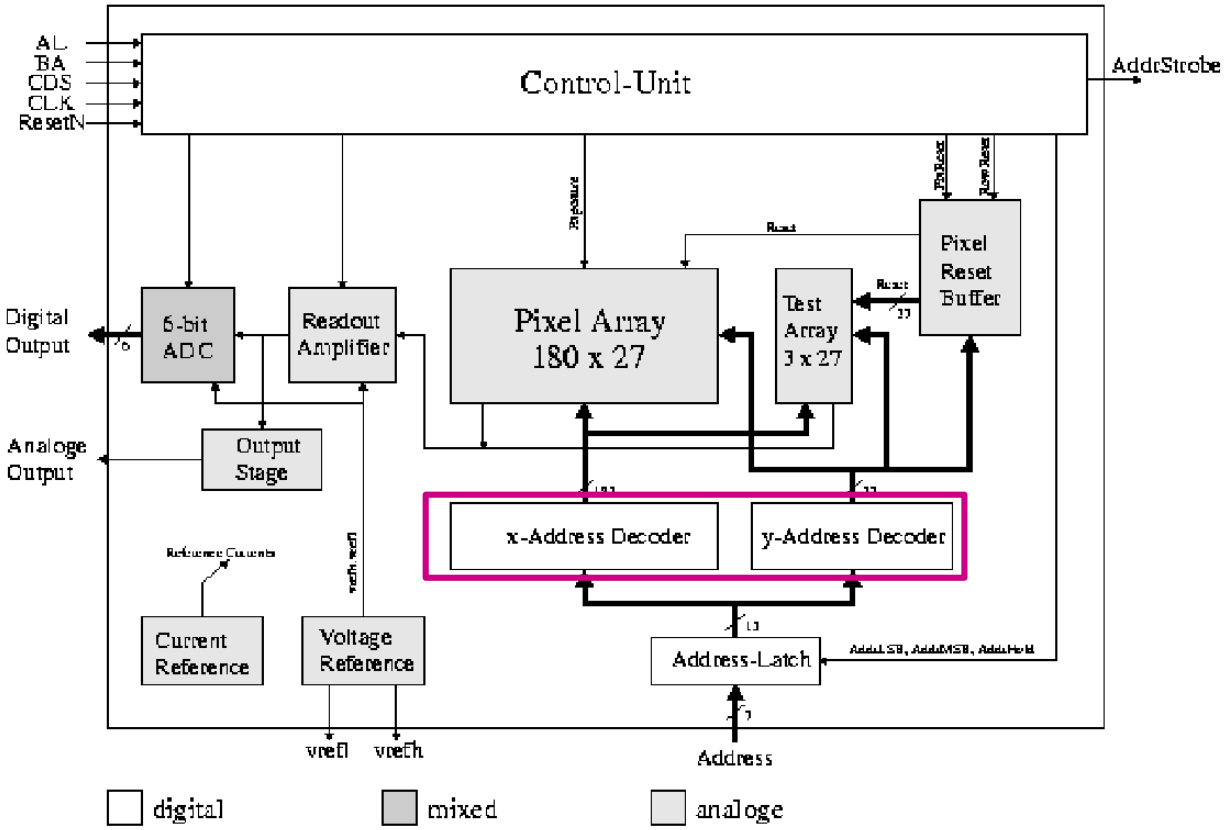
Address latch

Address latch – Post Layout Simulation

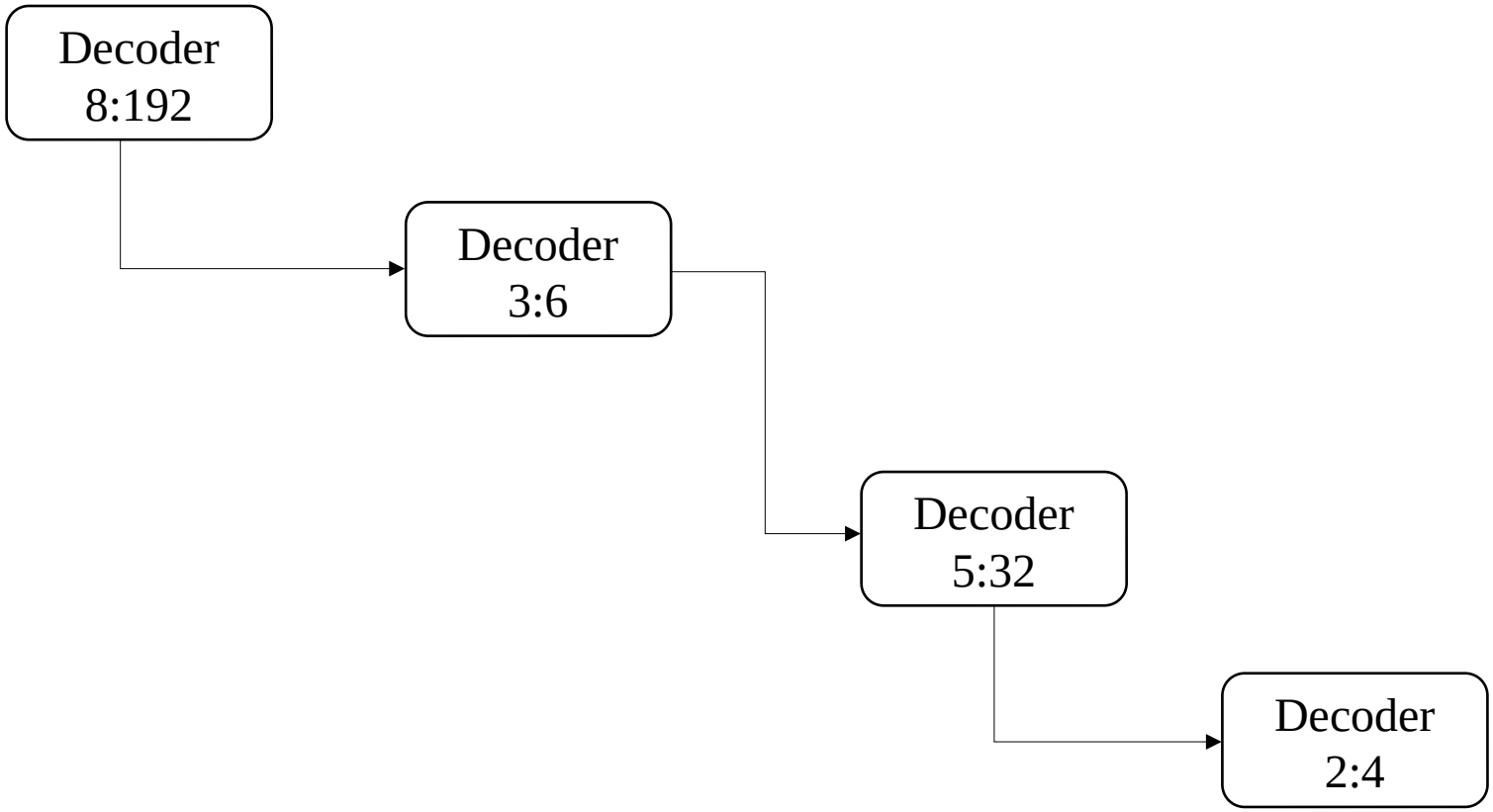
- The simulation shows that if ‘addHold’ and addLSB are '1', the value ‘address’ is stored in ‘y_address’. Moreover, if ‘addHold’ and addMSB are '1', the value ‘address’ is stored in ‘x_address’.



Decoder
Overview

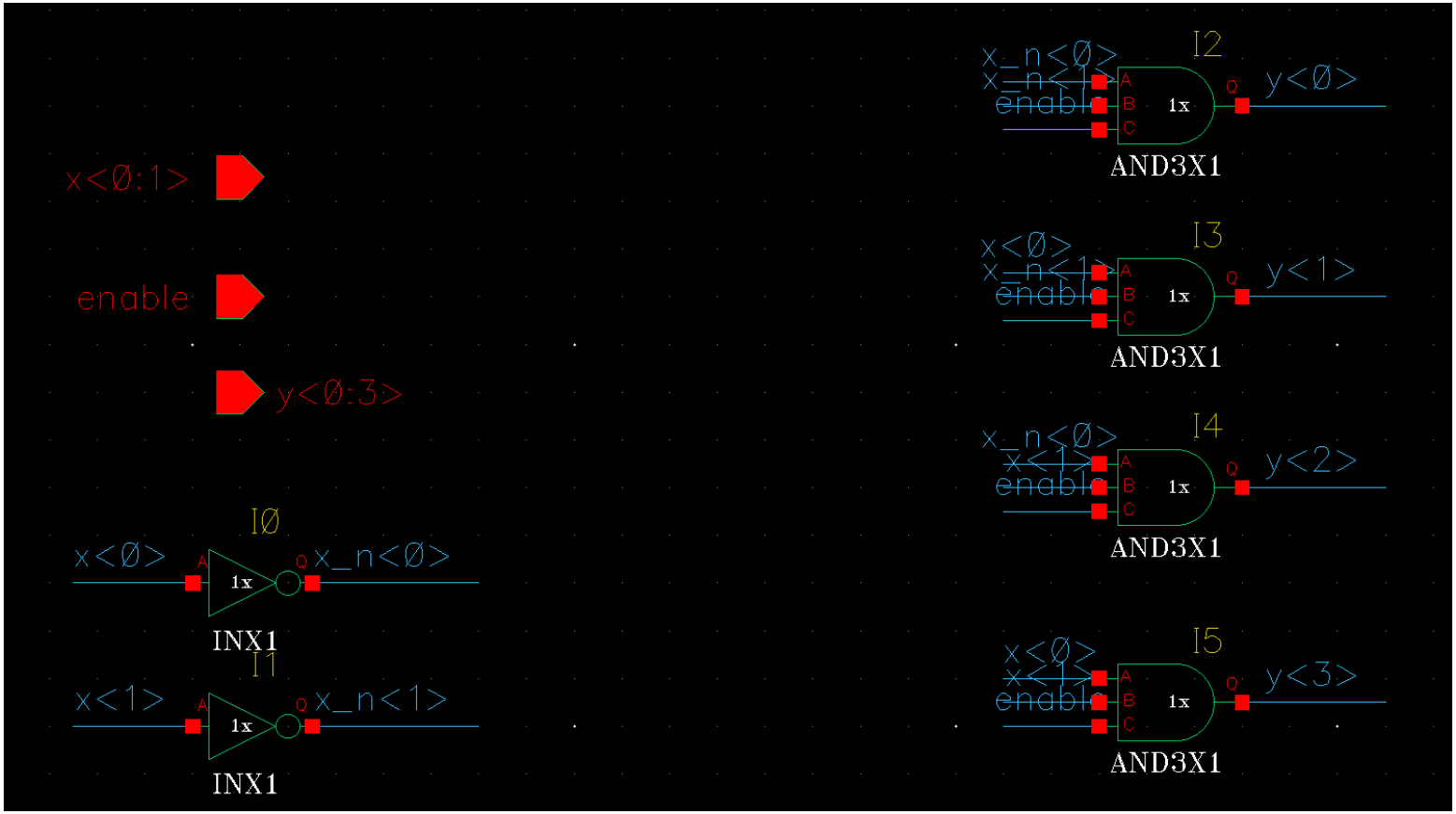


Decoder



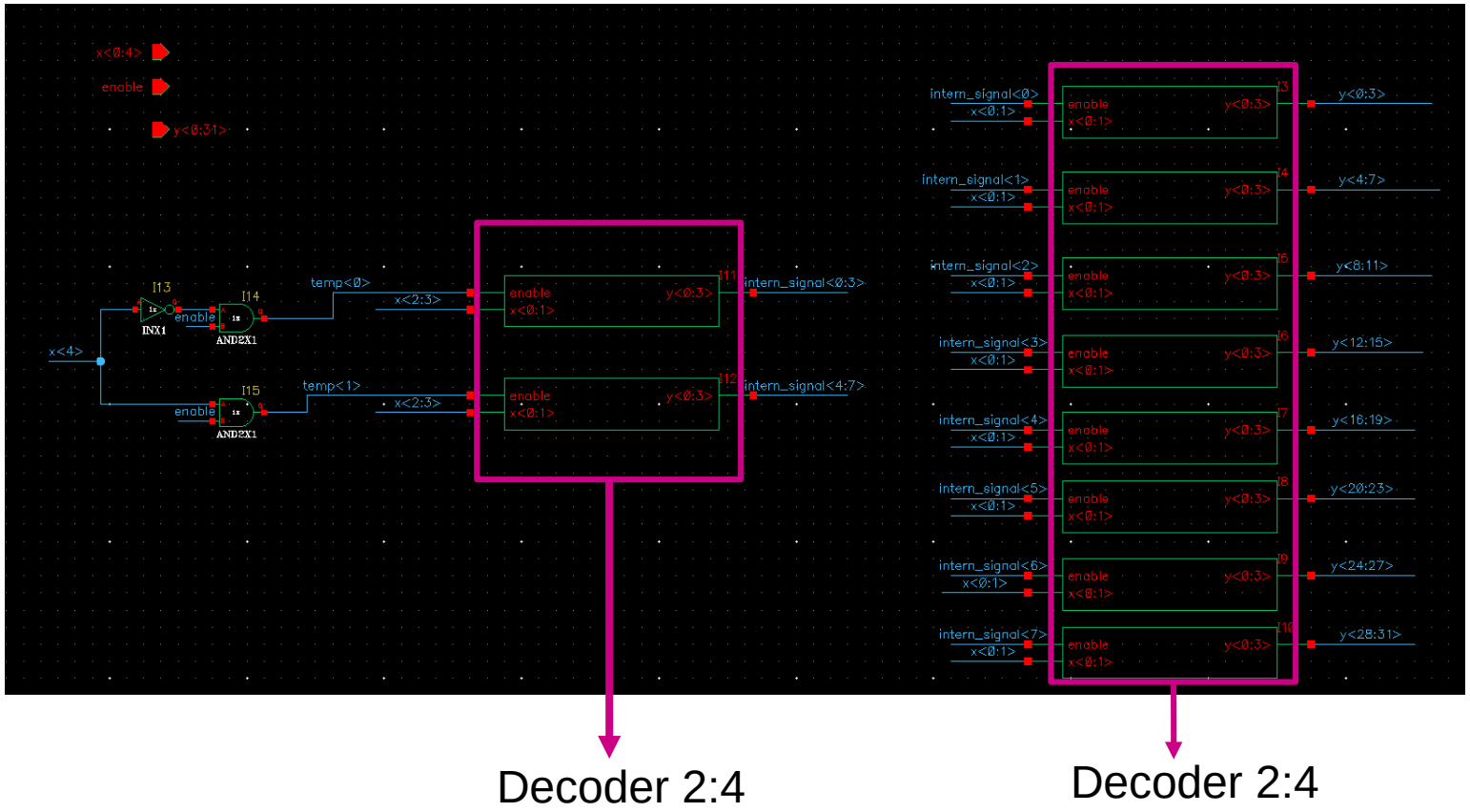
Decoder

Decoder 2:4 – Schematic



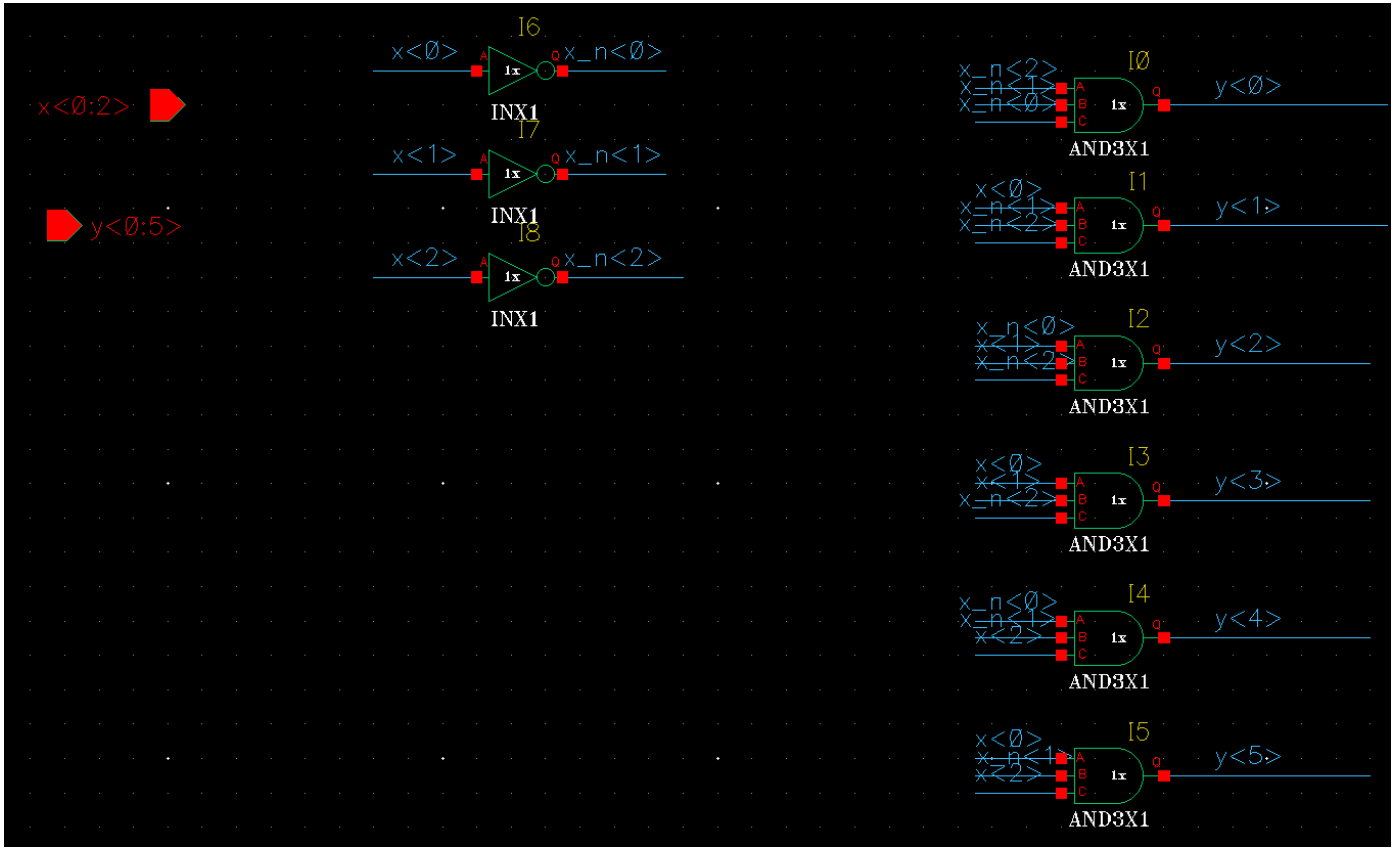
Decoder

Decoder 5:32 – Schematic



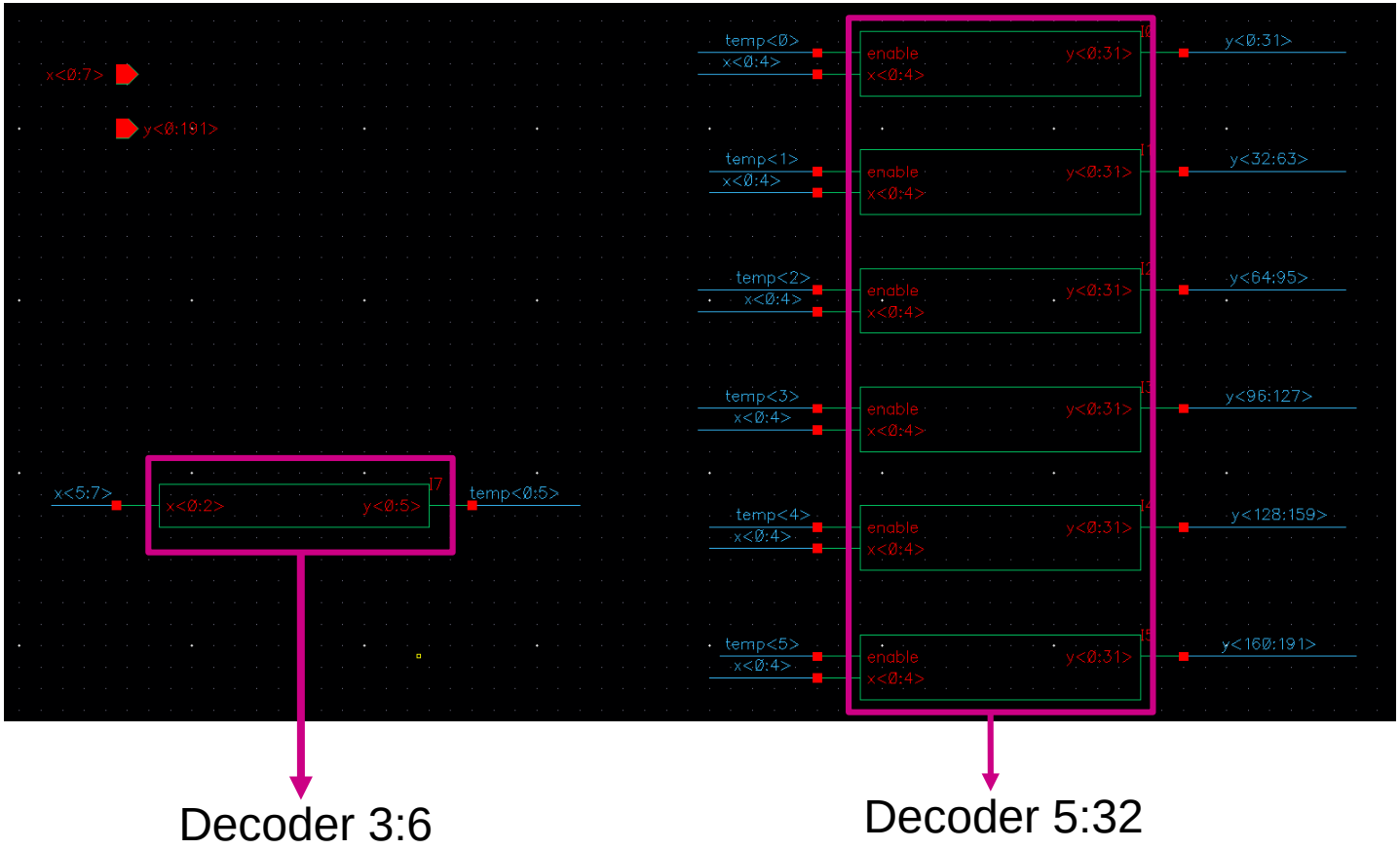
Decoder

Decoder 3:6 – Schematic



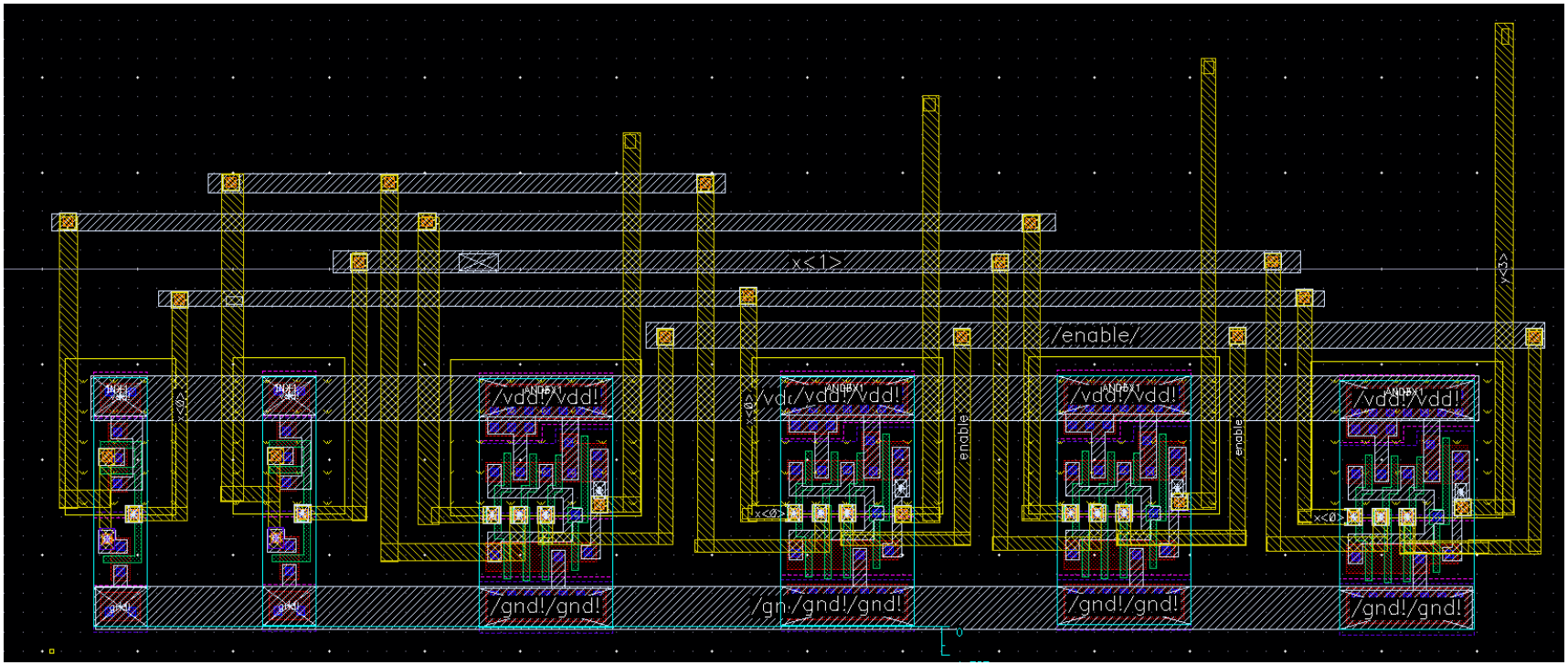
Decoder

Decoder 8:192 – Schematic



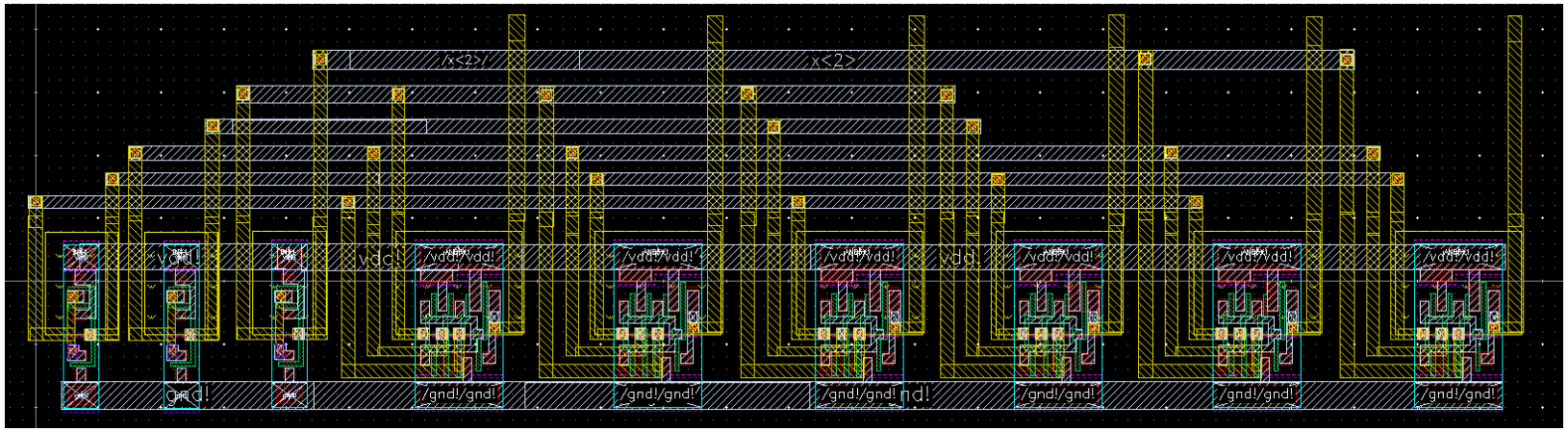
Decoder

Decoder 2:4 – Layout



Decoder

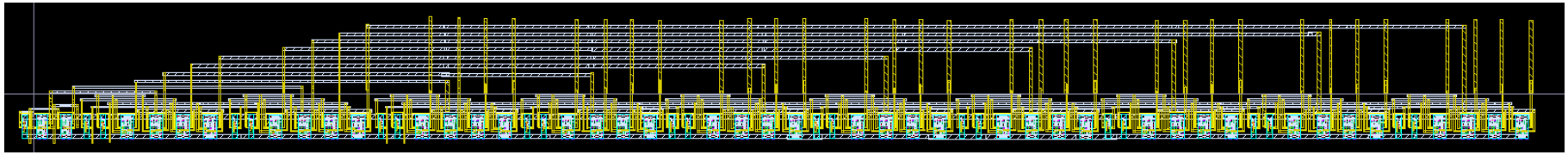
Decoder 3:6 – Layout



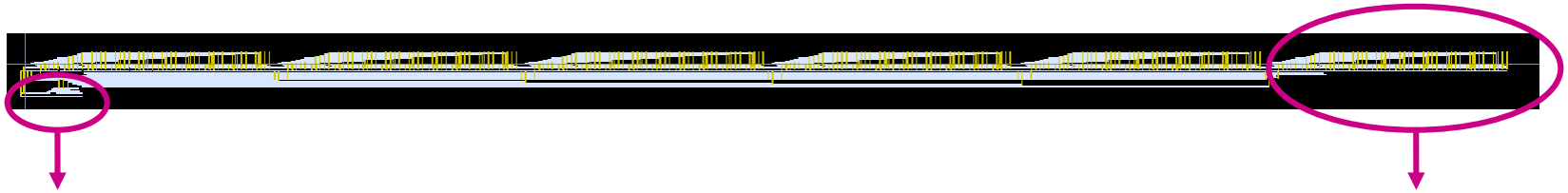
Decoder

Decoder 5:32 , Decoder 8:192 – Layout

Decoder 5:32



Decoder 8:192

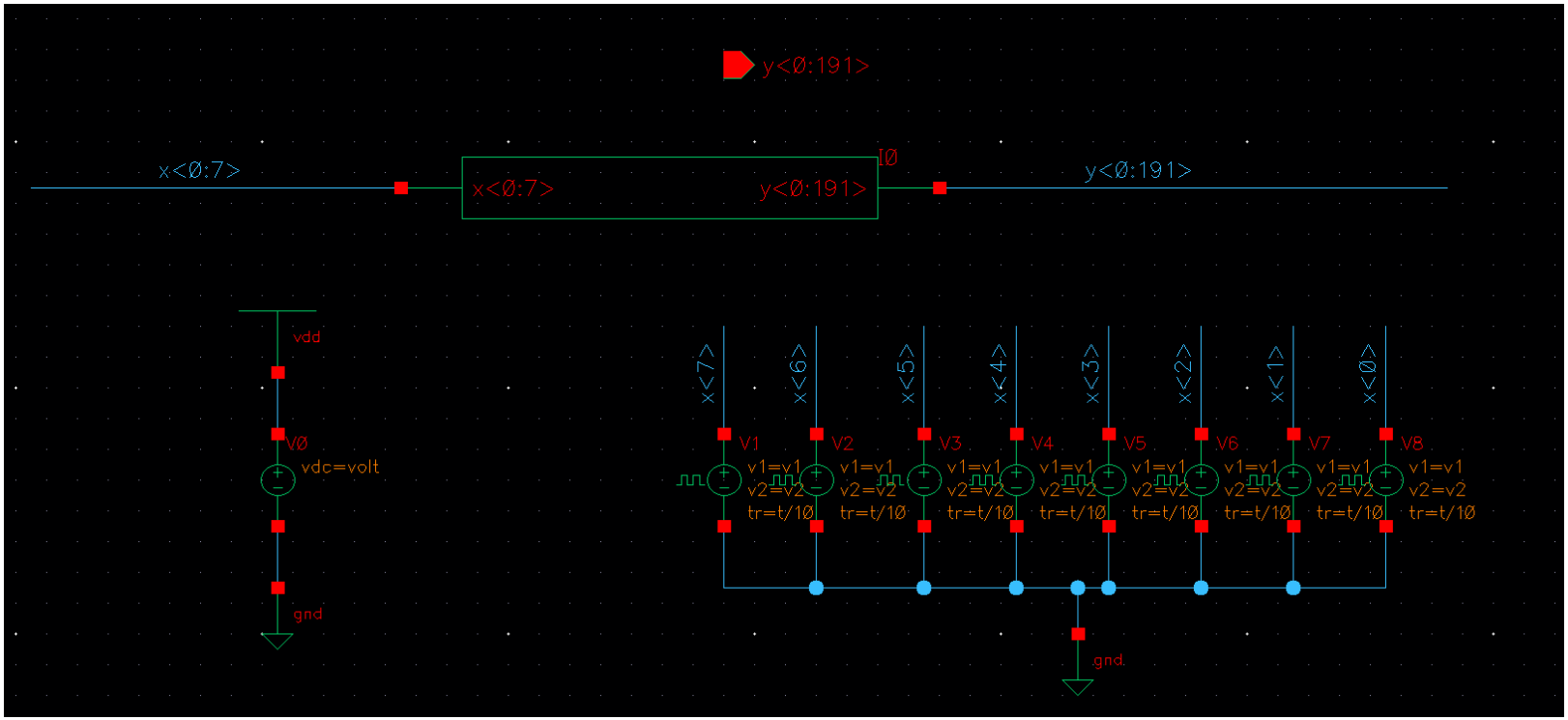


Decoder 3:6

Decoder 5:32

Decoder

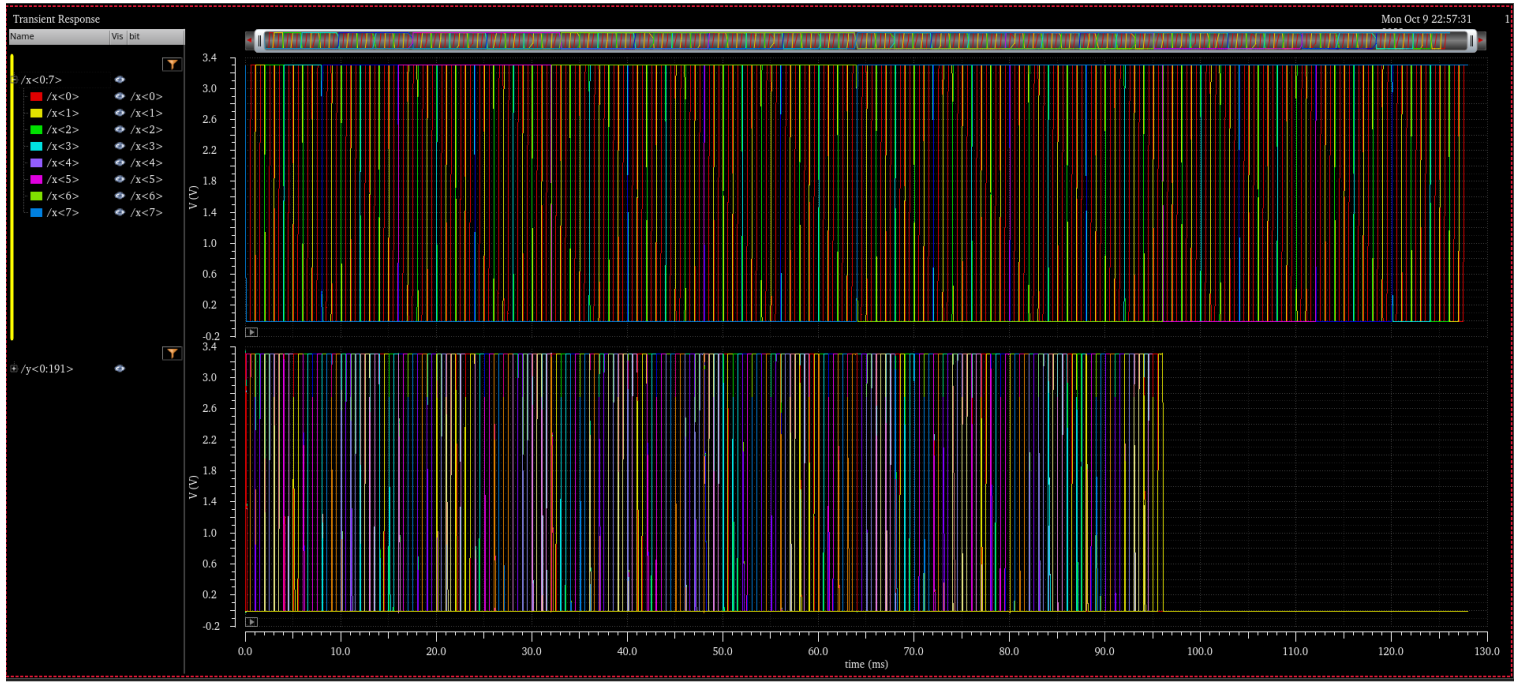
Decoder 8:192 – Test bench



Decoder

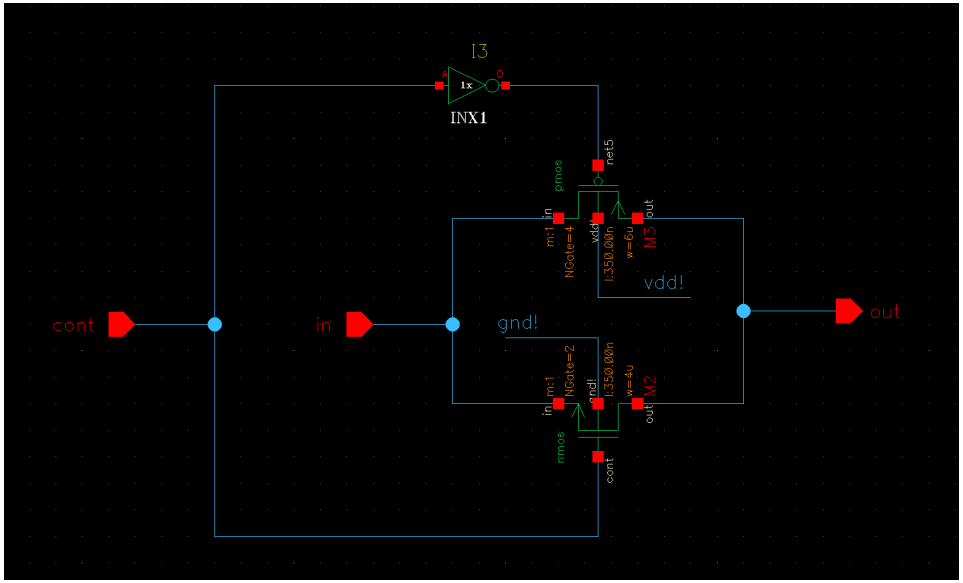
Decoder 8:192 – Post Layout Simulation

- We tried all possible combinations for the 8-bit input. The simulation shows that the decoder only responds if the input represents a number that is less than 192.



Design of Transmission gate

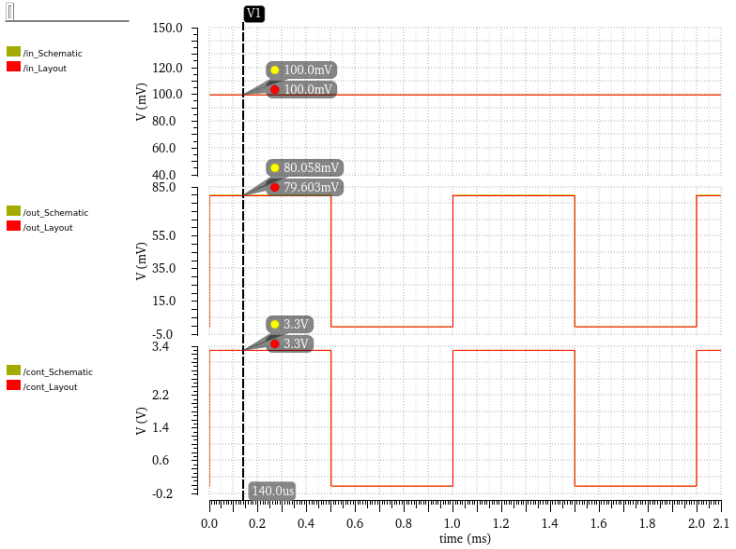
- With 'cont,' you can switch the output between 'in' and 'out.'
  - 'cont' = 1, there is a connection between 'in' and 'out';
  - 'cont' = 0, there is no connection between 'in' and 'out.

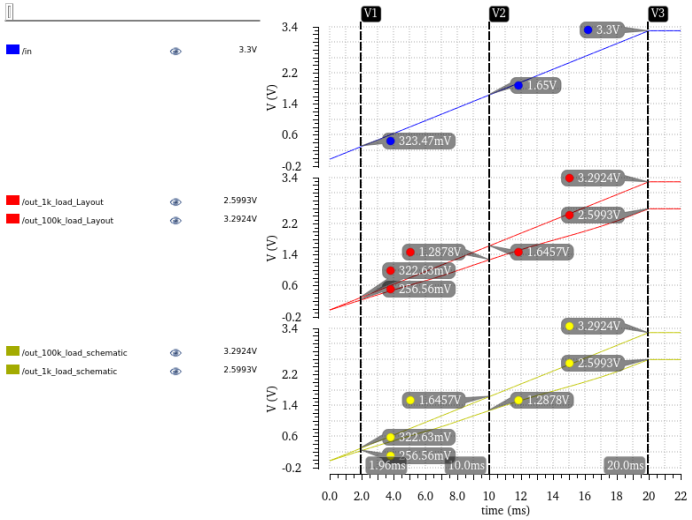


Transistor	Sizing
INVX(NMOS)	$\frac{1\,\mu m}{0.35\,\mu m}$
INVX(NMOS)	$\frac{2\,\mu m}{0.35\,\mu m}$
M2	$\frac{2\cdot 4\,\mu m}{0.35\,\mu m}=\frac{8\,\mu m}{0.35\,\mu m}$
M3	$\frac{4\cdot 6\,\mu m}{0.35\,\mu m}=\frac{24\,\mu m}{0.35\,\mu m}$

Layout vs. Schematic of Transmission Gate

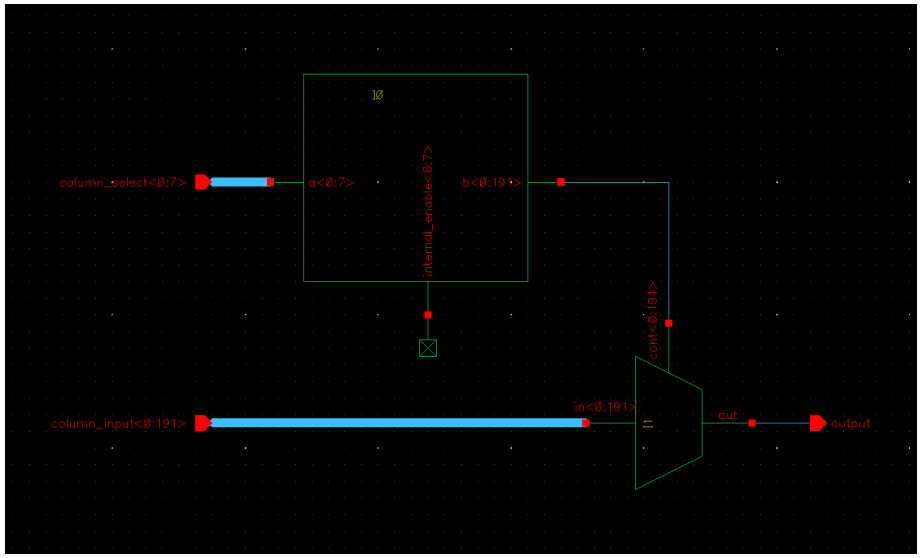
- There is no significant difference between the Layout and Schematic
- The Voltage drop between ‘in’ and ‘out’ depends on the Load





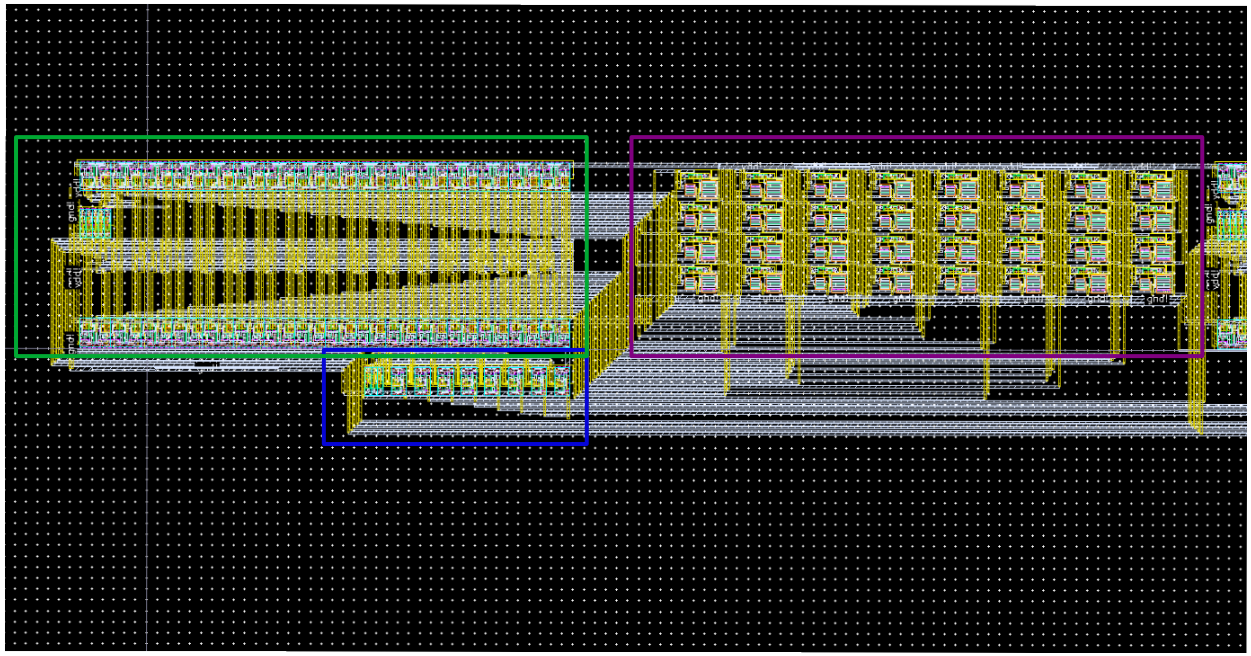
Design of Decoder with Analog Multiplexer

- Transmission gates are used to establish connections between the column inputs and the output
- Specific transmission gate that conducts is selected by the decoder, while the other transmission gates remain non-conducting
- Internal enable 6 and 7 are not needed



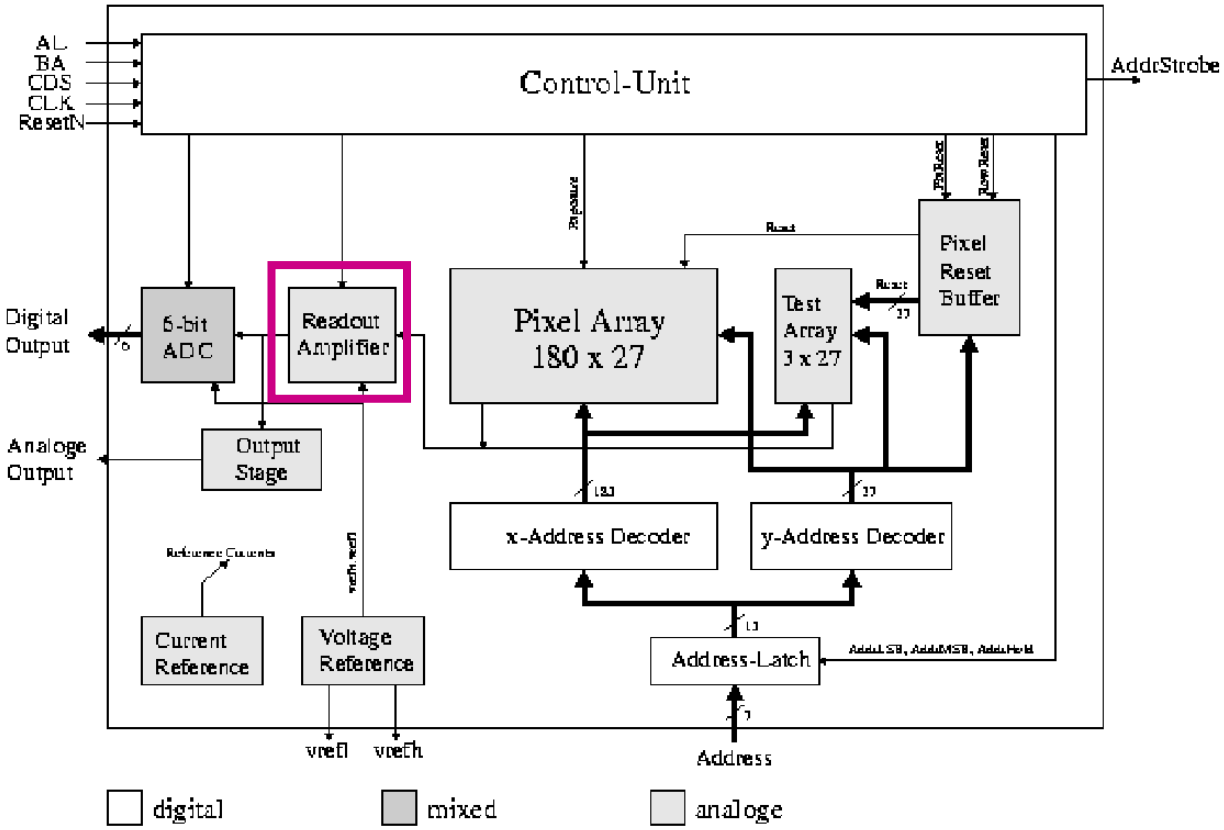
Layout of Decoder with Analog Multiplexer

- Decoder for enable signal
- 5 to 32 Bit Decoder
- 32 Transmission gates
  - 5 Decoder and transmission gates blocks
  - → 192 column inputs to 1 output



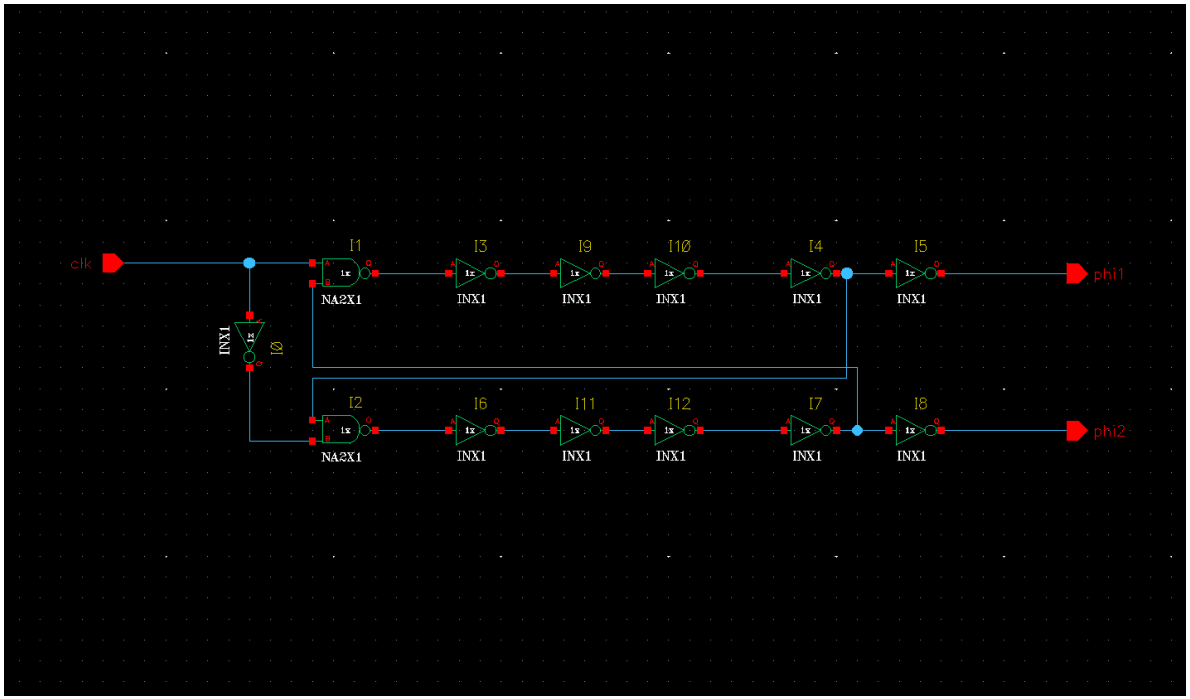
Design of Readout Circuit

Overview



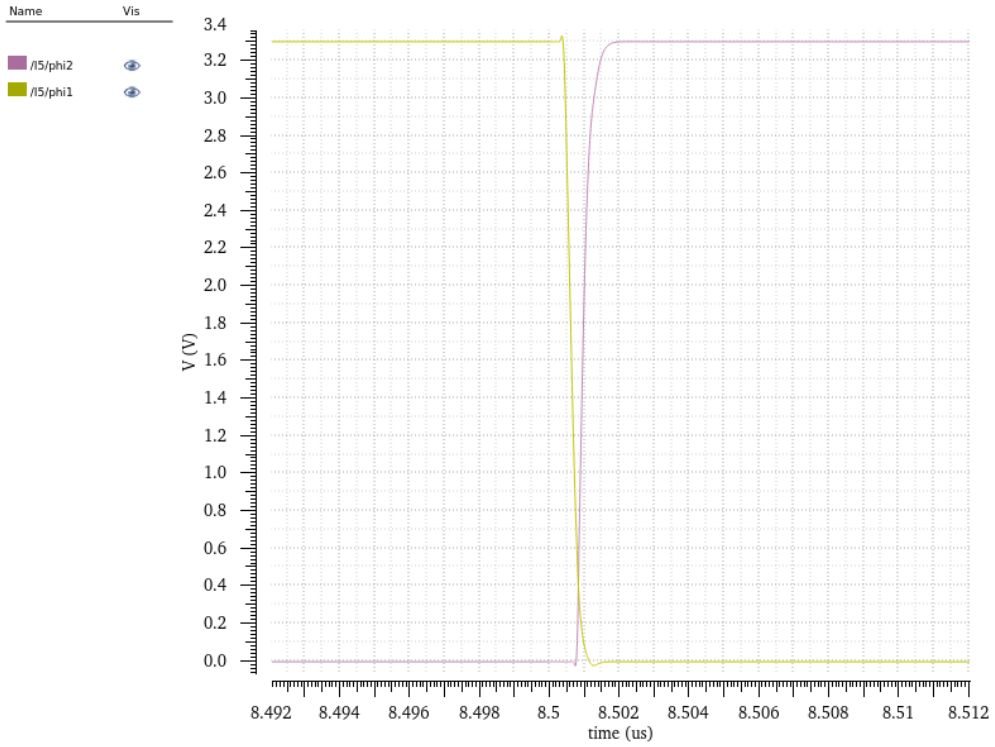
Design of SC-Amplifier
Non-overlapping clock generator

- A non-overlapping clock is needed for a switch capacitor circuit
- Delay is produced by a inverter chain



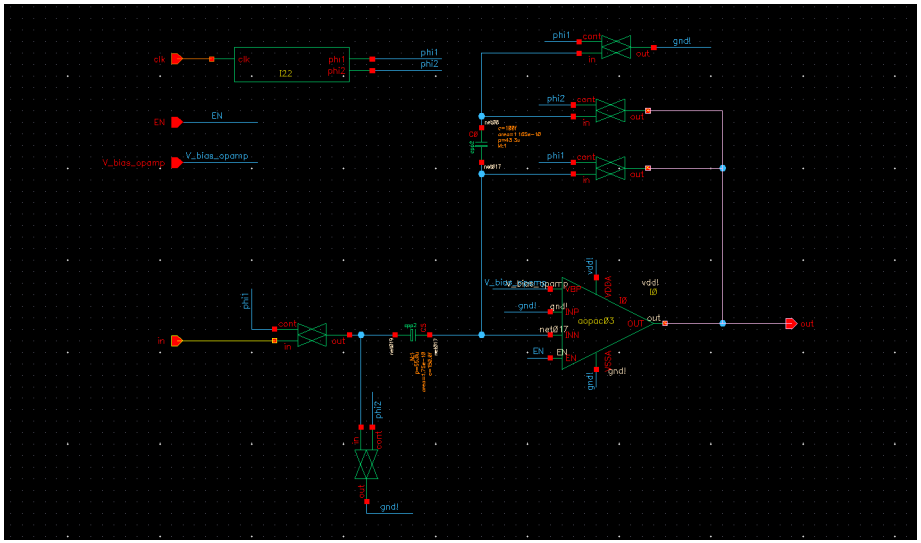
Design of SC-Amplifier
Non-overlapping clock generator

- The distance between falling and rising edge can be increased by the number of inverters
- The minimum distance is to be selected in such a way that the two clocks do not switch the corresponding device at the same time.



Design of SC-Amplifier
Schematic

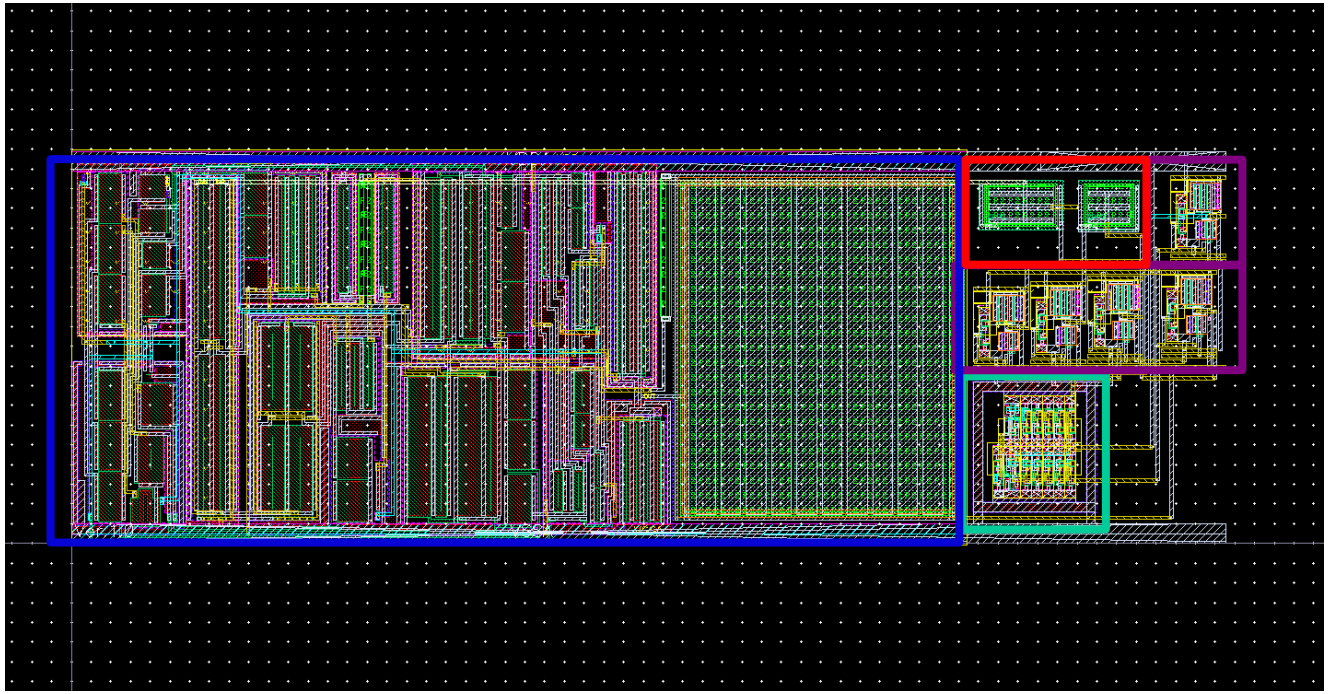
- A non-inverting SC-Amplifier was chosen because it has inherent offset compensation
  - ➔ $Gain = \frac{C_1}{C_2}$
- TGs are used for the switches
- An op-amp from xFab are used



Capacitor	Sizing
C1	150fF
C2	100fF

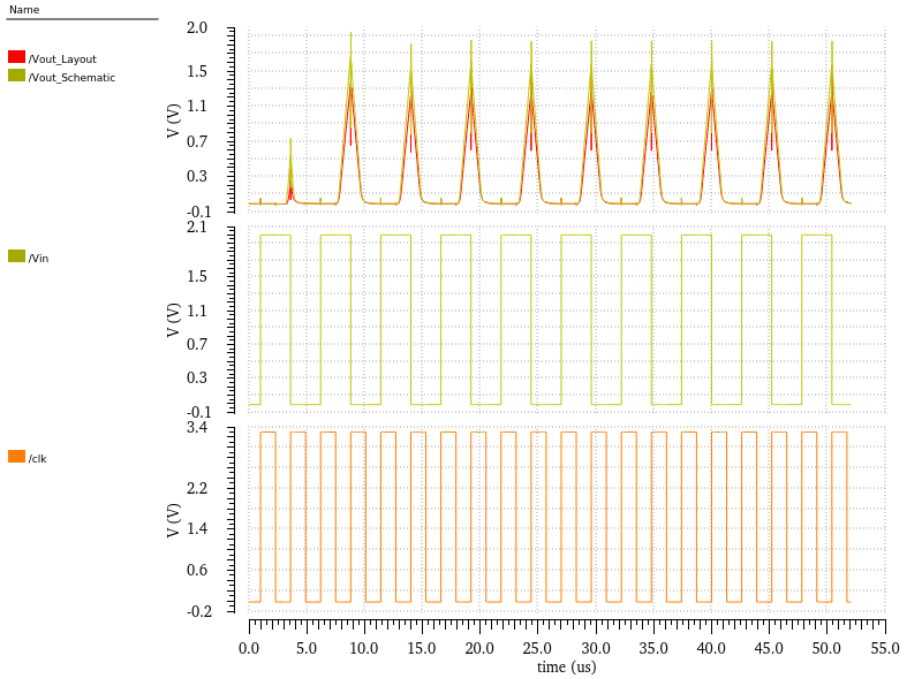
Design of SC-Amplifier
Layout

- Non-overlapping clock generator
- Switches
- Operation Amplifier (from xFab)
- Capacitors



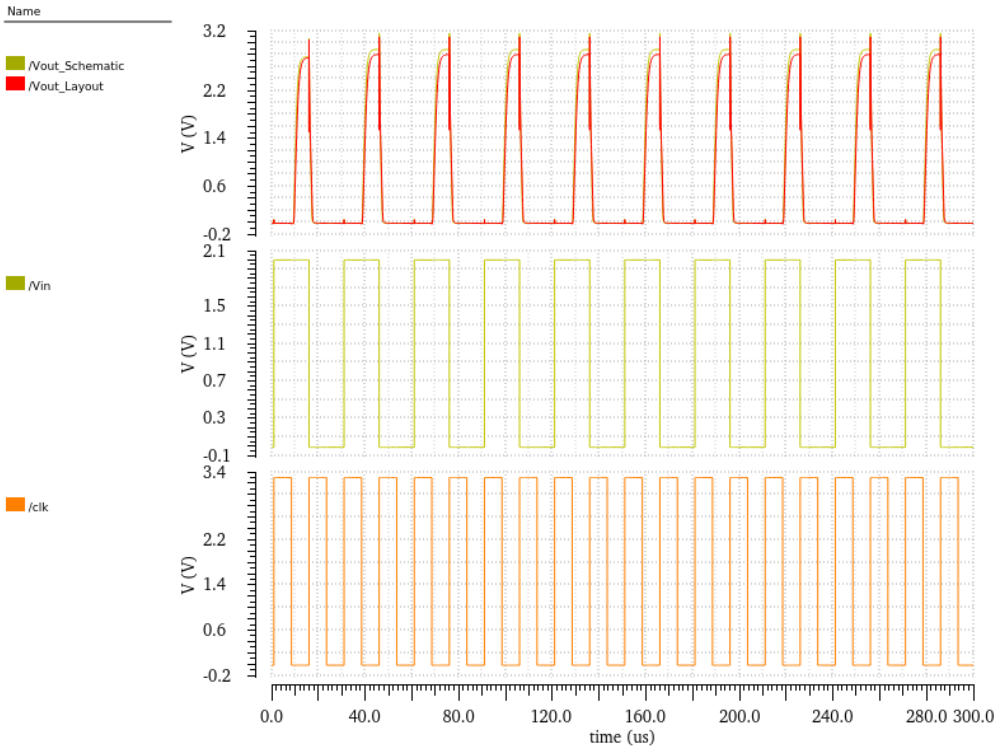
Design of SC-Amplifier
Layout vs. Schematic

- The slew rate from the Opamp is too slow for the required readout rate
- The Requirement is changed
  - Readout rate to 33.3 kHz
  -
  - 30 us per pixel

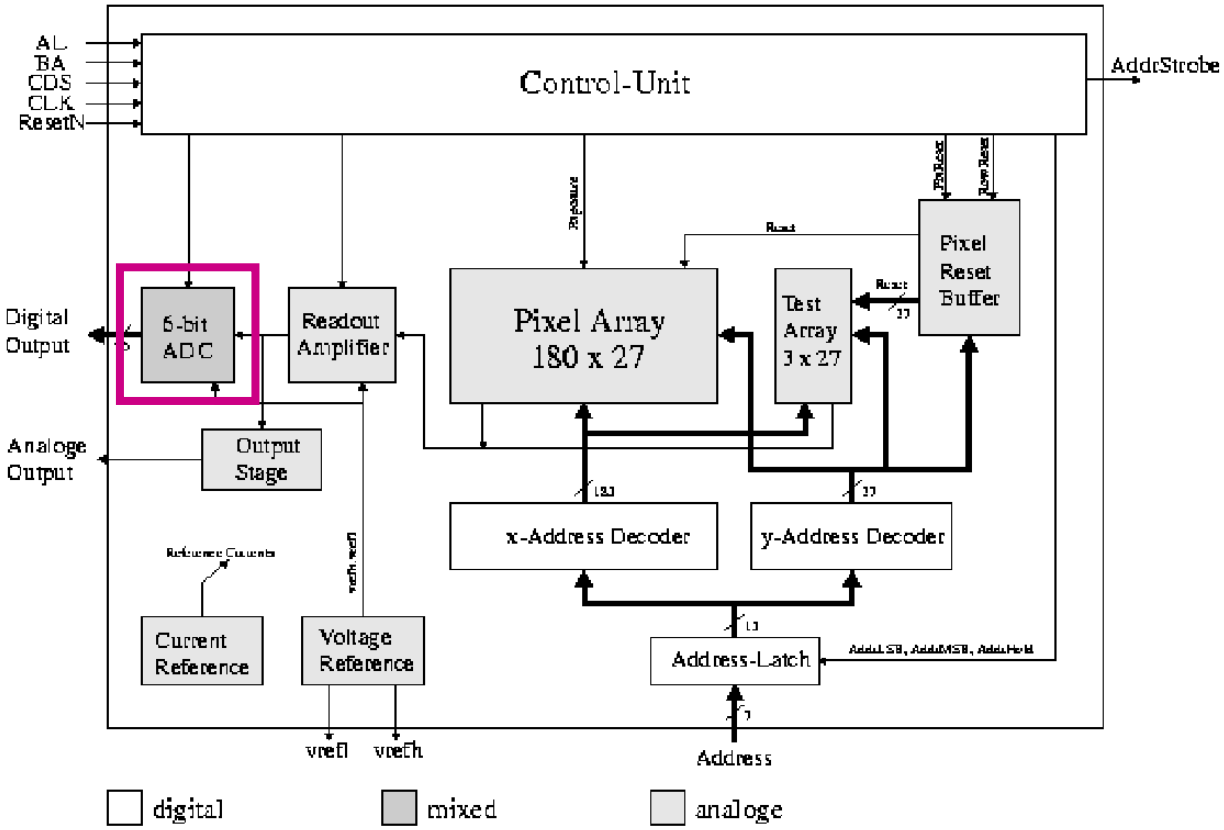


Design of SC-Amplifier
Layout vs. Schematic

- With the new requirements the SC-Amplifier works
- There is no significant difference between Layout and Schematic

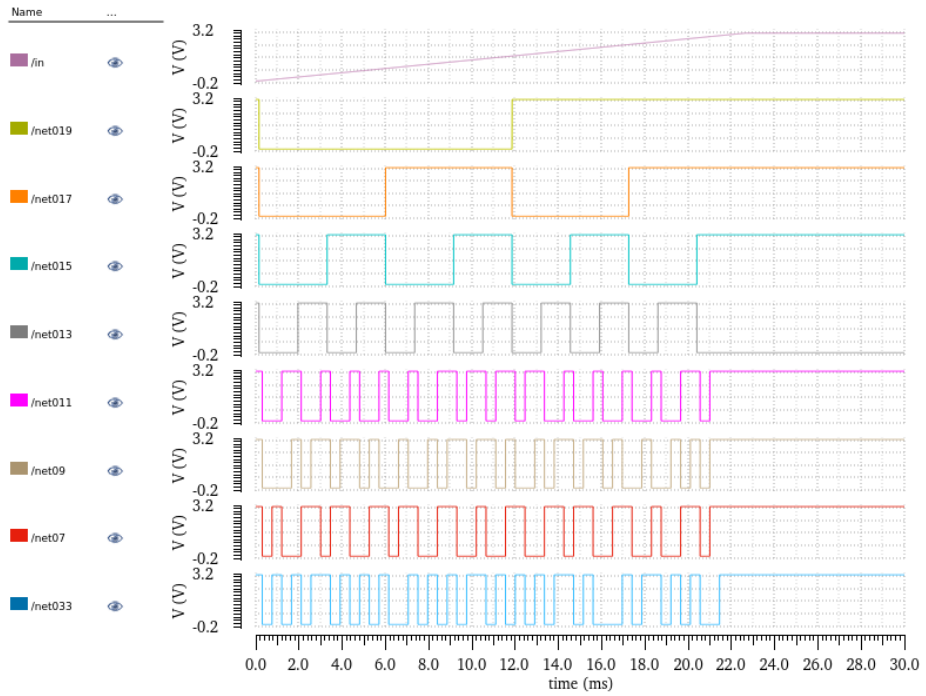


Design of ADC
Overview



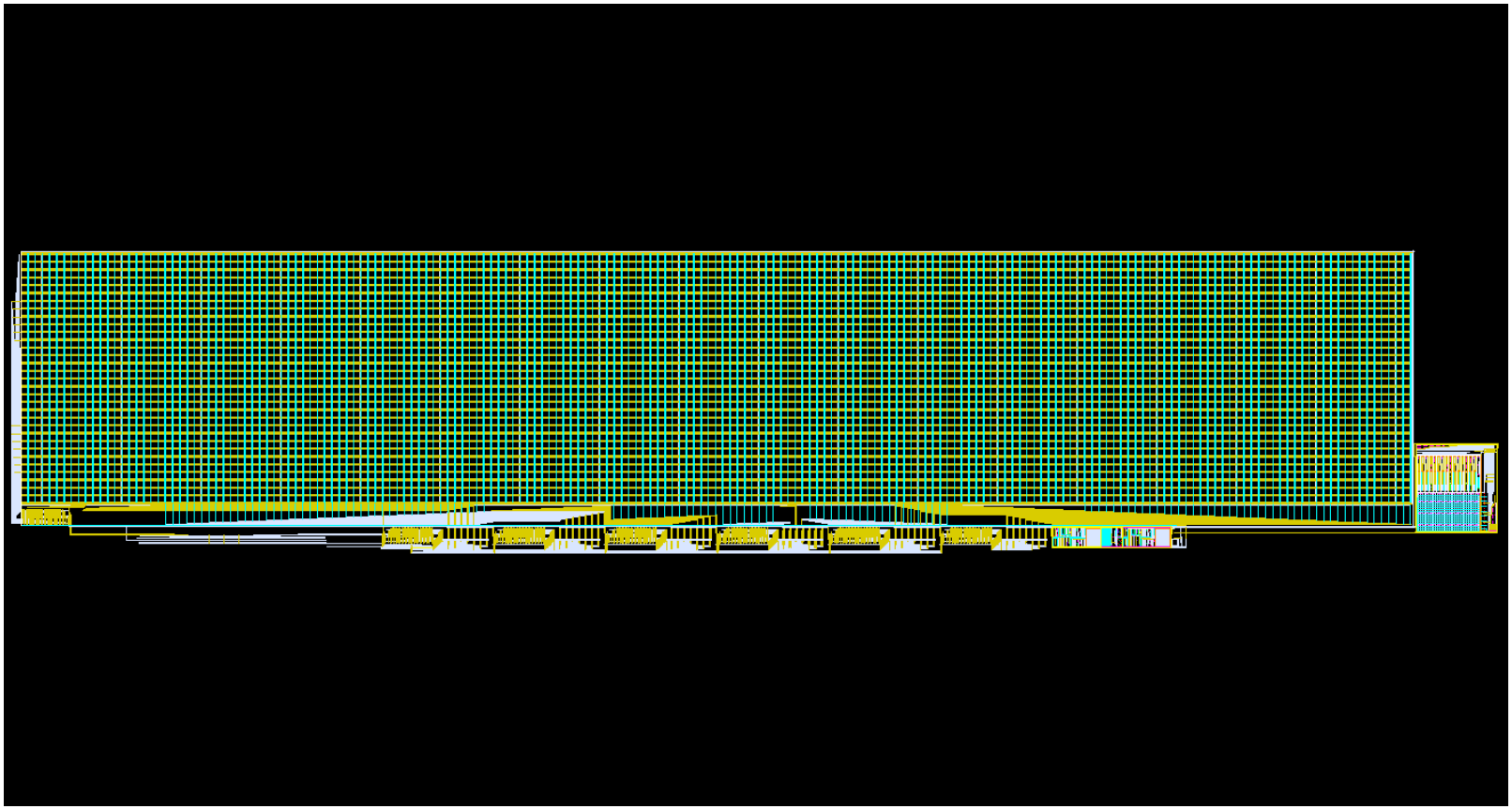
Design of ADC

- An ADC from xFab is used.
- The clock for ADC have to be faster than the clock for the SC-Amplifier, because the ADC have a conversion time of 3 clock cycles



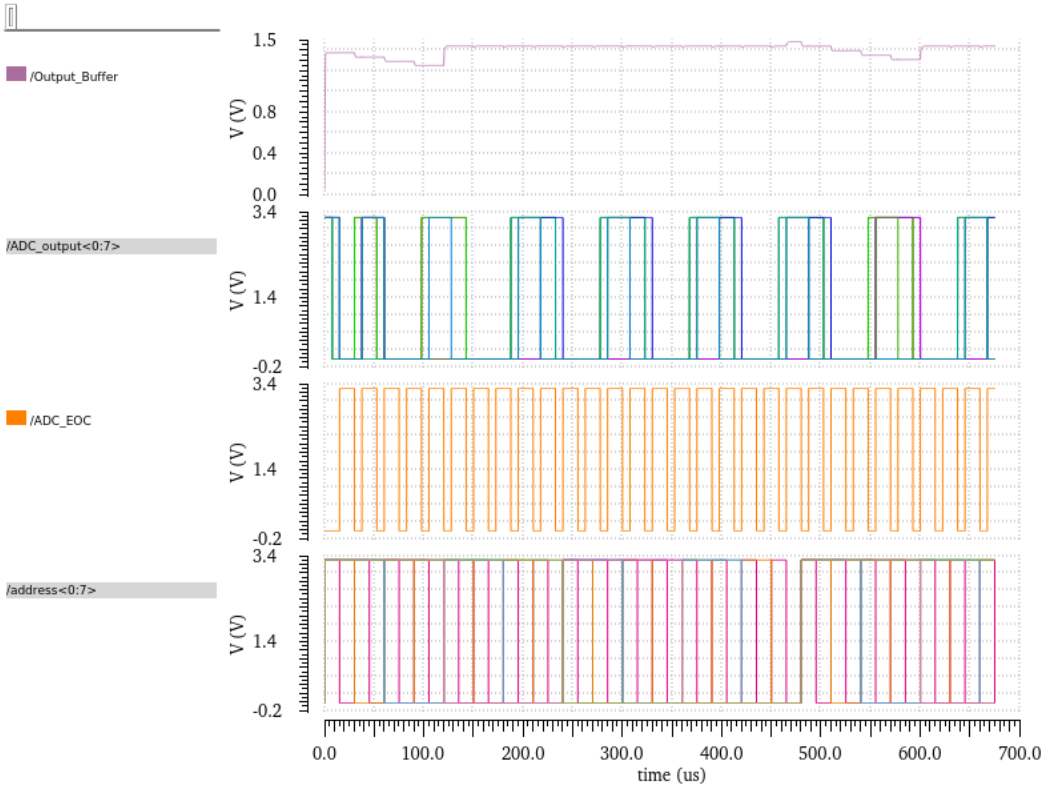
Top Level Hierarchical Layout

- Dimension: 6923.075 µm x 1408.8 µm



Post Layout Simulation

- Post Layout Simulation is not possible, therefore there is only the Schematic simulation



Future Work

- Design an Opamp with higher slew rate (approx. 15 V/us) to achieve the required readout rate
- Design an ADC for the exact requirements to avoid overhead in Layoutarea
- Verify post Layout design when more memory on the server is available
- Explore different sizing of Transistors and capacitor in APS cell to increase fill factor

Conclusion

- The project aimed at designing a pixel cell with a resolution of 192x32 in the 0.35um CMOS technology
- The designed pixel matrix, decoder, ADC, and readout circuit all functioned cohesively to capture and process images or data.
- Simulating the post layout of the active pixel matrix 192x32 reacquire high memory
- The top-level hierarchical layout was a critical step in translating the design into a physical layout.
- This project opens doors to several future opportunities. Potential improvements in the design and its adaptation for specific applications can be explored.

Thank you for your attention