Holistic Design of Reconfigurable, Low-Power Intelligent Sensor Systems

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1 Introduction

Intelligent embedded systems are of increasing importance in industrial and consumer applications and systems. Application domains comprise, e.g., mobile communication devices, games, monitoring devices or medical implants. In particular with the increasing variety of sensor devices, intelligent systems solving a diversity of recognition tasks for, e.g., autonomous system behavior or human-machine-interface, find more and more widespread application. Most recent application fields are summarized by the terms of ambient intelligence and distributed sensor networks. For this kind of application, appropriate integration or miniaturization techniques, adequate sensor devices, and sophisticated, application-specific signal processing are required. Further, the implementation of the required system, in particular its electronic components, have to meet additional constraints, such as real-time requirements or power consumption limitations. At the state-of-the-art, the design of recognition systems in general and integrated sensor systems in particular still is a predominantly expert-driven, tedious and labor-intensive task. The processing chain, depicted in Fig. 1 for the special case of vision, from sensor choice, over signal processing, feature computation, dimensionality reduction, and classification for decision making is instantiated manually according to existing experience and expertise. The quality of the overall solution very much depends on the involved experts ability. In particular the expense of resources and power in the later implementation is not explicitly cared for by this approach. In contrast, the design of integrated

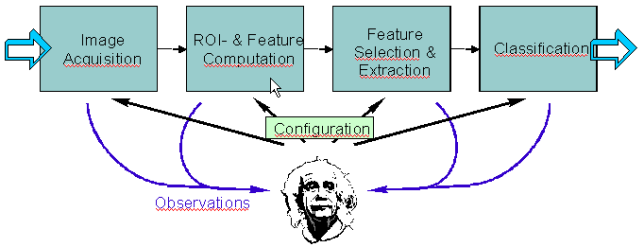

Fig. 1. Block diagram of recognition system

electronics is particularly well supported by design methodologies and tools, so that the physical implementation of the digital partition of recognition systems is a rather straightforward step. Due to well-known existing sensitivities of analog and mixed-signal circuits, the implementation of this system partition requires more attention, but is supported by methodologies and tools of increasing ability and quality.

However, the transfer of the obtained recognition system architecture to the hardware level and the effect of certain design options or compromises, e.g., reduced accuracy, behavioral deviations of analog circuits etc., can lead to significant performance deviations and intolerably reduced recognition rates. Thus, a design approach transcendent with regard to design levels is required, to assure the actual viability of implemented recognition systems. This issue as well as common remedies for potentially non-linear systems are well known from the domain of neural hardware design. Also, the significant potential of power conservation by appropriate choice of hardware-friendly operators could be exploited by coordinated design activities on both behavioral and physical levels.

This paper summarizes research activities of the last years, starting in 1998 to present, which were funded by a research project from DFG VIVA SPP 1062 for the first three years [8] [1]. The objective of this overall research work was to make a contribution to two key issues in the design of recognition systems. The first issue is related to the automation of the system design itself. The elaborated methodology and first tool implementations will be covered in the following section. The second issue is related to assuring system performance and obtaining minimum power consumption for the regarded task. Inclusion of the hardware model in the optimization or learning loop at design time as well as the hardware itself at deployment time is considered in a holistic design approach, which will be discussed in the third section. The fourth section will summarize particular design activities of hardware-friendly low-power sensor signal processing operators as well as reconfigurable low-power classifier. The fifth chapter will outline recent activities on dynamically reconfigurable sensor electronics for flexible and rapid system prototyping as well as self-trimming and -repairing properties. This work was largely inspired by the activities from the VIVA project. Concluding, open issues will be addressed and an outlook of upcoming activities will be provided.

2 Automation of Sensor System Design

Intelligent sensor systems require the definition of a principle architecture given in Fig. 1. In particular for multi sensor systems, each of the blocks basically can have a graph-like structure of cooperating methods. Thus, the choice of method itself, method parameters, and combination of methods on a certain processing level, e.g., feature computation, are the design tasks to undergo for each new application. The design could be founded on a knowledge-based approach, in-

fering one solution from previous experience, or the design could base on the machine learning paradigm learning from examples, which means appropriate samples have to be collected along with supervisor or target information and system configuration takes place based on performance assessment in a learning or optimization loop. Training neural networks is the typical example for this case. The techniques have been abstracted to the levels of dimensionality reduction and in more recent works also to feature computation [12] [14] and by some means also to sensor and scene optimization. In the reported work, with some bias to vision application, a general recognition system design framework, denoted as QuickCog has been conceived in the late nineties. The architecture of this system is illustrated in Fig. 2. Performance assessment based on

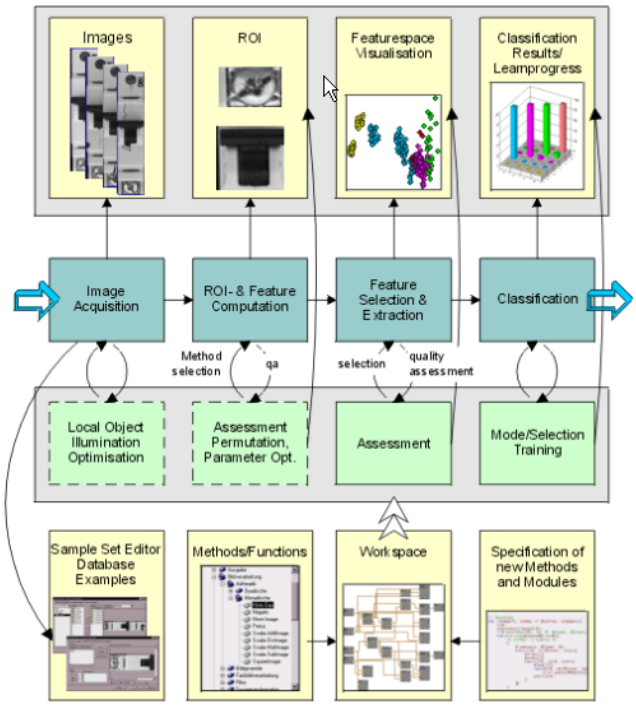

Fig. 2. Architecture of the QuickCog system

classification results as well as immediate feature space assessment by overlap, separability, or compactness measures are provided and used for open-loop as well as closed-loop optimization. Automatic selection of features is one closed-loop optimization example, that is employed in a case study for face tracking. Heuristic as well as stochastic or evolutionary optimization techniques have been studied in this context and in part have been implemented in the tool. Assessment measures have been employed and enhanced also to assess potential

effects of implementation options on system performance [1].
In more recent research work several improvements have been investigated. This includes additional techniques from the field of swarm intelligence, e.g., particle swarm optimization (PSO), which proved to be beneficial with regard to speed and result quality. Also, multi-objective optimization was investigated, both for cooperative application of several assessment measures as well as the inclusion of cost as an additional constraint [13]. This work explicitly introduces the option to include power consumption as an issue into the optimization process. In particular in conjunction with dimensionality reduction methods, lean and efficient yet well-performing recognition systems can be systematically constructed, or better, evolved. The QuickCog system, that also features dedicated interaction and visualization features for transparent sample collection and system design, was used as the platform for behavioral modeling of application-specific recognition systems, e.g., a face tracking system, and linked to chip design tools for validation and optimization of dedicated sensing, feature computation, and classification. The objective of this approach was, to achieve power savings on the behavioral level as well as by cooperative design activities between physical and behavioral level. This will be picked up in more detail in the following section.

3 Holistic Sensor System Design

Design options and compromises, circuit limitations, as well as the inevitable static and dynamic deviations due to manufacturing tolerances and drift phenomena have significant impact on the performance of sensors and corresponding electronics. The analog and mixed-signal system partitions are in particular vulnerable to numerous sources of influence. So, it cannot be a priori expected, that an electronic embodiment of an application-specific architecture elaborated by the approach and techniques of the previous section will perform exactly as its simulation counterpart, i.e., the yield of the resulting electronic embodiment will be compromised by significant deviations from the behavioral system implementation. However, the applied learning and optimization techniques basically allow to compensate weaknesses by collective adaptation, if informed on the underlying problem. Thus, the inclusion of the actual component into the optimization loop is an effective means to exploit collective parameter adaptation of one or several methods to compensate realization deficiencies.

This approach has first been introduced by Intel for its (*Electrically Trainable Artificial Neural Network*) ETANN chip, which implements multi-layer feed-forward neural networks in analog technology for classification. The chip suffers from significant scattering of neuron and synapse characteristics, but due to programmable synapses can be adapted. Host-based training of network synapses is not aware of these deviations, and, thus, returns weights which will not offer optimum performance after uploading in a chip instance. Inclusion of the chip in the learning loop allows the learning algorithm to effectively

compensate instance-specific deficiencies. This approach, denoted as Chip-In-the-Loop-Learning (CHILL) can be extended both to more complex system implementations, including lower-level processing, as well as to the design-level [6]. Generalizing the applied optimization procedure from gradient descent techniques to methods from Evolutionary Computation (EC), the CHILL concept is illustrated in Fig. 3 (left), and the extension to design-level is illustrated in Fig. 3 (right). These two cases in the context of Evolvable Hardware today are denoted as intrinsic and extrinsic evolution, respectively. EC optimization has the salient advantage compared to gradient descent techniques to be able to avoid local minima and potentially reach better solutions. In the extension to

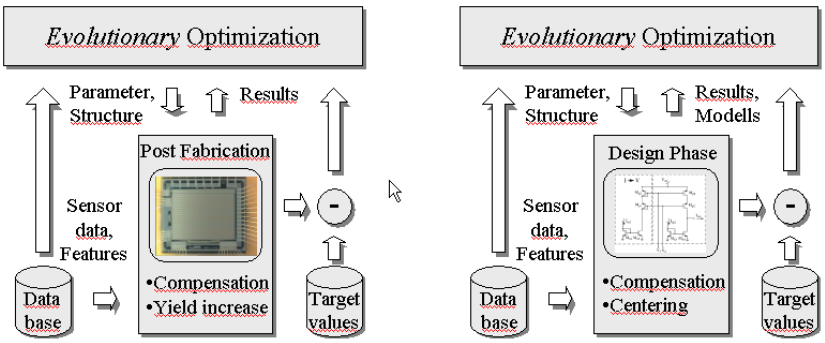

Fig. 3. CHILL concept (left) and the extension to the design level (right)

design level, behavioral information of the circuits under investigation have to be fed to the learning algorithm. This could be achieved by straightforward, yet cumbersome export of stimuli and parameter data to the circuit design environment, e.g., CADENCE DFW II, and simulation result import back to the learning loop for error computation and parameter update (s. Fig. 4). Also, validation of circuit and architecture choice can be carried out this way. A more elegant and considerable faster approach is the extraction of a simple but effective model of the circuit under investigation, using techniques such as look-up-tables or parameterized analytical models, and the inclusion of these models in the host-based learning system software implementation. For the case study of an analog low-power reconfigurable nearest-neighbor classifier, the chosen circuits and architecture has been validated employing the first approach, depicted in Fig. 3 (right) and Fig. 4. The regarded classifier was investigated for eye-shape data classification [6] [1] to serve as a component in a dedicated low-power implementation of an eye-tracker system for 3D-display application. In the context of this face-tracker case study [11], eye and no-eye shapes were collected from various scenes and feature computation was applied employing three major techniques in a comparative study (s. Fig. 4 (lower left)). Two of those methods will be discussed along with particular implementations of

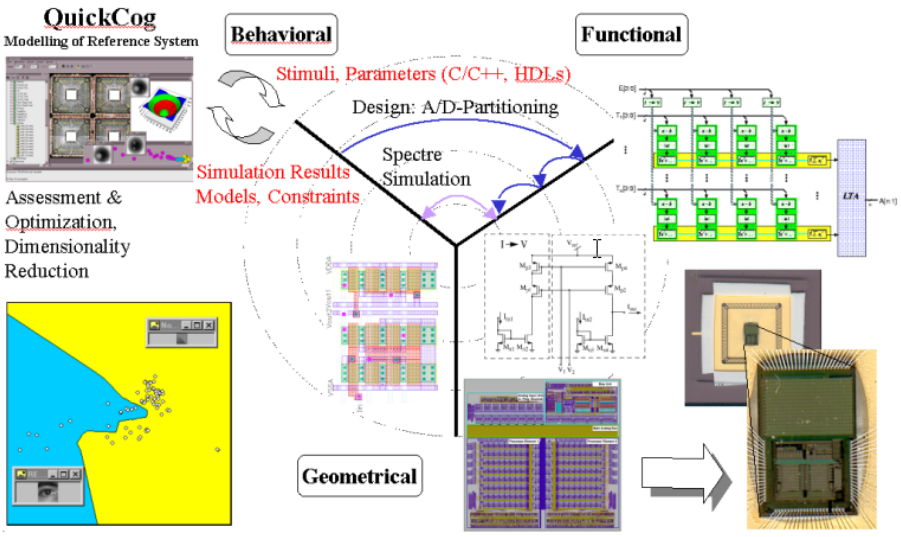

Fig. 4. Level transcendent GAME design methodology employing CHILL concepts

two simple and effective techniques in the following section. Dimensionality reduction by automatic feature selection was applied and followed by classifier training, which employed an heuristic reduction technique that limits the number of required reference vectors and alleviates the parallel implementation requirements [11].

4 Dedicated Recognition System Electronics

The concepts pursued in the overall research work were investigated for two particular implementation efforts based on the overall face-tracker case study. The first effort dealt with vision applications and particular options for hardware-friendly, low-power operators for oriented feature computation. This work lead to two architectures and vision chip implementations discussed in the first subsection. The second effort dealt with the implementation of a low-power reconfigurable 1NN-classifier. Cells of a dedicated low-power cell library for signal processing and classification, denoted as ULPAC [7], which was established as one part of the research work and the design methodology, were employed.

4.1 Image sensors with HDR Oriented Feature Computation

Vision applications, e.g., for surface inspection, object recognition, or tracking tasks, rely on appropriate feature computation in real-time. In particular, oriented features mimicking the information processing encountered in the hypercolumns of the visual cortex are a powerful means. Commonly, Gabor filters

and Gabor jets [9] are applied for oriented feature extraction. Though being very powerful, precision requirements are high, and digital implementations of this approach are computationally prohibitive. In this work, two simple and proven methods, the local autocorrelation (LAC) [2] [3] and its extension [10] (Extended LAC, ELAC) and the local orientation coding (LOC) were investigated as efficient alternatives. These methods commonly work with a 3×3 local neighborhood centered on the reference point and 25 masks[4] [10]. This is especially advantageous for planar VLSI implementation. Based on standard LAC, an enhanced method with local competition was introduced, which determines the strongest responding mask locally for each pixel. In this ELAC method ex-

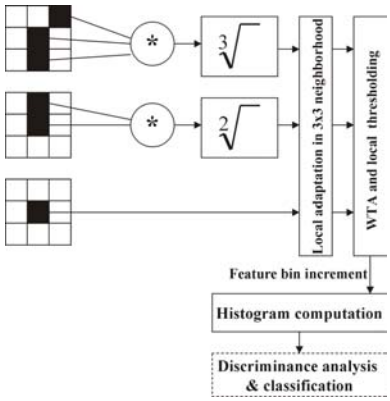

Fig. 5. Block diagram of the ELAC method.

plained in Fig. 5, the index of the prevalent orientation is digitally stored in each pixel. Thus, inherent A/D conversion lends itself naturally to this method. Figure 8 shows two pseudo images, where black dots indicate the prevalence of a horizontal or diagonal local orientation, respectively. Employing a scanning window over the image, a histogram can be computed as a characteristic fingerprint of the gray-value image contents at each position which can be used as feature vector in the following. Alternatively, second or higher order statistics could also be applied. Illumination invariance and spurious mask associations to monotonous image regions are avoided by thresholding the mask response. Responses below the given threshold are rejected, which leads to the increment of an additional histogram bin. Before thresholding, the mask response is normalized by the local gray value average. Thus, we achieve a local thresholding and effectively combine local adaptation mechanism and feature computation, which is a salient baseline for integrating both steps in a vision chip and system.

A first ELAC implementation was investigated in an 0.8μm 2M/2P CMOS technology. Figure 6 (left) shows a block diagram of the ELAC sensor pixel cell.

Illumination invariance and high dynamic range (HDR) properties are incorporated by the computation of a local average in each pixel for normalization, employing a common 2D smoothing network with MOS-transistors in subthreshold operation as controllable resistors. Normalization makes response comparison

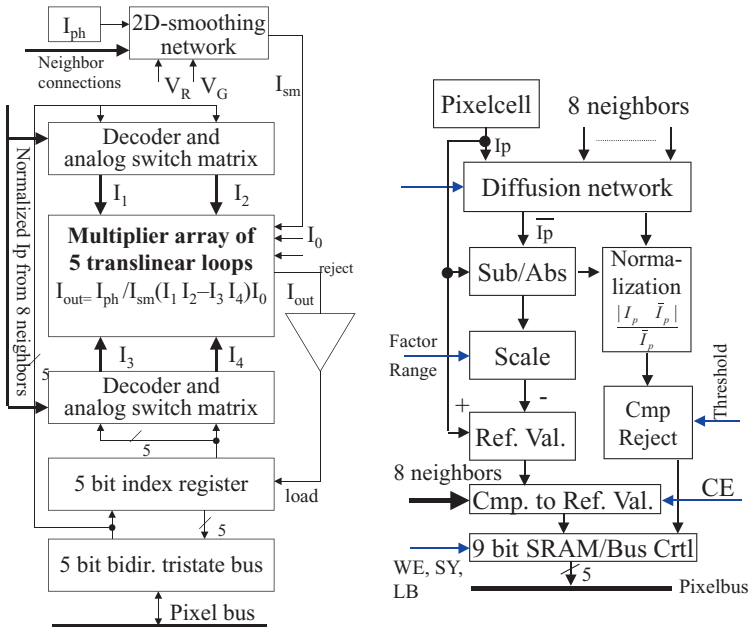

Fig. 6. Pixel cell block diagram of the ELAC chip (left) and the LOC chip (right).

of two and three pixel masks feasible (s. Fig. 5).
The selected orientations are successively computed and the index of the winning orientation is stored in the pixel feature register. The current orientation index is broadcasted by the controller to all pixels in the matrix. Thus no analog storage is required. Five one-quadrant multipliers (translinear loops) compute responses of current orientation and recent winner. These are compared and the pixel register is accordingly updated. Finally, the winning mask response is compared to a reject threshold to exclude low contrast regions with potential spurious orientation affiliation from further processing. So, the pixel register contains either the code of the winning mask or the reject code. The layout of the cascadable pixel cell and the prototype chip with 16 × 16 pixels are depicted in Fig. 7. The ELAC pixel cell design consists of 252 transistors, occupies $220\times204\mu m^2$ area, and consumes $100\mu W$ @3.3V. The computation of one orientation consumes $500\mu s$, thus, 20 orientations can be computed in 10ms. Allowing 10ms for digital readout of the matrix, 50 frames/s can be expected from modestly sized matrices. The photo sensitive area occupies $20\times20\mu m^2$

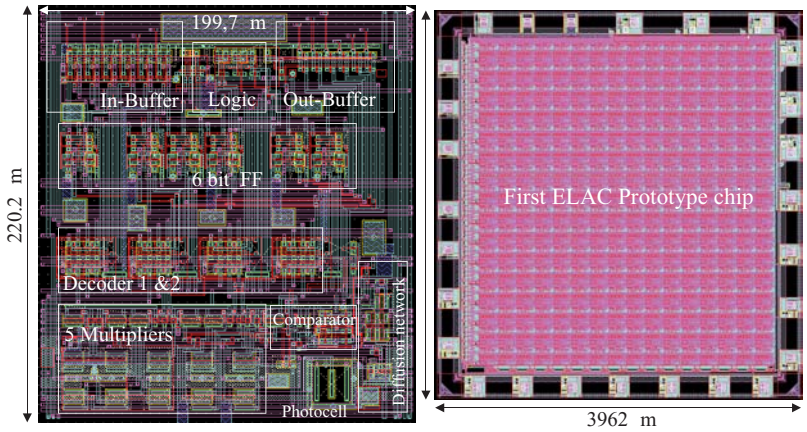

Fig. 7. Pixel cell and chip layout of the ELAC retina.

which implies a fill factor of only 0.89%. For the prototype chip, only address decoders, digital buffers and I/O-pads as well as four analog bias or control signals are required (V_R, V_G, I_0, Θ_{reject}).

The second regarded Local Orientation Coding (LOC) method [5]), though being a nonlinear feature computation method, is even simpler, as basically no multiplication is required. The registered pixel gray-value is compared to each of those of the four (eight) neighbors. According to the outcome of each compar-

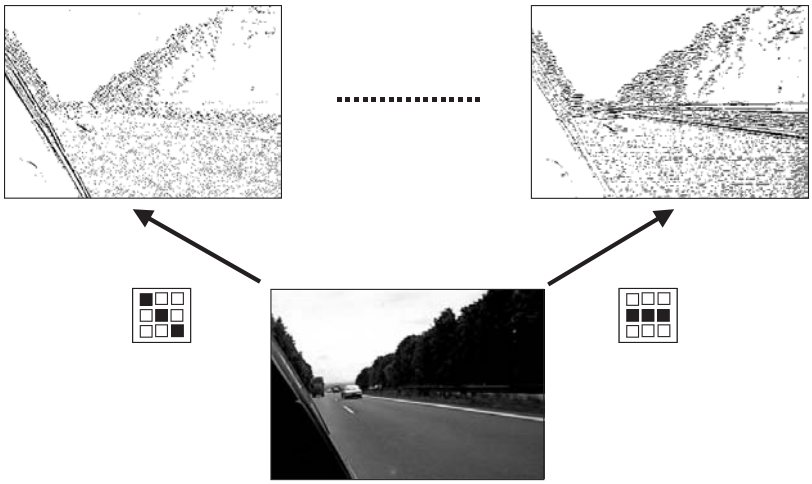

Fig. 8. ELAC coding examples.

ison, a dedicated bit pattern is generated for the N_4 or N_8 neighborhood, that codes the prevalent local orientation [5]. The resulting sum is uniquely separable into its components, thus, preserving the local orientation information [5]. The result is amenable to simple post processing employing bit arithmetic and also can be used for line detection or flow-field computation [5]. In the LOC retina architecture, the principal design features of ELAC have also been applied.

For the LOC retina, a 0.6μm CMOS 3M/2P technology was chosen. Fig. 6 (right) shows the block diagram and the computational steps of the LOC retina architecture, which implements an N_8 neighborhood and, including a reject code, requires a 9 bit register. Local average and reject computation is identical to the ELAC retina. The prototype chip has 16 $\times$ 26 pixels, which feature 169 transistors, an average power dissipation of 2μW3.3V, $\approx$ 130 $\times$ 100 μm^2 area, and 10ms computation time for all orientations (50 frames/s) (s. Fig. 9). This

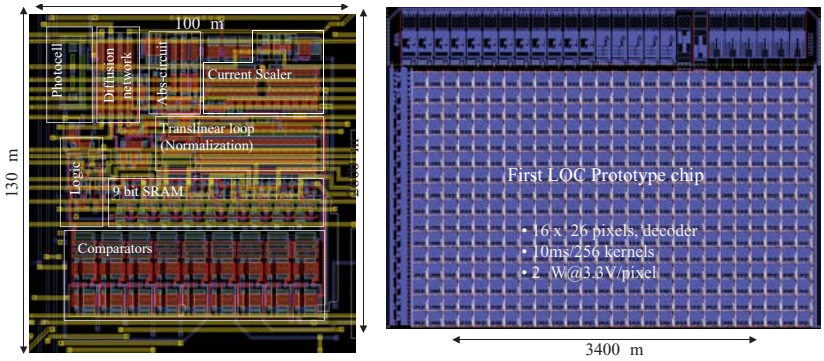

Fig. 9. Pixel cell and chip layout of the LOC retina.

more advantageous LOC-implementation requires four global analog parameters for the smoothing network, the rejection threshold, and the scaling factor (s. Fig. 6 (right)). The LOC chip pixel can be further down-scaled by introducing sequential orientation computation as done in the ELAC retina. Also, introducing negligible additional digital circuitry, parallel HDR gray value registration with pixel parallel A/D conversion will also be feasible, which is interesting, e.g., for more complex active vision system architectures.

4.2 Reconfigurable 1NN-Classifier

Based on the ULPAC circuit library [7] and the preliminary investigations and validations by simulations for the case study, a reconfigurable 1NN-classifier was designed in CMOS technology and subthreshold operation [6] [1]. Block diagram, architecture, and layout of this low-power 1NN-classifier is given in

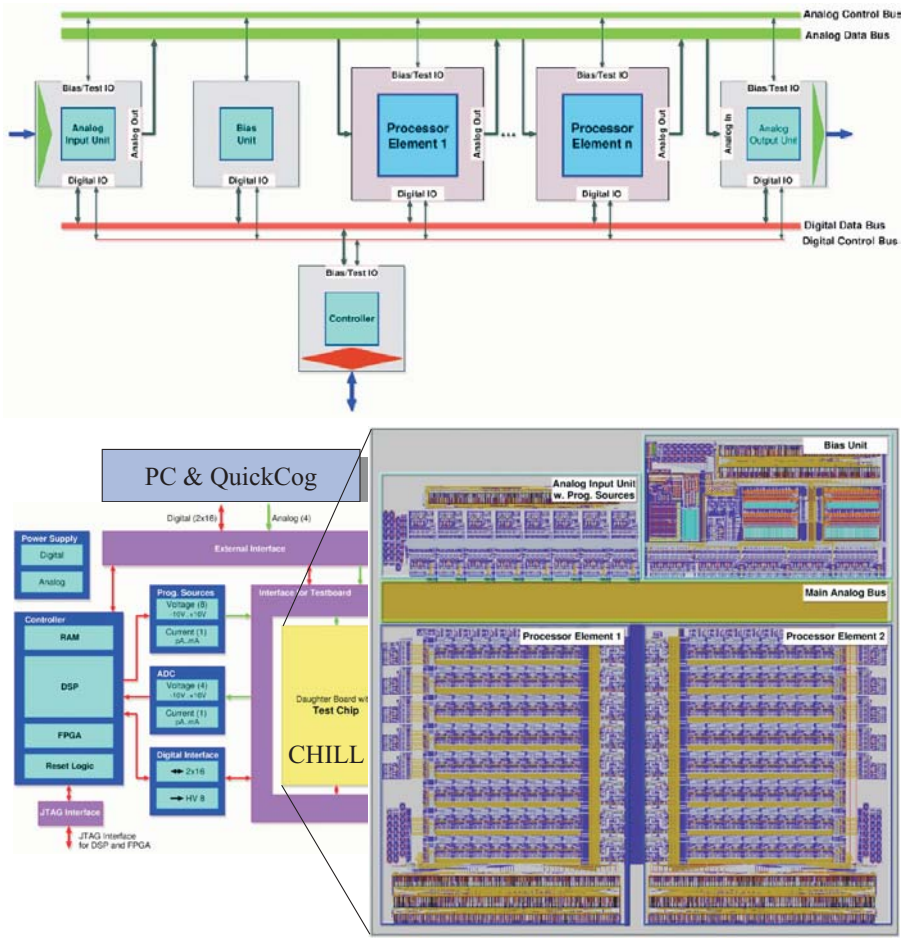

Fig. 10. Block diagram, architecture, and layout of low-power 1NN-classifier

Fig. 10. The chip incorporates two 8×8 fields of 1NN-classfiers as described in detail in, e.g., [1]. The two fields are complemented by framing circuits for interface and biasing purpose. Reconfigurability is achieved by externally loadable 6 bit RAM and DA-converter per synapse or reference vector component. The envisioned connection to the QuickCog architecture for programming or CHILL for compensation is also illustrated in Fig. 10. The CHILL concept application requires an extension of the initially employed Reduced-Nearest-Neighbor technique RNN to GA or PSO based technique. The selection of reference vectors was pursued sucessfully for PSO in recent work and in ongoing research issues of PSO-based compensation will be studied. The 1NN-classifier chip was also

manufactured in 0.6μm CMOS technology and packaged and bonded together with the LOC chip (s. Fig. 13).

5 Dynamically Reconfigurable Sensor Electronics

The application of reconfiguration concepts for analog and mixed-signal low-power circuits, as exploited for the 1NN-classifier, in general is attractive, but with regard to area requirement and associated cost, mainly are applicable for early signal conditioning and processing in sensor electronics. Actor electronics, of course, represent a similar case with the potential of later result transfer. The growing amount of different existing sensor principles and the increasing application of heterogeneous multi sensor systems both require improvements of flexibility and rapid-prototyping as well as self-calibration, self-trimming, and self-repairing aspects. In recent work [15], inspired by the described research work and other activities in evolvable hardware, the design of medium granularity reconfigurable analog arrays has been pursued. Both hardware and software aspects related to appropriate optimization techniques are regarded. In this approach, which bears some similarity to the CHILL concept, instead of weights or classifier parameters, aspect ratios and connectivity of devices, e.g., transistors, are adapted by switch patterns loaded into the reconfigurable chip. Based on appropriate measurement concepts, the switch patterns are determined in an optimization loop by GA or PSO techniques to meet and maintain a specifications. Currently, in the context of evolvable hardware, this concept is pursued by several research groups world wide. This groups particular interest lies in the design of linear circuits of standard topologies with predictable behavior [15]. This limits the reconfiguration concept to dynamic dimensioning of circuits, e.g., Miller or other amplifier topologies. Various circuits and optimization techniques have been studied on the basis of simulations and first silicon of the approved concepts is awaited from production to validate the results by measurements. A key issue in the context of low-power sensor system application, e.g., for mobile devices or medical implants, is the extension of the reconfiguration concepts to subthreshold designs. Subthreshold circuits are very vulnerable to deviations and, thus, reconfiguration is a promising concept. The effect of the distributed structure with the included switches was studied based on subthreshold Miller-OPA. Encouraging simulation results were obtained (s. Fig. 12) and the concept will be pursued to implementation for different amplifier architectures and low-power reconfigurable application circuits.

6 Conclusions

This paper summarizes activities on multi sensor recognition system design under the particular constraints of low-power design, rapid-prototyping and design automation, and compensation of static and dynamic deviations. Inspirations for nonlinear and linear processing and corresponding circuits were drawn

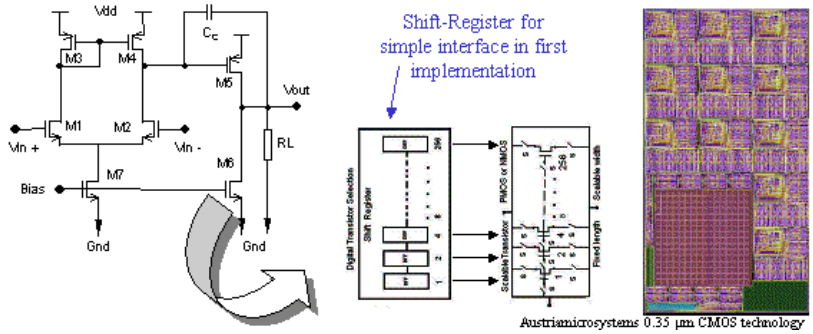

Fig. 11. Reconfigurable Miller OPA implementation in CMOS technology.

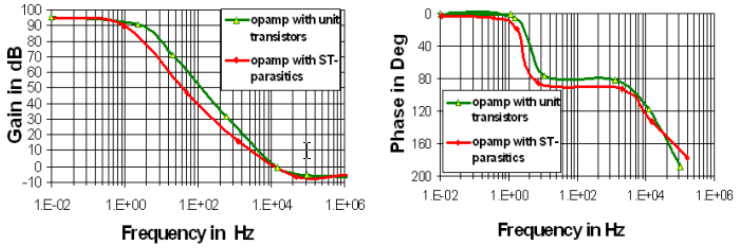

Fig. 12. AC simulation results for reconfigurable subthreshold Miller OPA: magnitude (left) and phase (right)

from the fields of Neurocomputing, Evolutionary Computation, and Neural and Evolvable Hardware. The work was conducted at two sites and numerous contributors under the supervision and guidance of the author. The work at TU Dresden was funded for three years in the GAME project in the six years duration DFG priority program VIVA SPP 1076. The second part of the work was in part self-financed and industry supported research at TU Kaiserslautern. The project has pursued technically relevant but ambitious goals with funding duration limited to just half of the VIVA program duration. So, studies on principle concepts and solutions, tool implementations and case studies have been conducted mainly on algorithmic level. Also, physical measurements for the chips given in Fig. 13 designed in the context of the case study of eye shape classifier for face tracking could not be gained. The developed approach, methodology, as well as first tools can be abstracted to other application domains in the field of integrated multi-sensor systems and their applications. For instance the two recently emerged fields of ambient intelligence and sensor networks are clearly in need of the introduced methods and algorithms. More recent priority programs on reconfigurable computing and organic computing, exploiting at large concepts of, e.g., reconfiguration, self-observation, -trimming, or -repair, in particular in the digital domain underpin the viability of the general chosen

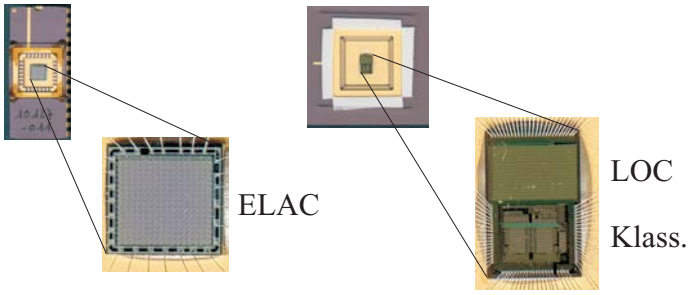

Fig. 13. Manufactured chips : ELAC (left) and combined LOC/classifier (right)

approach.
However, the concepts of analog and mixed-signal implementation with regard to the performance of digital systems is limited to processing tasks in high spatial proximity to actual sensor elements. This small yet ubiquitous domain is an attractive candidate and is currently investigated for reconfigurable implementations on the level of analog arrays, in particular, for low-power applications. One major difficulty for dynamic reconfiguration of linear circuits is the embedding of appropriate measurement electronics for the assessment and optimization loops. Nonlinear signal processing approaches potentially can offer remedies in some cases, but at the loss of transparency. Also high speed or extremely low-power requirements for limited complexity, e.g., in distributed sensor networks could also advocate picking up and continuing the concepts developed in GAME under DFG VIVA grant.

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